HN58V1001 Series

132K x 8-Bit CMOS
Electrically Erasable and Programmable ROM

Preliminary
Rev. 0.01

HITACHI®

The Hitachi HN58V1001 is an electrically erasable and programmable (EEPROM) organized as 131,072-word x 8-bit. It realizes high speed, low power consumption, and a high level of reliability, employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 128-byte page reprogramming function to make its erase and write operations faster.

Features

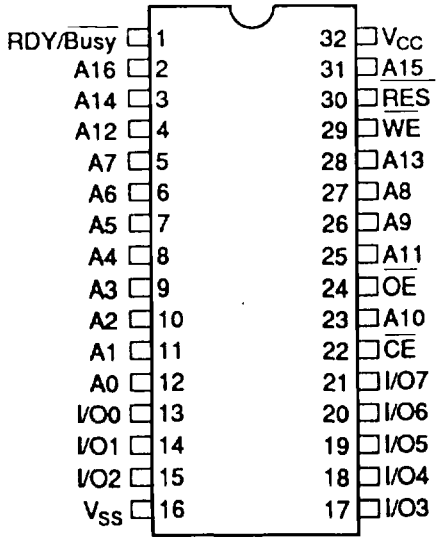
- Single 3 V supply
- On-chip latches:
  Address, Data, CE\, OE\, WE\
- Automatic byte write: 15 ms max
- Automatic page write (128 bytes): 15 ms max
- Fast access time: 200 ns max
- Low power dissipation:
  20 mW/MHz, typ (active)
  100 µW max (standby)
- Data \ Polling and Ready/Busy\
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Data protection by RES\pin

Ordering Information

Type no.	Access time	Package
HN58V1001P-20	200 ns	600 mil 32-pin plastic DIP (DP-32)
HN58V1001FP-20	200 ns	525 mil 32-pin plastic SOP (FP-32D)
HN58V1001T-20	200 ns	8 x 14 mm 32-pin plastic TSOP (TFP-32DA)
HN58V1001R-20	200 ns	8 x 14 mm 32-pin plastic TSOP (reverse) (TFP-32DAR)

Pin Arrangement

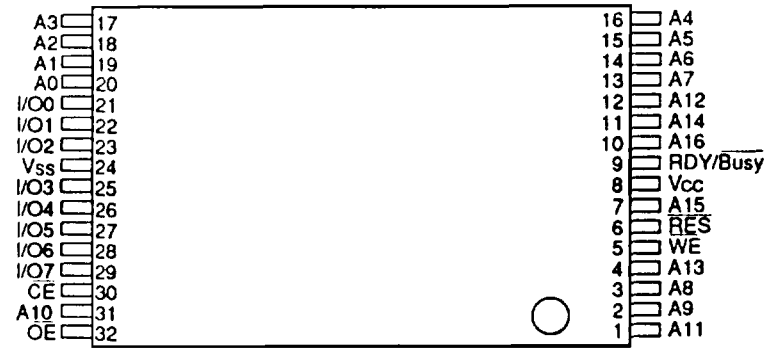
• HN58V1001P/FP Series



(Top View)

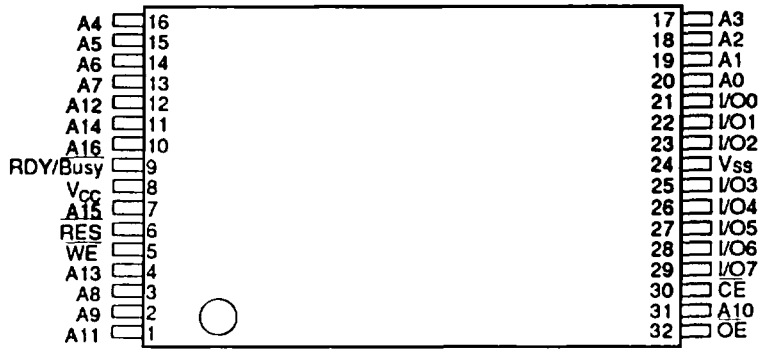
Pin Arrangement (cont)

• HN58V1001T Series



(Top View)

• HN58V1001R Series



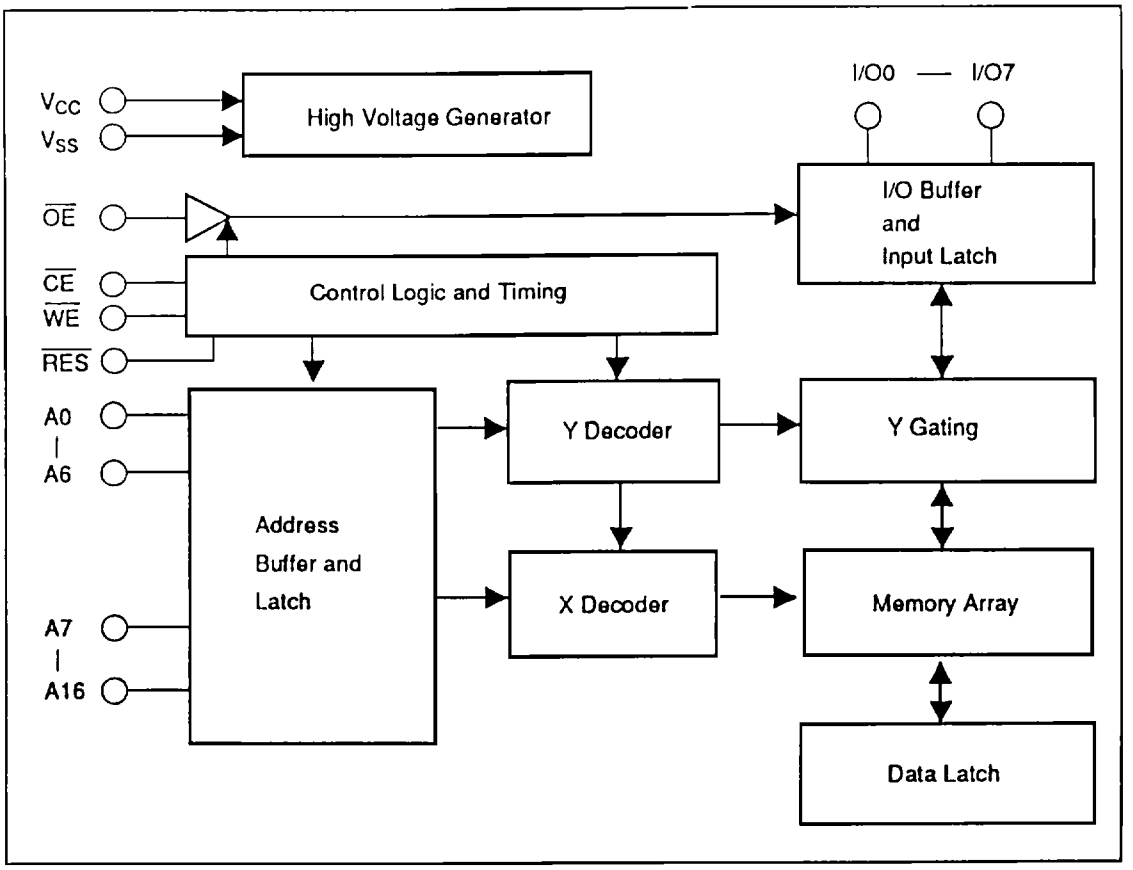
(Top View)

Pin Description

Pin name	Function
A0-A16	Address
I/O0-I/O7	Input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable

Pin name	Function
$\overline{WE}$	Write enable
V_{CC}	Power (+5 V)
V_{SS}	Ground
RDY/$\overline{Busy}$	Ready busy
$\overline{RES}$	Reset

Block Diagram



Mode Selection

Pin Mode	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{WE}$ (29)	$\overline{RES}$ (30)	RDY/$\overline{Busy}$ (1)	I/O (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	High-Z	Dout
Standby	V_{IH}	X	X	X	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z→V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_{IH}	High-Z	High-Z
Write Inhibit	X	X	V_{IH}	X	—	—
	X	V_{IL}	X	X	—	—
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{OL}	Data out (I/O7)
Program reset	X	X	X	V_H	High-Z	High-Z

Note: 1. X = Don't care

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage *1	V_{CC}	–0.6 to +7.0	V
Input voltage *1	Vin	–0.5*2 to +7.0	V
Operationg temperature range *3	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. With respect to V_{SS}
2. Vin min = –3.0 V for pulse width ≤ 50 ns

Recommended DC Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	5.5	V
Input voltage	V_{IL}	–0.3	—	0.8	V
	V_{IH}	1.9	—	V_{CC} + 0.3	V
	V_H	V_{CC} – 1	—	V_{CC} + 0.3	V
Operating temperature	Topr	0	—	70	°C

DC Characteristics (Ta=0 to +70°C, V_{CC} = 2.7 to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	V_{CC} = 3.6 V, Vin = 3.6 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 3.6 V, Vout = 3.6/0.4 V
VCC current (standby)	I_{CC1}	—	—	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	1	mA	$\overline{CE}$ = V_{IH}
VCC current (active)	I_{CC3}	—	—	10	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs
		—	—	25	mA	Iout = 0mA, Duty = 100%, Cycle = 200 ns
Input low voltage	V_{IL}	–0.3*1	—	0.8	V	
Input high voltage	V_{IH}	1.9*2	—	V_{CC} + 0.3	V	
	V_H	V_{CC}–1	—	V_{CC} + 0.3	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	V_{CC} x 0.8	—	—	V	I_{OH} = –400 µA

Note: 1. V_{IL} min = –1.0 V for pulse width ≤ 50 ns
2. V_{IH} min = 2.2 V for V_{CC} = 3.6 to 5.5 V.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	—	12	pF	Vout = 0 V

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 2.7 to 5.5 V)

Test Conditions

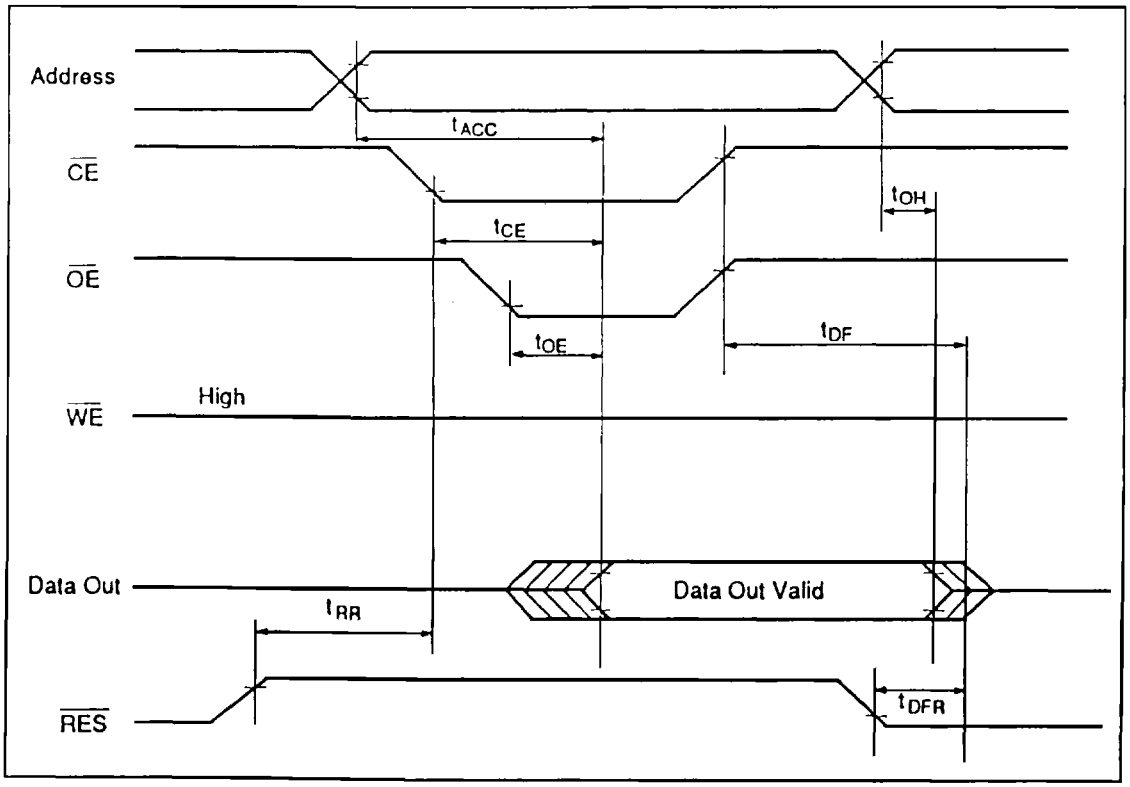
- Input pulse levels : 0.4 V to 2.4 V
- Input rise and fall time : ≤ 20 ns
- Output load : 1TTL Gate +100 pF
- Reference levels for measuring timing : 0.8 V, 1.8 V

Read Cycle

Parameter	Symbol	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	200	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	90	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ high to output float*1	t_{DF}	0	70	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to output delay	t_{RR}	0	450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform

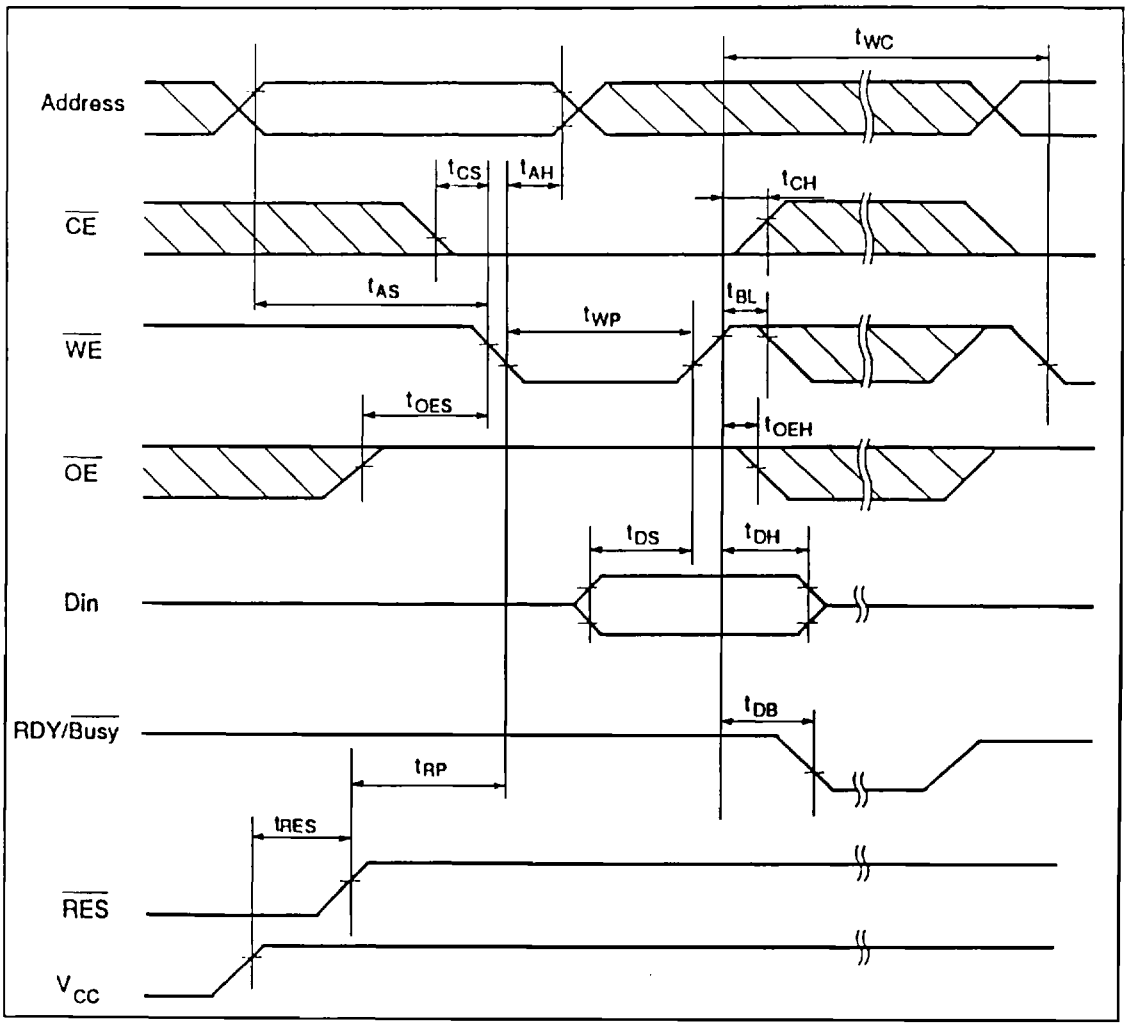


Byte Erase and Byte Write Cycle ($\overline{WE}$ Controlled)

Parameter	Symbol	Min*1	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns	
Write pulse width	t_{WP}	250	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Write cycle time	t_{WC}	10	—	—	ms	
Byte load window	t_{BL}	100	—	—	µs	
Time to device busy	t_{DB}	120	—	—	ns	
$\overline{RES}$ to write setup time	t_{RP}	100	—	—	µs	
V_{CC} to $\overline{RES}$ setup time	t_{RES}	1	—	—	µs	

Note: 1. Use this device in longer cycle than this value.

Byte Erase and Byte Write TimingWaveform(1) ($\overline{WE}$ Controlled)

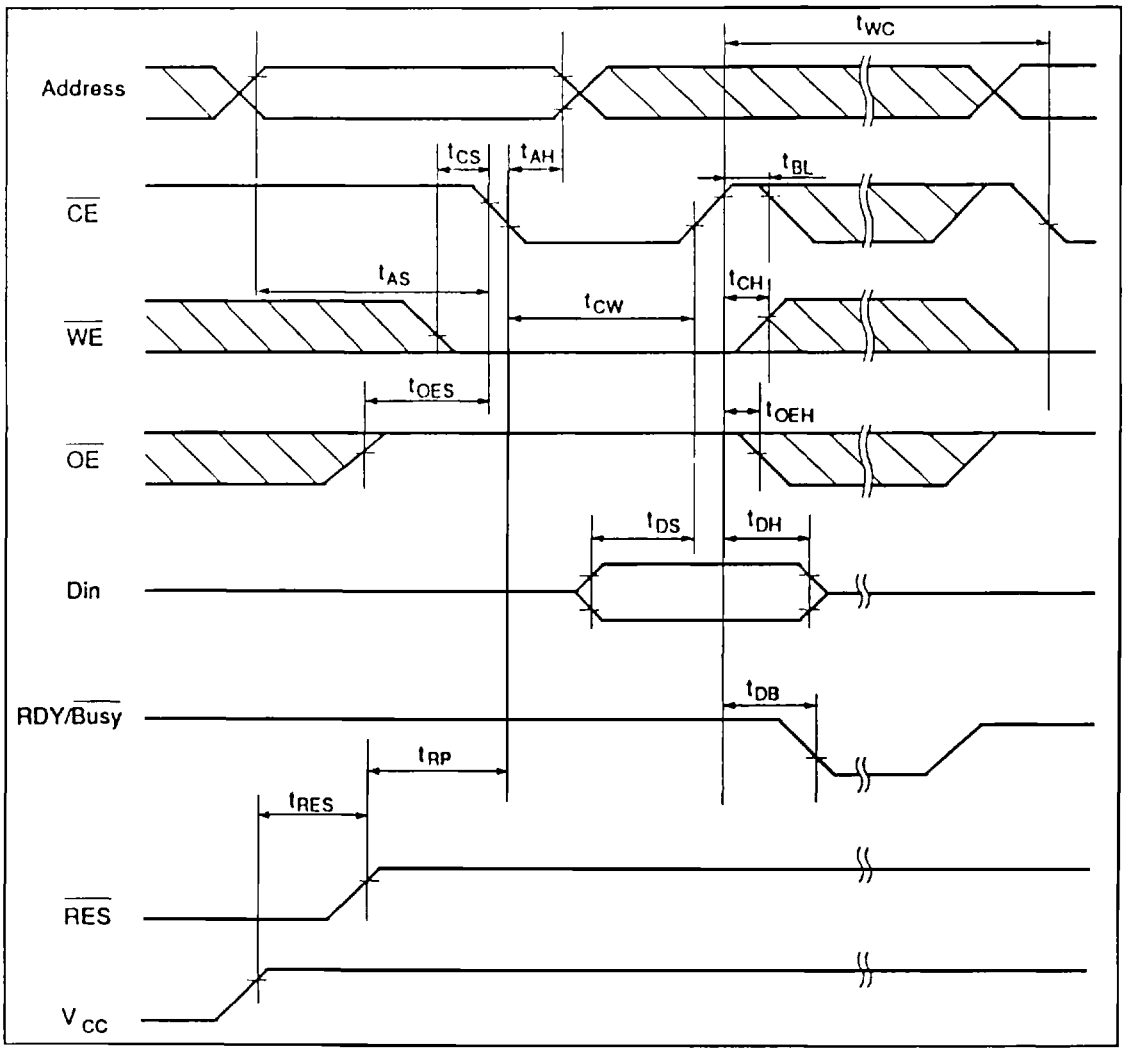


Byte Erase and Byte Write Cycle ($\overline{CE}$ Controlled)

Parameter	Symbol	Min*1	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns	
Write pulse width	t_{CW}	250	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns	
$\overline{CE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Write cycle time	t_{WC}	15	—	—	ms	
Byte load window	t_{BL}	100	—	—	µs	
Time to device busy	t_{DB}	120	—	—	ns	
$\overline{RES}$ to write setup time	t_{RP}	100	—	—	µs	
V_{CC} to $\overline{RES}$ setup time	t_{RES}	1	—	—	µs	

Note: 1. Use this device in longer cycle than this value.

Byte Erase and Byte Write Timing Waveform (2) ($\overline{CE}$ Controlled)

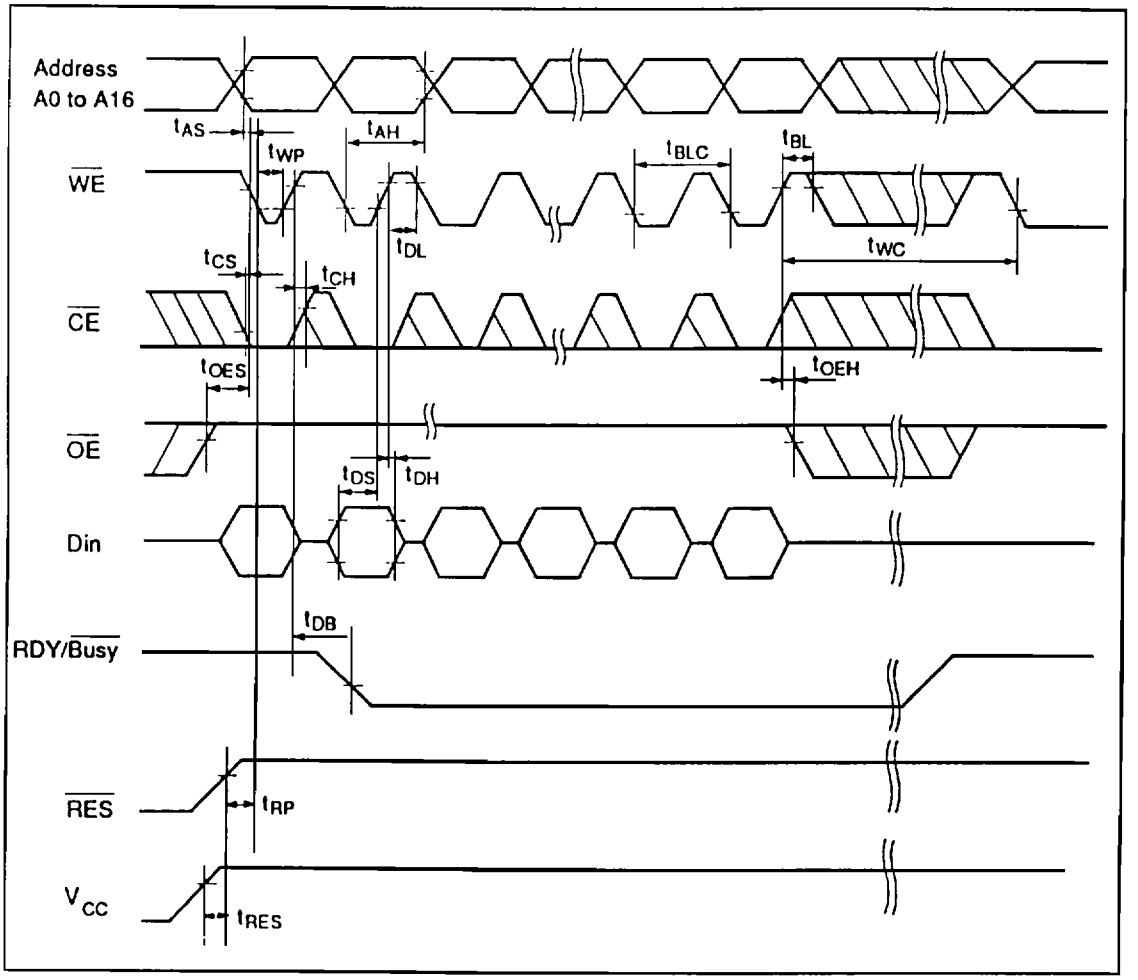


Page Erase and Page Write Cycle ($\overline{WE}$ Controlled)

Parameter	Symbol	Min*1	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns	
Write pulse width	t_{WP}	250	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data latch time	t_{DL}	300	—	—	ns	
Write cycle time	t_{WC}	15	—	—	ms	
Byte load window	t_{BL}	100	—	—	µs	
Byte load cycle	t_{BLC}	0.55	—	30	µs	
Time to device busy	t_{DB}	120	—	—	ns	
$\overline{RES}$ to write setup time	t_{RP}	100	—	—	µs	
V_{CC} to $\overline{RES}$ setup time	t_{RES}	1	—	—	µs	

Note: 1. Use this device in longer cycle than this value.

Page Erase and Page Write Timing Waveform (1) ($\overline{WE}$ Controlled)

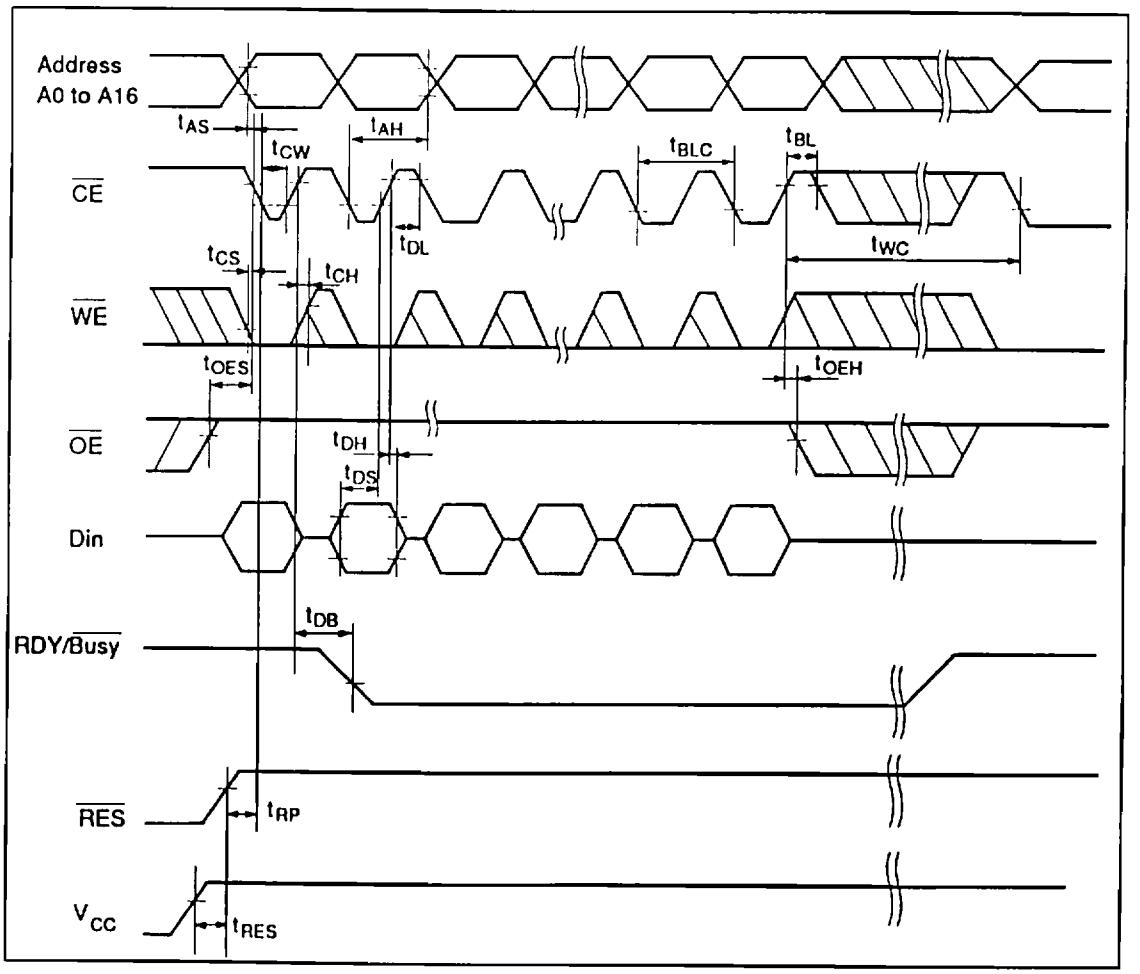


Page Erase and Page Write Cycle ($\overline{CE}$ Controlled)

Parameter	Symbol	Min*1	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns	
Write pulse width	t_{CW}	250	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data latch time	t_{DL}	300	—	—	ns	
Write cycle time	t_{WC}	15	—	—	ms	
Byte load window	t_{BL}	100	—	—	µs	
Byte load cycle	t_{BLC}	0.55	—	30	µs	
Time to device busy	t_{DB}	120	—	—	ns	
$\overline{RES}$ to write setup time	t_{RP}	100	—	—	µs	
V_{CC} to $\overline{RES}$ setup time	t_{RES}	1	—	—	µs	

Note: 1. Use this device in longer cycle than this value.

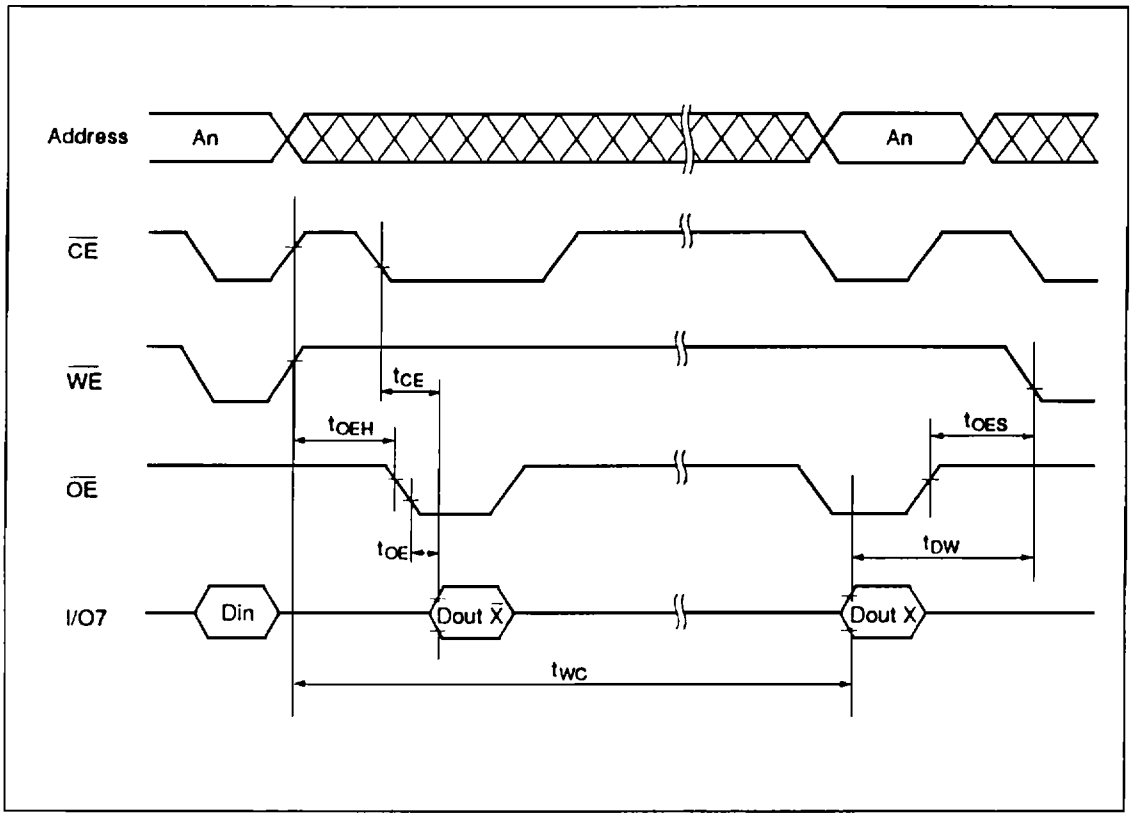
Page Erase and Page Write Timing Waveform (2) ($\overline{CE}$ Controlled)



$\overline{\text{Data}}$ Polling Cycle

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
$\overline{\text{OE}}$ hold time	t_{OEH}	0	—	—	ns	
$\overline{\text{OE}}$ to write setup time	t_{OES}	0	—	—	ns	
Write start time	t_{DW}	150	—	—	ns	
Write cycle time	t_{WC}	—	—	15	ms	

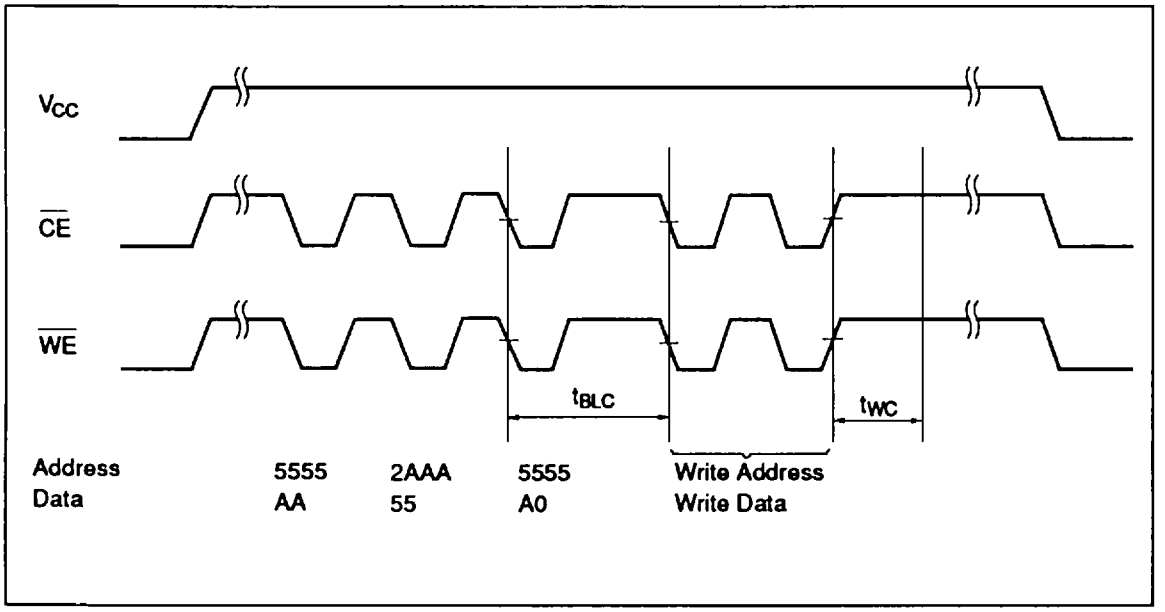
$\overline{\text{Data}}$ Polling Timing Waveform



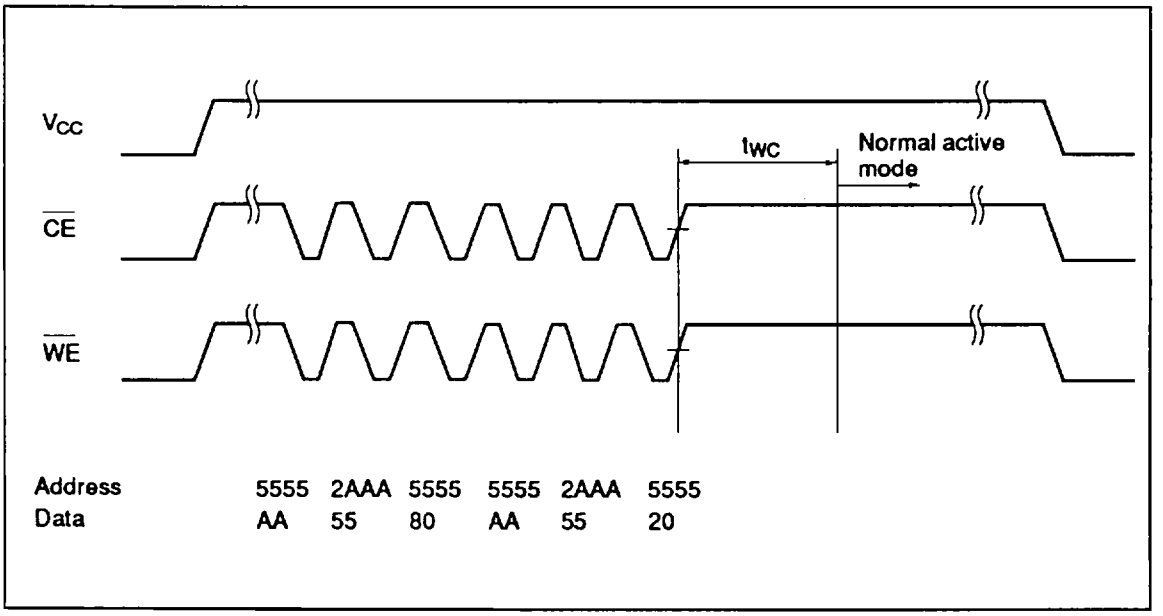
Software Data Protection Cycle

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Byte load cycle time	t_{BLC}	0.35	—	30	µs	
Write cycle time	t_{WC}	10	—	—	ms	

Software Data Protection Timing Waveform (1) (in protection mode)



Software Data Protection Timing Waveform (2) (in non-protection mode)



Mode Description

Device Identifier Mode

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of Flash Memory. By this mode, the device will be automatically matched its own corresponding erase and programming algorithm, using programming equipment.

HN58V1001 Series IdentifierCode

	Pins	A0	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	
	HN58V1001P/FP	(12)	(21)	(20)	(19)	(18)	(17)	(15)	(14)	(13)	
Identifier	HN58V1001T/R	(20)	(29)	(28)	(27)	(26)	(25)	(23)	(22)	(21)	Hex Data
Manufacturer code		V_{IL}	0	0	0	0	0	1	1	1	07
Device code		V_{IH}	0	1	0	1	1	0	0	0	58

Notes: 1. Device identifier code can be read out by applying 12.0 V ± 0.5 V to A9.
2. A1 to A8,A10 to A16, and $\overline{CE}$,$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}
3. V_{CC}=2.7 to 5.5 V

Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 128 bytes of data to be written into the EEPROM in a single cycle, and allows the undefined data within 128 bytes to be written corresponding to the undefined address (A0 to A6). Loading the first byte of data, the data load window of 30 µs opens for the second. In the same manner each additional byte of data can be loaded within 30 µs. In case $\overline{CE}$ and $\overline{WE}$ are kept high for 100 µs after data input, EEPROM enters erase and write mode automatically and only the input data are written into the EEPROM. In page mode the data can be written and accessed 10^5 times per page, and in byte mode 10^4 times per byte.

$\overline{Data}$ Polling

Data polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operartion.

Write Protection

(1) Noise protection: Noise on a write cycle will not act as a triger with a $\overline{WE}$ pulse of less than 20 ns.
(2) Write inhibit: Holding $\overline{OE}$ low, $\overline{WE}$ high, or $\overline{CE}$ high, inhibits a write cycle during power on/off.

$\overline{WE}$ $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

Write/Erase Endurance and Data Retention Time

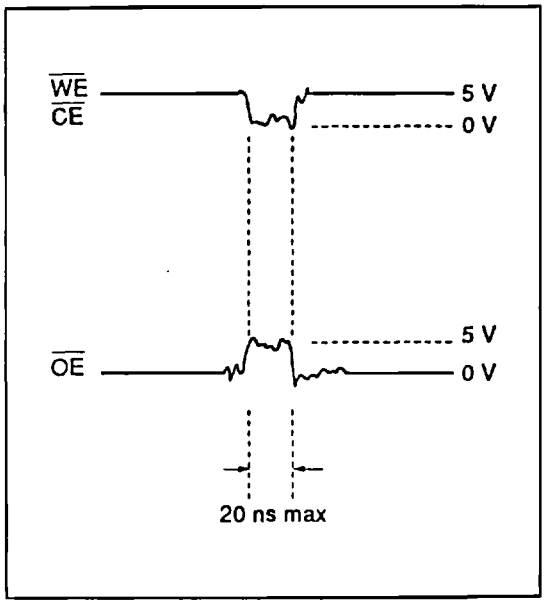
The endurance with page programming is 10^5 cycles (1% cummulative failure rate) and the data retention time is more than 10 years when a device is programmed less than 10^4 cycles.

Data Protection

To protect the data during operation and power on/off, the HN58C1001 has the internal functions described below.

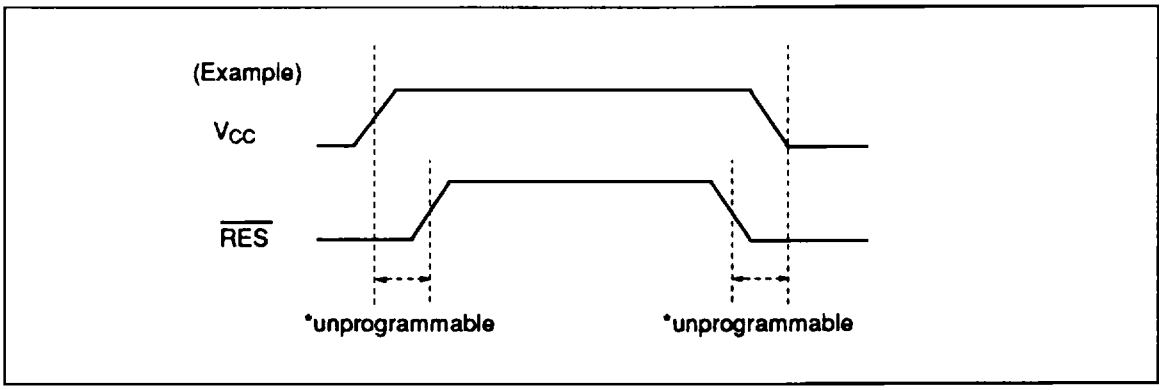
1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.
To prevent this phenomenon, the HN58C1001 has a noise cancelation function that cuts noise if its width is 20 ns or less in programming mode.
Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data protection at V_{CC} on/off

When $\overline{RES}$ is low, the EEPROM cannot be erased and programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during programming because it doesn't provide a latch function.



When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable, standby or readout state by using a CPU reset signal to RES\ pin.
In addition, when RES\ is kept high at V_{CC} on/off timing, the input level of control pins (CE\, OE\, WE\) must be held as CE\ =V_{CC} or OE\ =Low or WE\ =V_{CC} level.

3. Software data protection

To prevent unintentional programming caused by noise generated by external circuits, HN58V1001 has the software data protection function. In software data protection mode, 3 bytes of data must be input before write data as follows. And these bytes can switch the non-protection mode to the protection mode.

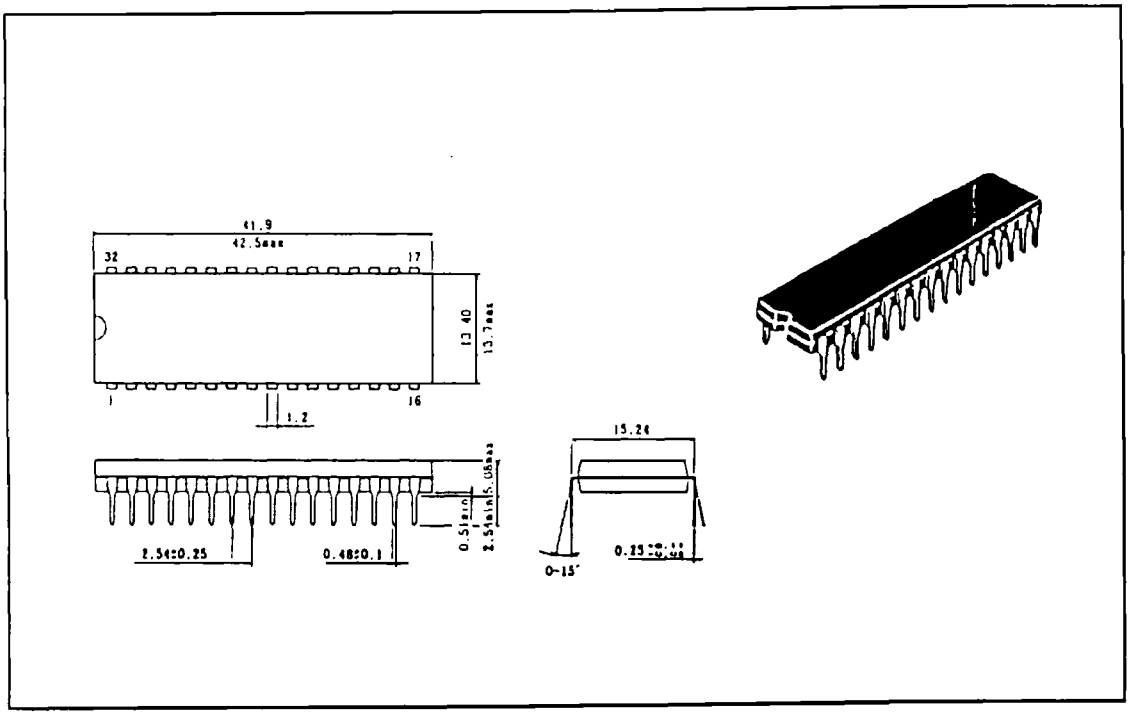
Address	Data	
5555	AA	
2AAA	55	
5555	A0	
Write address	Write data	} Normal data input

Software data protection mode can be canceled by inputting the following 6 bytes. After that, HN58V1001 turns to the non-protection mode and can write data normally. But when the data is input in the canceling cycle, the data cannot be written.

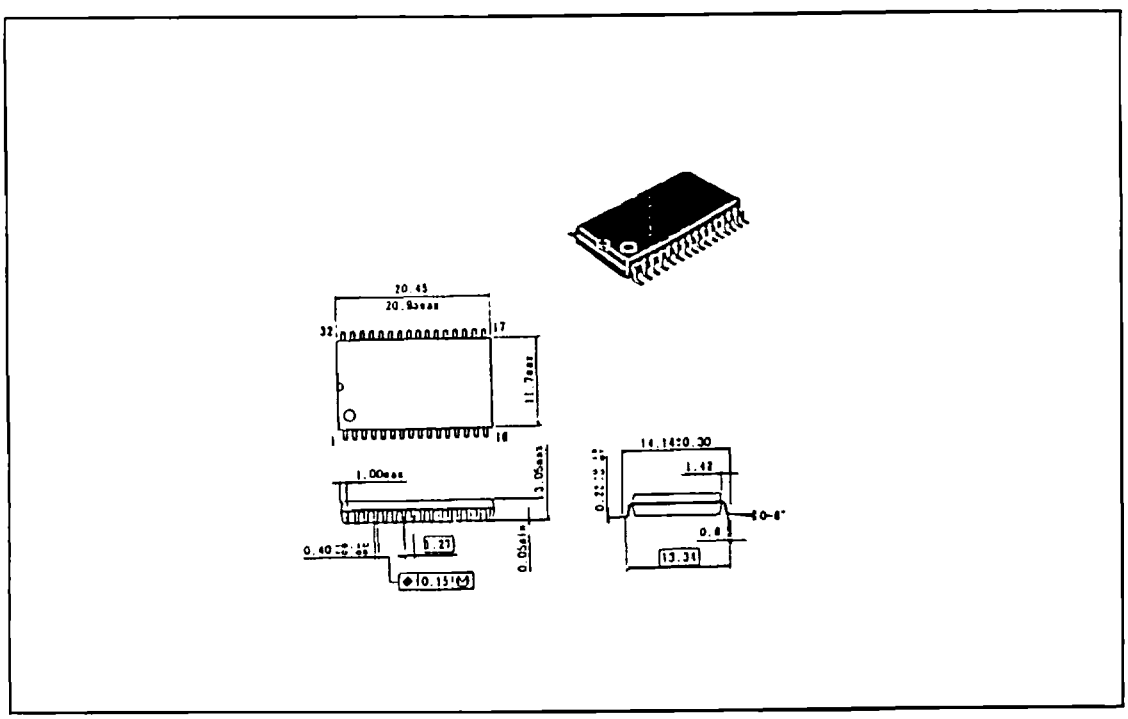
Address	Data
5555	AA
2AAA	55
5555	80
5555	AA
2AAA	55
5555	20

Package Dimensions

HN58V1001P Series (DP-32) **Unit : mm**

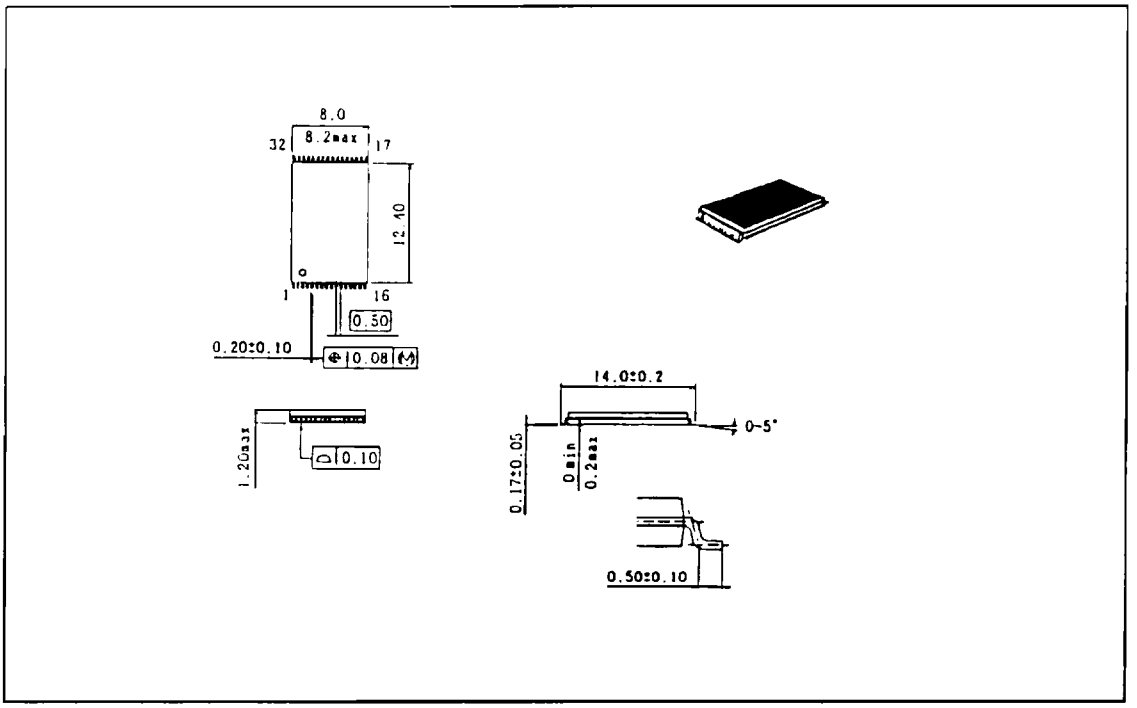


HN58V1001FP Series (FP-32D)

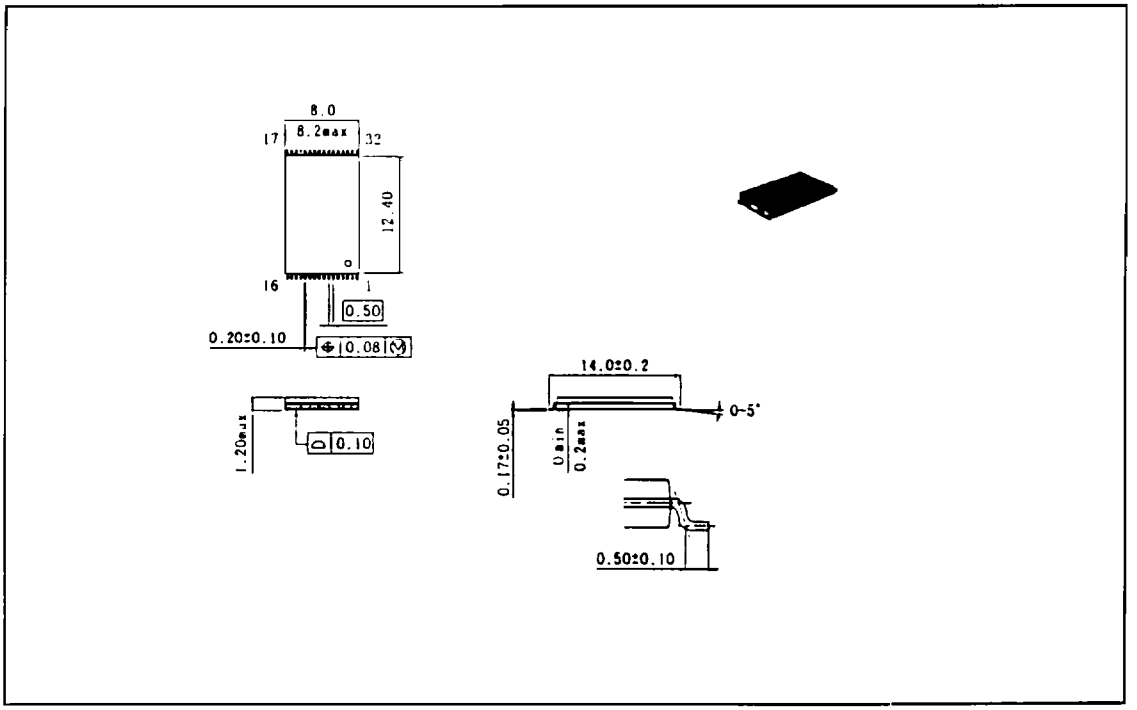


Package Dimensions (Cont)

HN58V1001T Series (TFP-32DA) **Unit : mm**



HN58V1001R Series (TFP-32DAR)



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