CD54HC4053/3A
CD54HCT4053/3A

Switching Speed (Limits with black dots (•) are tested 100%.)

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{EE}	V_{CC}	25°C				-55°C to +125°C				UNITS
				HC		HCT		54HC		54HCT		
			V	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay		0	2	—	60	—	—	—	90	—	—	
Switch In to Out	t_{PLH}	0	4.5	—	12	—	12	—	18	—	18	
	t_{PHL}	0	6	—	10	—	—	—	15	—	—	
		-4.5	4.5	—	8	—	8	—	12	—	12	
Maximum Switch		0	2	—	210	—	—	—	315	—	—	
Turn "Off" Delay	t_{PHZ}	0	4.5	—	42•	—	44•	—	63•	—	66•	
from S or $\overline{E}$ to	t_{PLZ}	0	6	—	36	—	—	—	54	—	—	ns
Switch Output		-4.5	4.5	—	29	—	31	—	44	—	47	
Maximum Switch		0	2	—	220	—	—	—	330	—	—	
Turn "On" Delay	t_{PZL}	0	4.5	—	44•	—	48•	—	66•	—	72•	
from S or E to	t_{PZH}	0	6	—	37	—	—	—	56	—	—	
Switch Output		-4.5	4.5	—	31	—	34	—	47	—	51	
Input Capacitance	C_I	—	—	—	10	—	10	—	10	—	10	pF

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT4053	4,14,15	1-3,5,6,7*,8*,9-13	16	4,14,15	7*,8*	1-3,5,6,9-13,16
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR**	
					50 kHz	**25 kHz**
CD54HC/HCT4053	—	1,5,6,7*,8*,12	4,14,15	2,3,13,16	9-11	—

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.
Connect pins marked (*) without using a resistor.

Programmable Divide-by-"N" Counter

CD54HC4059/3A
CD54HCT4059/3A

The RCA CD54HC4059 and CD54HCT4059 are high-speed silicon-gate devices that are pin compatible with the CD4059B devices of the CD4000B series. These devices are divide-by-N down-counters that can be programmed to divide an input frequency by any number "N" from 3 to 15,999. The output signal is a pulse one clock cycle wide occurring at a rate equal to the input frequency divided by N. The down-counter is preset by means of 16 jam inputs.

The three mode-select inputs Ka, Kb and Kc determine the modulus ("divide-by" number) of the first and last counting sections. Every time the first (fastest) counting section goes through one cycle, it reduces by one the number that has been preset (jammed) into the three decades of the intermediate counting section and into the last counting section, which consists of flip-flops that are not needed for operating the first counting section. For example, in the ÷ 2 mode, only one flip-flop is needed in the first counting section. Therefore, the last counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands. If ÷ 10 is desired for the first section, Ka and J4 are used to preset the first counting section and there is no last counting section. The intermediate counting section consists of three cascaded BCD decade (÷ 19) counters presettable by means of jam inputs J5 through J16.

The mode-select inputs permit frequency-synthesizer channel separations of 10, 12.5, 20, 25, or 50 parts. These inputs set the maximum value of N at 9999 (when the first counting section divides by 5 or 10) or 15,999 (when the first counting section divides by 8, 4, or 2).

The three decades of the intermediate counter can be preset to a binary 15 instead of a binary 9, while their place values are still 1, 10, and 100, multipled by the number of the ÷ N mode. For example, in the ÷ 8 mode, the number from which counting down begins can be preset to:

3rd decade: 1500
2nd decade: 150
1st decade: 15
Last counting section 1000

CD54HC4059/3A
CD54HCT4059/3A

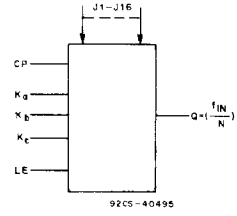
The total of these numbers (2665) times 8 equals 21,320. The first counting section can be preset to 7. Therefore, 21,327 is the maximum possible count in the ÷ 8 mode.

Control inputs Kb and Kc can be used to initiate and lock the counter in the "master preset" state. In this condition, the flip-flops in the counter are preset in accordance with the jam inputs and the counter remains in that state as long as Kb and Kc both remain low. The counter begins to count down from the preset state when a counting mode other than the master preset mode is selected.

The counter should always be put in the master preset mode before the ÷ 5 mode is selected. Whenever the master preset mode is used, control signals Kb = "low" and Kc = "low" must be applied for at least three full clock pulses.

After the master preset mode inputs have been changed to one of the ÷ modes, the next positive-going clock transition changes an internal flip-flop so that the countdown can begin at the second positive-going clock transition. Thus, after an MP (Master Preset) mode, there is always one extra count before the output goes high. If the master preset mode is started two clock cycles or less before an output pulse, the output pulse will appear at the time due. If the master preset mode is not used, the counter jumps back to the "jam" count when the output pulse appears.

A "high" on the latch enable input will cause the counter output to remain high once an output pulse occurs, and to remain in the high state until the latch input returns to "low". If the latch enable is "low", the output pulse will remain high for only one cycle of the clock-input signal.



FUNCTIONAL DIAGRAM

Package Specifications

See Section 11, Fig. 15

Static Electrical Characteristics (Limits with black dots (•) are tested 100%)

CHARACTERISTICS		TEST CONDITIONS HC/HCT V_{DD}	V_O	I_O	V_{CC} or GND	V_{IN} HC V_{IL} or V_{IH}	V_{IN} HCT V_{IL} or V_{IH}	LIMITS MIN.	LIMITS MAX.	UNITS
Quiescent	25°C	6	—	—	6, 0	—	—	—	8•	μA
Device Current I_{CC}	-55°C / +125°C	6	—	—	6, 0	—	—	—	160•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

HCT INPUT LOADING TABLE

INPUT	UNIT LOAD*
All J Inputs	0.5
CP	0.65
LE	1.65
Ka	1
Kb	1.5
Kc	0.85

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54HC4059/3A
CD54HCT4059/3A

Switching Speed (Limits with black dots (•) are tested 100%.)

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_n, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_{CC} V	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Propagation Delay CP to Q	t_{PLH}	2	—	200	—	—	—	300	—	—	ns
		4.5	—	40•	—	46•	—	60•	—	69•	
		6	—	34	—	—	—	51	—	—	
	t_{PHL}	2	—	175	—	—	—	265	—	—	
LE to Q		4.5	—	35	—	46	—	53	—	69	
		6	—	30	—	—	—	45	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	110	—	—	
		4.5	—	15	—	15	—	22	—	22	
		6	—	13	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	pF

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I OPEN	GROUND	V_{CC} (6V)	STATIC BURN-IN II OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT4059	23	1-22	24	23	12	1-11,13-22,24
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR 50 kHz**	**25 kHz**
CD54HC/HCT4059	—	2,4,5,8,9,11,12, 16,17,20,21	23	3,6,7,10, 13,14,15,18, 19,22,24	1	—

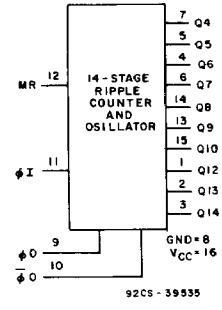
NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

CD54HC4060/3A
CD54HCT4060/3A

14-Stage Binary Ripple Counter w/Oscillator

The RCA CD54HC4060 and CD54HCT4060 each consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A master reset input is provided which resets the counter to the all-0's state and disables the oscillator. A high level on the MR line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of ϕ_I (and ϕ_O). All inputs and outputs are buffered. Schmitt trigger action on the input-pulse line permits unlimited rise and fall times.

In order to achieve a symmetrical waveform in the oscillator section, the HCT4060 input pulse switchpoints are the same as in the HC4060; only the MR input in the HCT4060 has TTL switching levels.



FUNCTIONAL DIAGRAM

Package Specifications

See Section 11, Fig. 11