DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

MC-422000A32

2 M-WORD BY 32-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-422000A32 is a 2,097,152 words by 32 bits dynamic RAM module on which 16 pieces of 4 M DRAM: μPD424400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2,097,152 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-422000A32-60	60 ns	110 ns	4,290 mW	88 mW (CMOS level input)
MC-422000A32-70	70 ns	130 ns	3,850 mW	
MC-422000A32-80	80 ns	160 ns	3,850 mW	
MC-422000A32-10	100 ns	190 ns	3,850 mW	

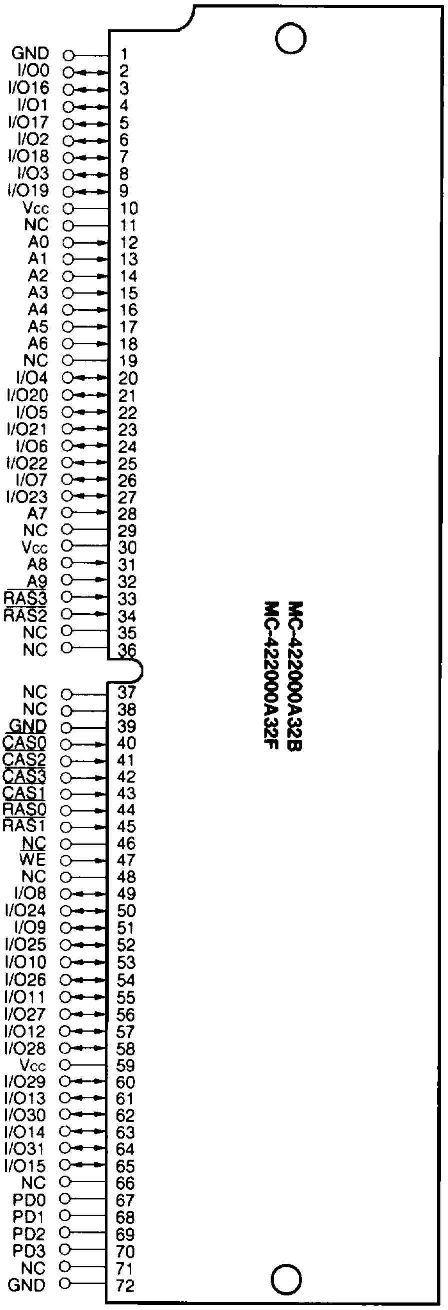
- 1,024 refresh cycles/16 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000A32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	16 pieces of μPD424400LA (300 mil SOJ) [Double side]
MC-422000A32B-70	70 ns		
MC-422000A32B-80	80 ns		
MC-422000A32B-10	100 ns		
MC-422000A32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-422000A32F-70	70 ns		
MC-422000A32F-80	80 ns		
MC-422000A32F-10	100 ns		

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)

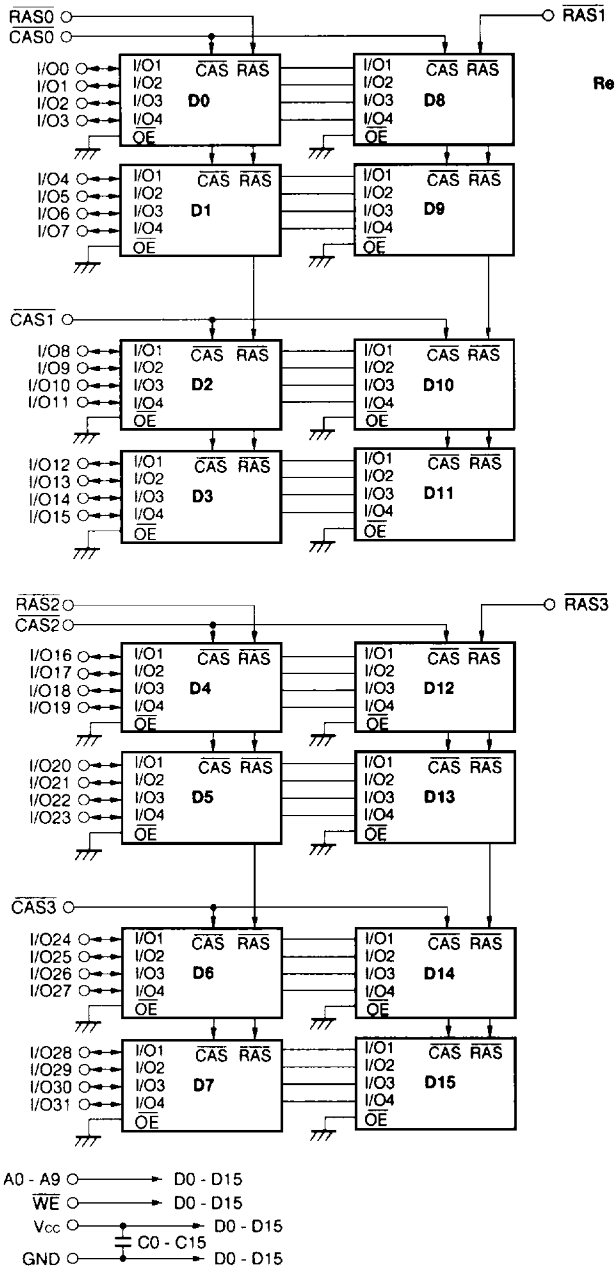


A0 - A9	:	Address Inputs
I/O0 - I/O31	:	Data Inputs/Outputs
$\overline{\text{CAS0}}$ - $\overline{\text{CAS3}}$	:	Column Address Strobe
$\overline{\text{RAS0}}$ - $\overline{\text{RAS3}}$	:	Row Address Strobe
$\overline{\text{WE}}$	:	Write Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time			
		60 ns	70 ns	80 ns	100 ns
PD0	67	NC	NC	NC	NC
PD1	68	NC	NC	NC	NC
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

Block Diagram



Remark D0 - D15: μPD424400

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		–1.0 to +7.0	V
Supply voltage	V_{CC}		–1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		16	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		–1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			121	pF
	C_{I2}	$\overline{\text{WE}}$			137	
	C_{I3}	$\overline{\text{RAS0}}$ - $\overline{\text{RAS3}}$			48	
	C_{I4}	$\overline{\text{CAS0}}$ - $\overline{\text{CAS3}}$			48	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			29	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ Cycling $t_{RC} = t_{RC\,(MIN.)}$ $I_O = 0$ mA	$t_{RAC} = 60$ ns		780	mA	3, 4, 7
			$t_{RAC} = 70$ ns		700		
			$t_{RAC} = 80$ ns		700		
			$t_{RAC} = 100$ ns		700		
Standby current	I_{CC2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ $\geq V_{IH\,(MIN.)}$	$I_O = 0$ mA		32	mA	
		$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ $\geq V_{CC} - 0.2$ V	$I_O = 0$ mA		16		
$\overline{\text{RAS}}$ only refresh current	I_{CC3}	$\overline{\text{RAS}}$ Cycling $\overline{\text{CAS}}$ $\geq V_{IH\,(MIN.)}$ $t_{RC} = t_{RC\,(MIN.)}$ $I_O = 0$ mA	$t_{RAC} = 60$ ns		780	mA	3, 4, 5, 7
			$t_{RAC} = 70$ ns		700		
			$t_{RAC} = 80$ ns		700		
			$t_{RAC} = 100$ ns		700		
Operating current (Fast page mode)	I_{CC4}	$\overline{\text{RAS}}$ $\leq V_{IL\,(MAX.)}$, $\overline{\text{CAS}}$ Cycling $t_{PC} = t_{PC\,(MIN.)}$ $I_O = 0$ mA	$t_{RAC} = 60$ ns		620	mA	3, 4, 6
			$t_{RAC} = 70$ ns		540		
			$t_{RAC} = 80$ ns		540		
			$t_{RAC} = 100$ ns		540		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I_{CC5}	$\overline{\text{RAS}}$ Cycling $t_{RC} = t_{RC\,(MIN.)}$ $I_O = 0$ mA	$t_{RAC} = 60$ ns		780	mA	3, 4
			$t_{RAC} = 70$ ns		700		
			$t_{RAC} = 80$ ns		700		
			$t_{RAC} = 100$ ns		700		
Input leakage current	$I_{I\,(L)}$	$V_I = 0$ to 5.5 V All other pins not under test = 0 V		−10	+10	μA	
Output leakage current	$I_{O\,(L)}$	$V_O = 0$ to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage	V_{OH}	$I_O = -5.0$ mA		2.4		V	
Low level output voltage	V_{OL}	$I_O = +4.2$ mA			0.4	V	

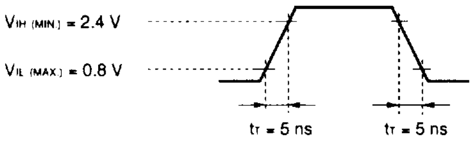
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		t_{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		160		190		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		60		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		20		20		25	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40		50	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45		55	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	17	50	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	0	25	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		70		80		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	100	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		20		20		25		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	25	75	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		10		10		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	10		10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		55		ns	
Row Address Setup Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		20		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		50		ns	
Read Command Setup Time	t_{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		10		10		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	15		15		15		20		ns	15
Data-in Setup Time	t_{DS}	0		0		0		0		ns	16
Data-in Hold Time	t_{DH}	15		15		15		20		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		15		20		ns	
$\overline{WE}$ Setup Time	t_{WSR}	0		0		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	10		10		15		20		ns	
Refresh Time	t_{REF}		16		16		16		16	ms	

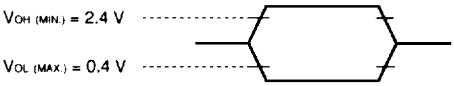
Notes

1. All voltages are referenced to GND.
2. After power up ($V_{CC} \geq V_{CC\,(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\,(MAX.)}$ and $\overline{CAS} \geq V_{IH\,(MIN.)}$.
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification

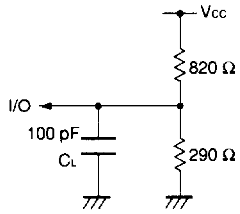


10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\,(MAX.)}$ and $t_{RCD} \leq t_{RCD\,(MAX.)}$	$t_{RAC\,(MAX.)}$	$t_{RAC\,(MAX.)}$
$t_{RAD} > t_{RAD\,(MAX.)}$ and $t_{RCD} \leq t_{RCD\,(MAX.)}$	$t_{AA\,(MAX.)}$	$t_{RAD} + t_{AA\,(MAX.)}$
$t_{RCD} > t_{RCD\,(MAX.)}$	$t_{CAC\,(MAX.)}$	$t_{RCD} + t_{CAC\,(MAX.)}$

$t_{RAD\,(MAX.)}$ and $t_{RCD\,(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\,(MAX.)}$ and $t_{RCD} \geq t_{RCD\,(MAX.)}$ will not cause any operation problems.

11. Output load condition



12. $t_{OFF\,(MAX.)}$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.

13. $t_{CRP\,(MIN.)}$ requirements should be applied to $\overline{RAS}$/$\overline{CAS}$ cycles.

14. Either $t_{RCH\,(MIN.)}$ or $t_{RRH\,(MIN.)}$ should be met in read cycles.

15. In early write cycles, $t_{WCH\,(MIN.)}$ should be met.

16. $t_{DS\,(MIN.)}$ and $t_{DH\,(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.

17. If $t_{WCS} \geq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

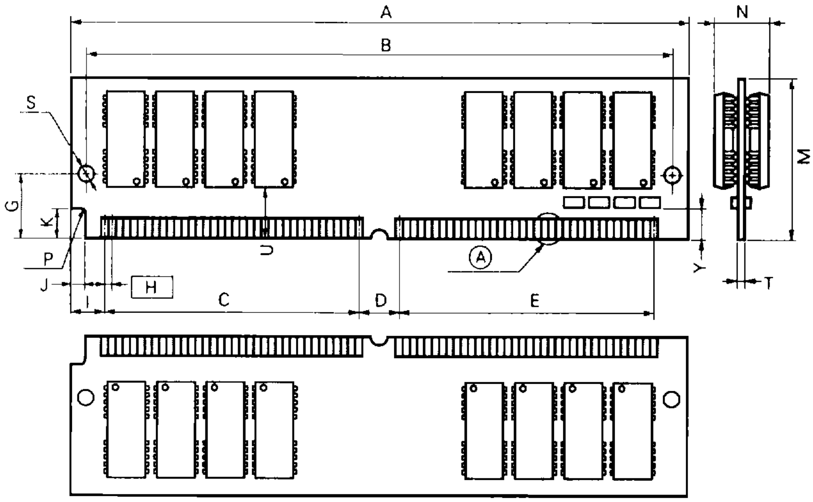
Timing Chart

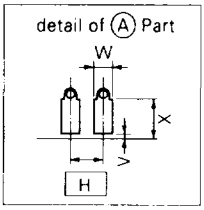
Please refer to Timing Chart 10, page 479.

Package Drawing

[MC-422000A32B, 422000A32F]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





M72B-50A22-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R 2.0	R 0.079
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	6.5 MIN.	0.255 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.75 MIN.	0.147 MIN.