FEATURES

- Industry Standard Pinouts
- 50, 60, 70 or 80ns RAS Access Time (tRAC)
- Static Column Mode or Enhanced Page Mode
- RAS-Only Refresh, Hidden Refresh and CAS-before-RAS Refresh
- Battery Backup Mode with Automatic Refresh
- Test Mode
- Commercial Voltage/Temperature Range
  - 4.5 - 5.5 Volts Vcc
  - 0 - 70°C Operating Temperature
- Packages - 20 Pin 300mil PDIP
  - 26 Pin SOJ
  - 20 Pin ZIP

See pages 11 and 12 for Package and Pinout details

AAA4M200 SERIES

Part Number	t_{RAC} [1]	t_{CAC} [2]	t_{AA} [3] (t_{CAA})	t_{RC} [4]	t_{PC} [5]	Icc [6] (Standby)	Icc [7] (Battery Backup)	Icc [8] (Active)	Refresh [9] (t_{REF})
4M x 1 AND 1M x 4 - STATIC COLUMN AND ENHANCED PAGE MODE									
AAA4M20XX-05	50ns	13ns	25ns	100ns	30ns	1mA	200µA	100mA	16ms
AAA4M20XX-06	60ns	15ns	30ns	110ns	35ns	1mA	200µA	90mA	16ms
AAA4M20XX-07	70ns	20ns	35ns	130ns	40ns	1mA	200µA	80mA	16ms
AAA4M20XX-08	80ns	20ns	40ns	150ns	45ns	1mA	200µA	70mA	16ms

NOTES:

1. tRAC defines maximum RAS Access Time.
2. tCAC defines maximum CAS Access Time.
3. tAA (alternatively tCAA) defines maximum Column Address Access Time.
4. tRC defines minimum Read or Write Cycle Time.
5. tPC defines minimum Enhanced Page Mode or Static Column Mode Cycle Time.
6. Icc (Standby) defines maximum Vcc supply current with inputs at CMOS levels and RAS, CAS ≥ Vcc - 0.2V.
7. Icc (Battery Backup) defines maximum Vcc supply current while in Battery Backup Mode with CAS ≤ V_{IL}, other inputs at CMOS levels. Refer to Data Sheet for details.
8. Icc (Active) defines maximum Vcc supply current under normal operation with tRC= tRC min., 4.5 ≤ Vcc ≤ 5.5 volts and 0°C ≤ Ta ≤ 70°C.
9. tREF defines the Refresh Interval during which all internal rows (1024) must be refreshed when not in Battery Backup Mode.

ORDERING INFORMATION:

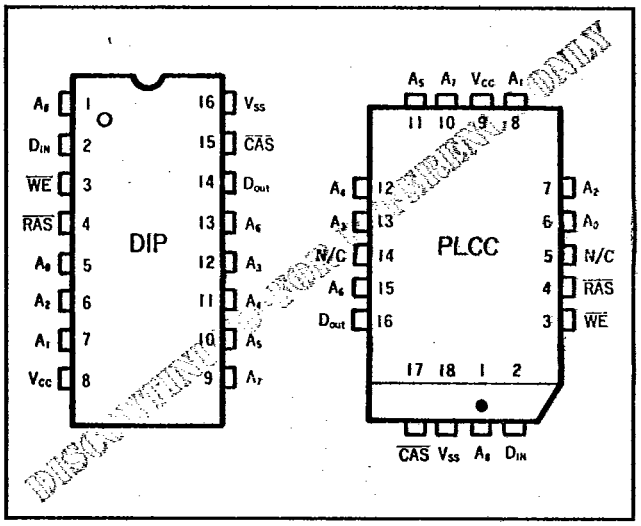
AAA4M20XX - XX

- SPEED
  - 05: 50ns tRAC
  - 06: 60ns tRAC
  - 07: 70ns tRAC
  - 08: 80ns tRAC
- PACKAGE
  - J: SOJ
  - P: PDIP
  - Z: ZIP
  - S: TSOP (I) Normal Bend
  - Q: TSOP (I) Reverse Bend
  - T: TSOP (II) Normal Bend
  - R: TSOP (II) Reverse Bend
- ORGANIZATION/MODE
  - 0: 4M x 1 Enhanced Page Mode
  - 1: 4M x 1 Static Column Mode
  - 4: 1M x 4 Enhanced Page Mode
  - 5: 1M x 4 Static Column Mode
- WRITE MODE
  - 0: No Write Per Bit
  - 1: Write Per Bit (To be announced)

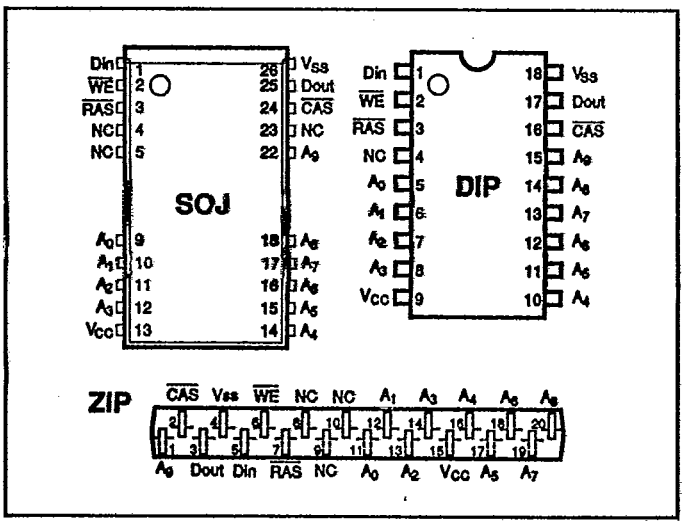
PACKAGE AND PINOUT DETAILS

T-91-20

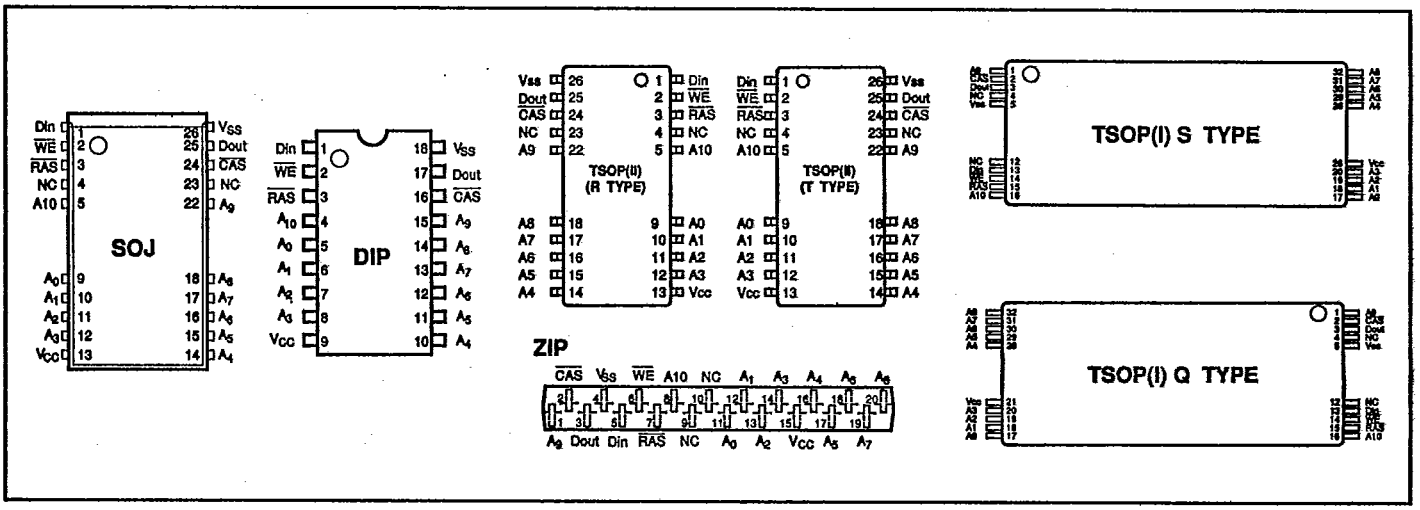
AAA2800 SERIES - 256K x 1



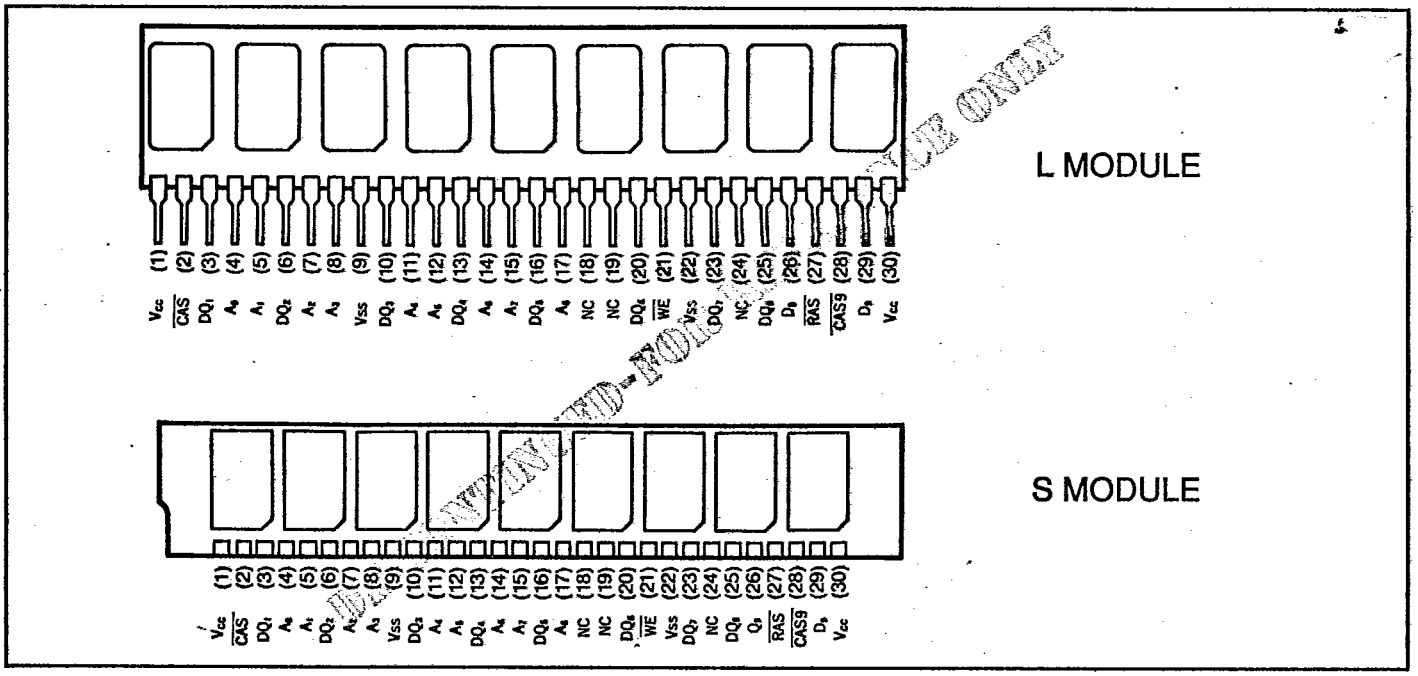
AAA1M300 SERIES - 1M x 1



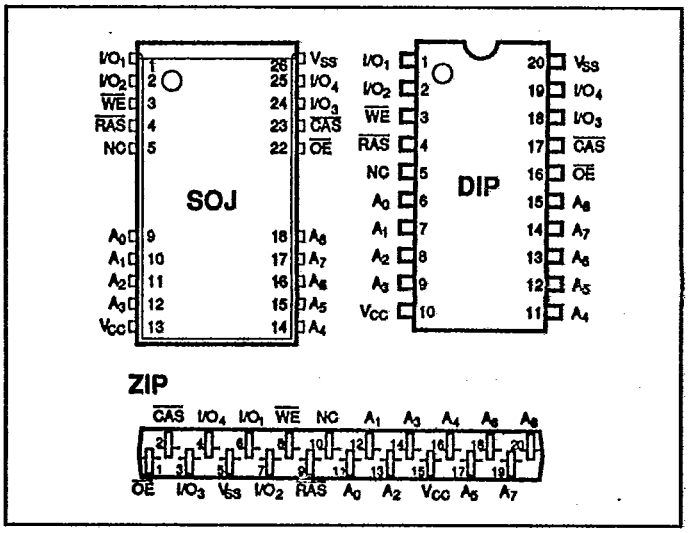
AAA4M200 SERIES - 4M x 1



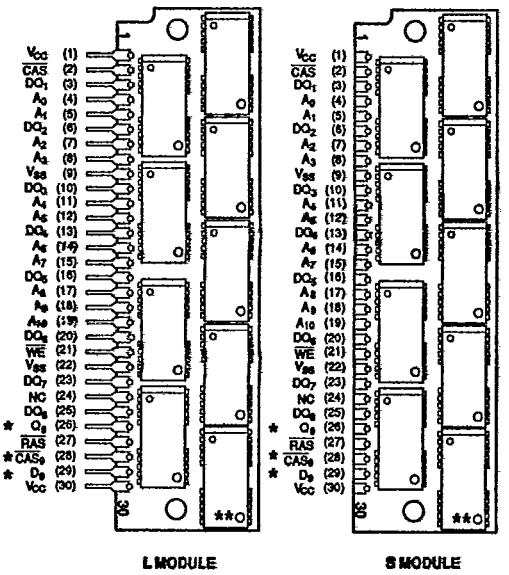
MM2800 J8/J9 SERIES - 256K x 8/9



AAA1M300 SERIES - 256K x 4

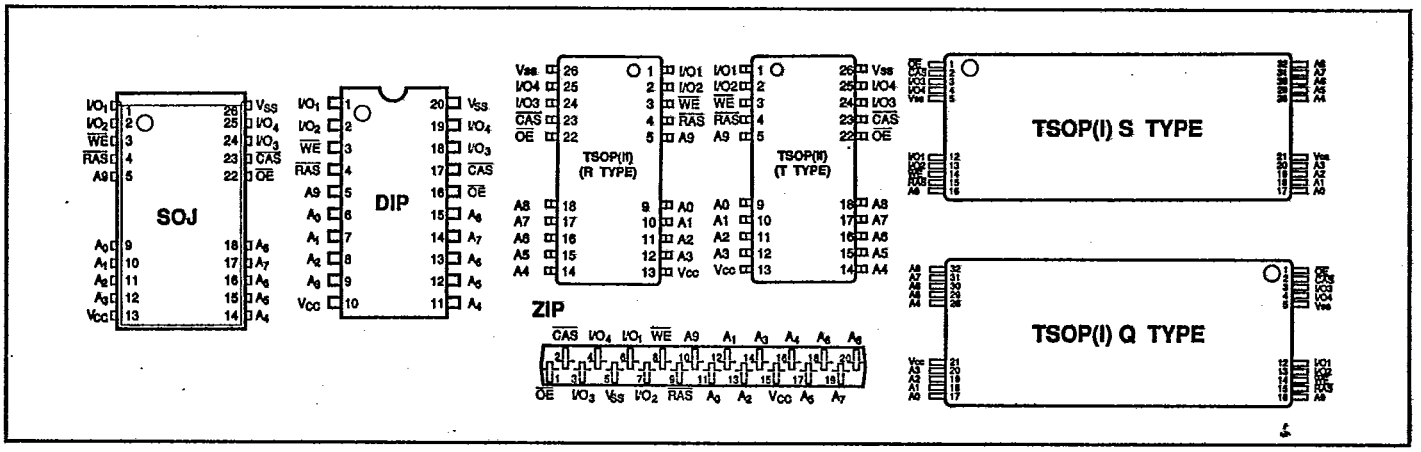


MM4M200 J8/J9 SERIES - 4M x 8/9

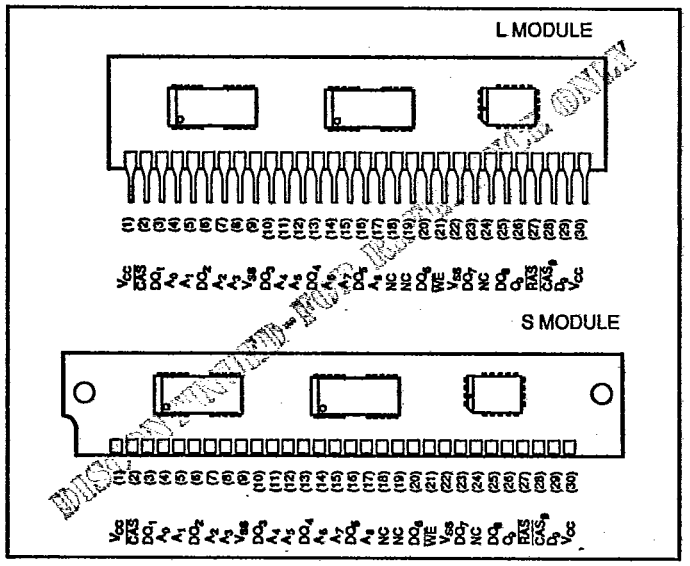


Notes:
1. * No connection (NC) for 4M x 8 bit module.
2. ** This chip is not mounted on 4M x 8 bit module.

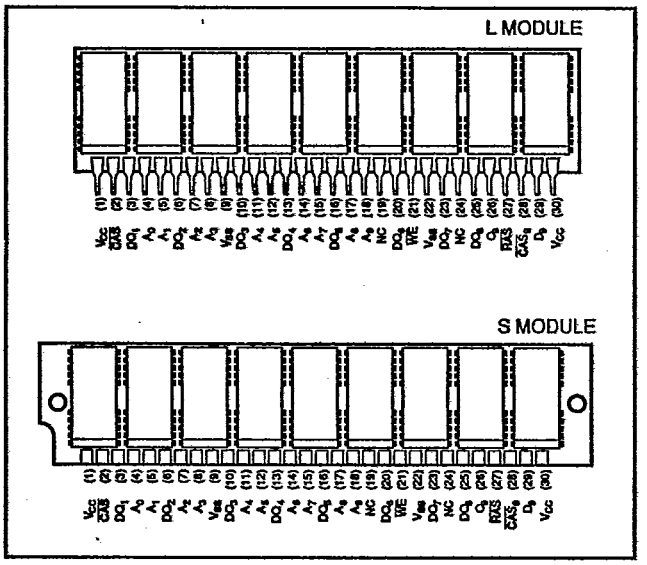
AAA4M200 SERIES - 1M x 4



MM256K0J9 SERIES - 256K x 9 (3 CHIP VERSION)



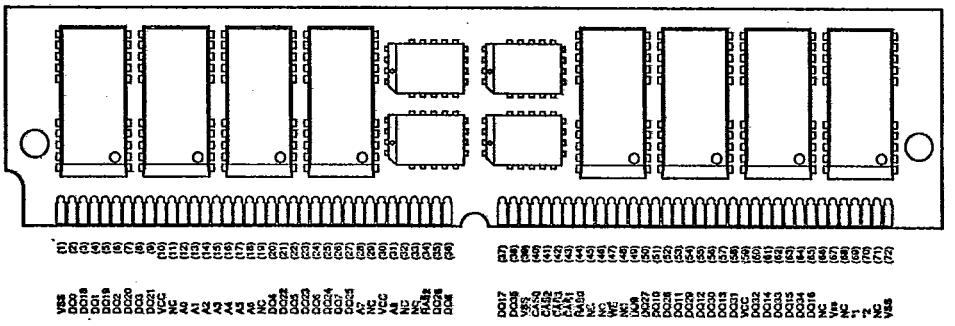
MM1M300J8/J9 SERIES - 1M x 8/9



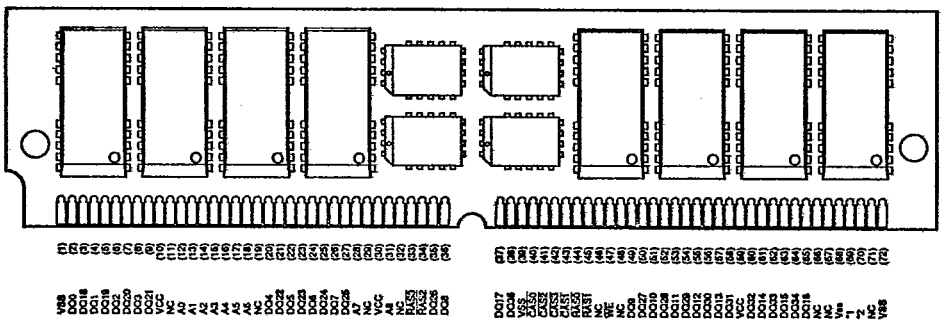
PACKAGE AND PINOUT DETAILS

MM256K0J36/MM512K0J36 SERIES - 256K x 36 and 512K x 36

256K x 36
(Components on one side of PCB)



512K x 36
(Components on both sides of PCB)



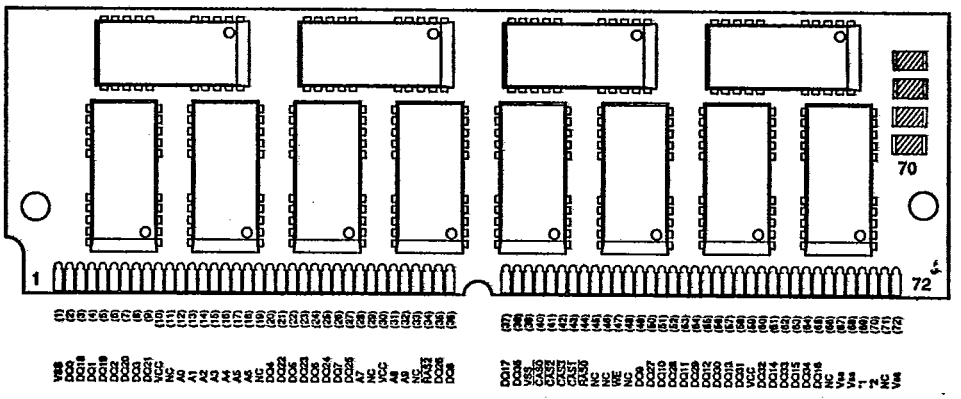
Pinout Variations

	-06	-07	-08
*1	TBD	Vss	NC
*2	TBD	NC	Vss

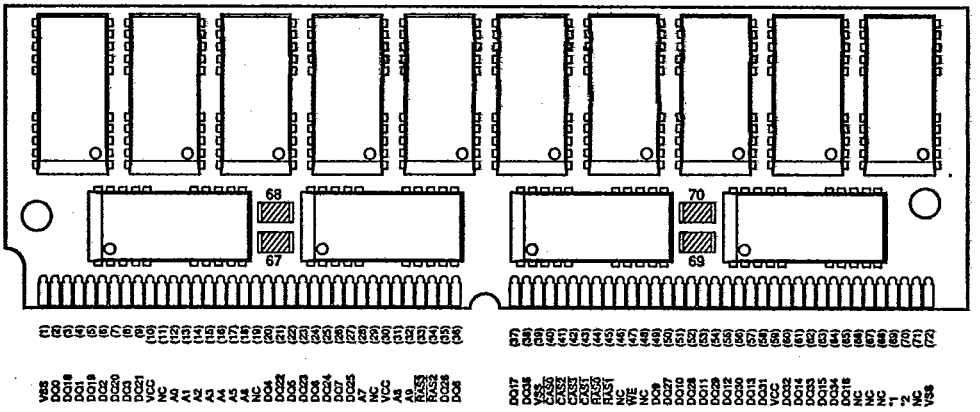
Note: TBD: To be determined

MM1M0J36/MM2M0J36 - 1M x 36 and 2M x 36

1M x 36
(Components on one side of PCB)



2M x 36
(Components on both sides of PCB)



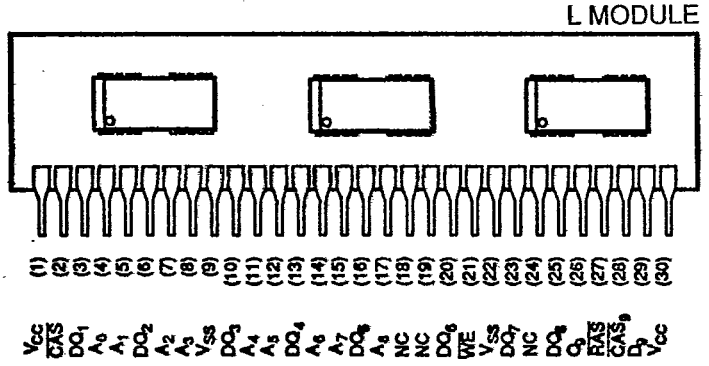
Pinout Variations

	-06	-07	-08
*1	TBD	Vss	NC
*2	TBD	NC	Vss

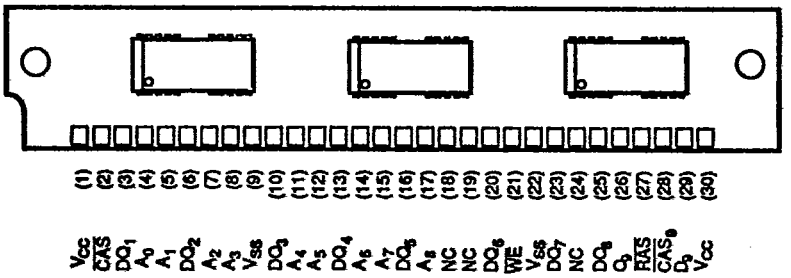
Note: TBD: To be determined

MM256K0J8R/J9R SERIES - (3 CHIP "R" VERSION)
MM1M0J8/J9 SERIES - (3 CHIP VERSION)
MM1M0J8R/J9R SERIES - (3 CHIP "R" VERSION)

L MODULE



S MODULE



Pinout 18 Variations

256K x 8/9	3 Chip "R"	N/C
1M x 8/9	3 Chip	A9
1M x 8/9	3 Chip "R"	A9