

MC100EP90



SO-20, DT SUFFIX
20 PIN PLASTIC TSSOP PACKAGE
CASE 948E

ORDERING INFORMATION
MC100EP90DT TSSOP

ECL_{PL}PS Plus™

Product Preview
**Triple LVECL to LVPECL
Translator**

- 350ps Typical Propagation Delay
- PECL mode: 3.0V to 5.5V VCC with VEE = 0V
- ECL mode: 0V VCC with VEE = -3.0V to -5.5V
- Fully Differential Design
- 20-Lead SOIC Package
- Internal Input Resistors: Pulldown on D, \bar{D}
- Q Output will default LOW with inputs open or at VEE
- ESD Protection: >4 kV HBM, > 200V MM
- Maximum Frequency > 2.7GHz
- VBB Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = devices

PIN DESCRIPTION

PIN	FUNCTION
Q(0:2), \bar{Q} (0:2)	Diff LVPECL Outputs
D(0:2), \bar{D} (0:2)	Diff LVECL Inputs
VCC	PECL +3.3V Supply
GND	Ground
VEE	LVECL -3.3V Supply
VBB	LVECL Reference Supply

The MC100EP90 is a TRIPLE LVECL TO LVPECL translator. The device receives Low Voltage differential LVECL signals and translates them to Low Voltage differential LVPECL output signals.

A VBB output is provided for interfacing with single ended LVECL signals at the input. If a single ended input is to be used the VBB output should be connected to the Db input. The active signal would then drive the D input. When used the VBB output should be bypassed to ground via a 0.01 μ F capacitor. The VBB output is designed to act as the switching reference for the EP90 under single ended input switching conditions, as a result this pin can only source/sink up to 0.5 mA of current.

To accomplish the level translation the EP90 requires three power rails. The VCC supply should be connected to the positive supply, and the VEE connected to the negative supply.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

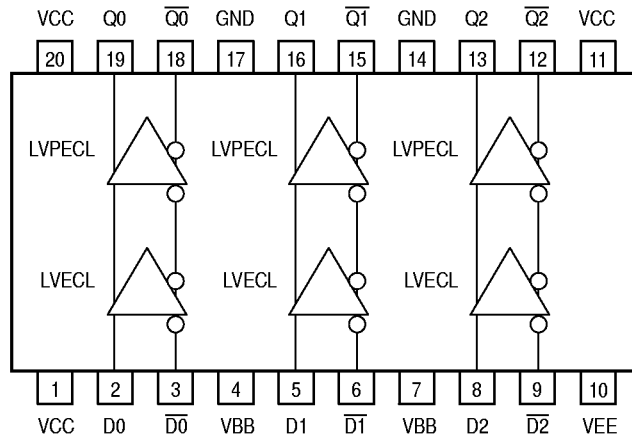


Figure 1. 20-Lead SOIC (Top View) and Logic Diagram

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{EE}	Power Supply (V _{CC} = 0V)	-6.0 to 0	VDC
V _{CC}	Power Supply (V _{EE} = 0V)	6.0 to 0	VDC
V _I	Input Voltage (V _{CC} = 0V, V _I not more negative than V _{EE})	-6.0 to 0	VDC
V _I	Input Voltage (V _{EE} = 0V, V _I not more positive than V _{CC})	6.0 to 0	VDC
I _{out}	Output Current	50 100	mA
I _{BB}	V _{BB} Sink/Source Current†	± 0.5	mA
T _A	Operating Temperature Range	-40 to +85	°C
T _{stg}	Storage Temperature	-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	190 130	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	41 to 44 ± 5%	°C/W
T _{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL ($V_{CC} = 0V$; $V_{EE} = -5.5V$ to $-3.0V$) (Note 4.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 1.)	23	24	29	23	24	29	23	24	29	mA
VOH	Output HIGH Voltage (Note 2.)	-1135	-1060	-885	-1070	-945	-820	-1010	-885	-760	mV
VOL	Output LOW Voltage (Note 2.)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
V _{IH}	Input HIGH Voltage Single Ended	-1210		-885	-1145		-820	-1085		-760	mV
V _{IL}	Input LOW Voltage Single Ended	-1935		-1610	-1870		-1545	-1810		-1485	mV
V _{BB}	Output Voltage Reference	-1510	-1410	-1310	-1445	-1345	-1245	-1385	-1285	-1185	mV
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V _{EE} +2.0		0.0	V _{EE} +2.0		0.0	V _{EE} +2.0		0.0	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	$\frac{D}{\bar{D}}$	0.5 -150		0.5 -150			0.5 -150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. $V_{CC} = 0V$, $V_{EE} = V_{EEmin}$ to V_{EEmax} , all other pins floating.
2. All loading with 50 ohms to $V_{CC}-2.0$ volts.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .
4. Input and output parameters vary 1:1 with V_{CC} .

DC CHARACTERISTICS, LVPECL ($V_{CC} = 3.3V \pm 0.3V$, $V_{EE} = 0V$) (Note 8.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)	23	24	29	23	24	29	23	24	29	mA
VOH	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
VOL	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V _{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V _{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V _{BB}	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	$\frac{D}{\bar{D}}$	0.5 -150		0.5 -150			0.5 -150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. $V_{CC} = 3.3V$, $V_{EE} = 0V$, all other pins floating.
6. All loading with 50 ohms to $V_{CC}-2.0$ volts.
7. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .
8. Input and output parameters vary 1:1 with V_{CC} .

DC CHARACTERISTICS, PECL ($V_{CC} = 5.0V \pm 0.5V$, $V_{EE} = 0V$) (Note 12.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current (Note 9.)	23	24	29	23	24	29	23	24	29	mA
V _{OH}	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V _{OL}	Output LOW Voltage (Note 10.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V _{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V _{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
V _{BB}	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	D D̄	0.5 -150		0.5 -150			0.5 -150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. $V_{CC} = 5.0V$, $V_{EE} = 0V$, all other pins floating.

10. All loading with 50 ohms to $V_{CC} - 2.0$ volts.

11. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

12. Input and output parameters vary 1:1 with V_{CC} .

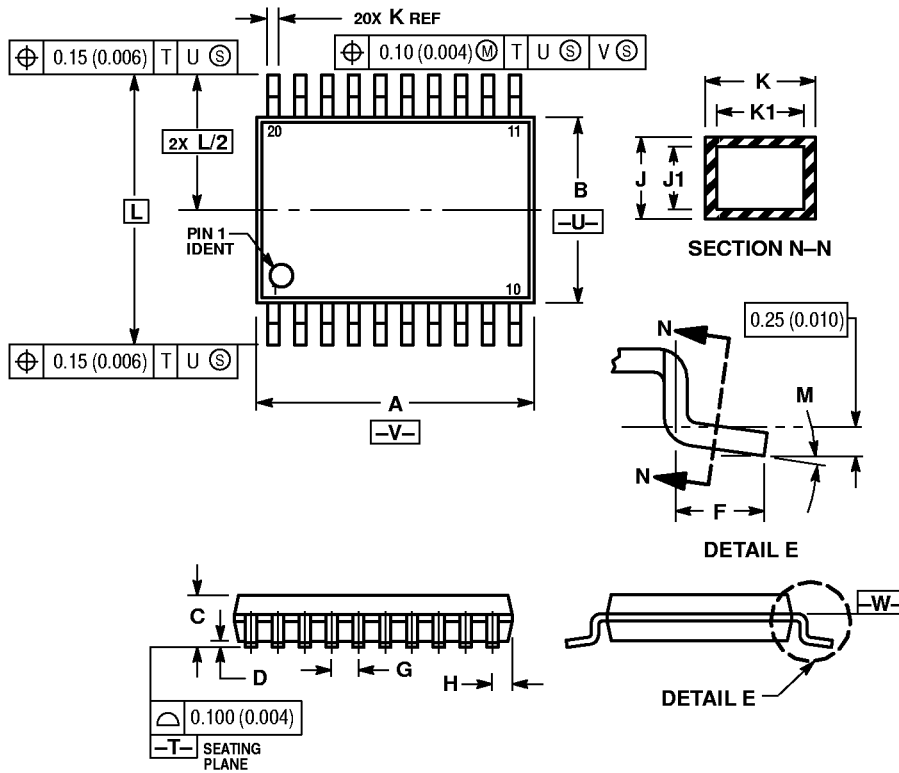
AC CHARACTERISTICS ($V_{CC} = 0V$; $V_{EE} = -3.0V$ to $-5.5V$) or ($V_{CC} = 3.0V$ to $5.5V$; $V_{EE} = 0V$)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{max}	Maximum Toggle Frequency (Note 13.)	2.7			2.7			2.7			GHz
t _{PLH} , t _{PHL}	Propagation Delay to Output Differential		160			160			160		ps
t _{SKEW}	Duty Cycle Skew (Note 14.)		5.0			5.0	20		5.0	20	ps
t _{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
V _{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t _r , t _f	Output Rise/Fall Times Q (20% - 80%)		110			110			110		ps

13. F_{max} guaranteed for functionality only. See Figure 2 for typical output swing. V_{OL} and V_{OH} levels are guaranteed at DC only.

14. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

OUTLINE DIMENSIONS
SO-20, DT SUFFIX
20 PIN PLASTIC TSSOP PACKAGE
CASE 948E-02
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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USA/EUROPE/ Locations Not Listed: Motorola Literature Distribution;
 P.O. Box 5405, Denver, Colorado 80217. 1-303-675-2140 or 1-800-441-2447

JAPAN: Motorola Japan Ltd.; SPD, Strategic Planning Office, 141,
 4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan. 81-3-5487-8488

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 2, Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.
 852-26629298

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