

April 1988

## Z84C30 CMOS Z80<sup>®</sup> CTC Counter/Timer Circuit

### FEATURES

- Four independently programmable counter/timer channels, each with a readable downcounter and a selectable 16 or 256 prescaler. Downcounters are reloaded automatically at zero count.
- Selectable positive or negative trigger initiates timer operation.
- Three channels have Zero Count/Timeout outputs capable of driving Darlington transistors.
- Interfaces directly to the Z80 CPU or—for baud rate generation—to the Z80 SIO.
- Standard Z80 Family daisy-chain interrupt structure provides fully vectored, prioritized interrupts without external logic. The CTC may also be used as an interrupt controller.
- Can be operated at 6.144 MHz clock

### GENERAL DESCRIPTION

The CMOS Z80 CTC (hereafter referred to as the Z80 CTC; or CTC) four-channel counter/timer can be programmed by system software for a broad range of counting and timing applications. The four independently programmable channels of the Z80 CTC satisfy common microcomputer system requirements for event counting, interrupt and interval timing, and general clock rate generation.

System design is simplified because the CTC connects directly to both the Z80 CPU and the Z80 SIO with no additional logic. In larger systems, address decoders and buffers may be required.

Programming the CTC is straightforward: each channel is programmed with two bytes; a third is necessary when

\*ZILGS020\*

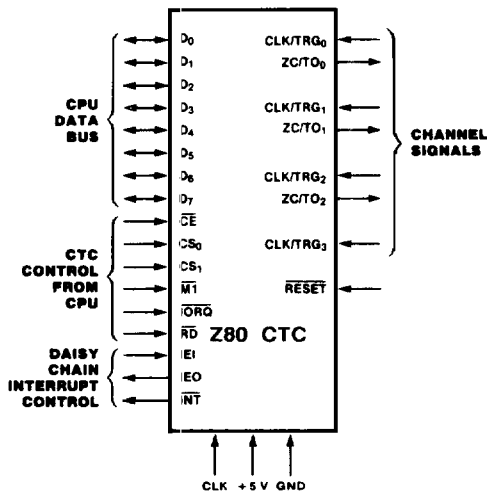


Figure 1. Pin Functions

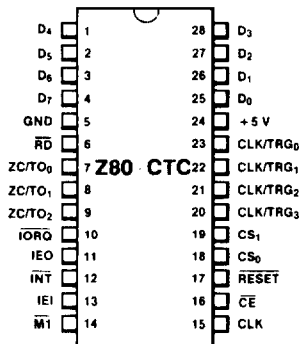


Figure 2. 40-pin Dual-In-Line Package (DIP), Pin Assignments

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interrupts are enabled. Once started, the CTC counts down, automatically reloads its time constant, and resumes counting. Software timing loops are completely eliminated. Interrupt processing is simplified because only one vector need be specified; the CTC internally generates a unique vector for each channel.

The Z80 CTC requires a single +5V power supply and the standard Z80 single-phase system clock. It is fabricated with n-channel silicon-gate depletion-load technology, and packaged in 28-pin DIPs.

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## FUNCTIONAL DESCRIPTION

The Z80 CTC has four independent counter/timer channels. Each channel is individually programmed with two words: a control word and a time-constant word. The control word selects the operating mode (counter or timer), enables or disables the channel interrupt, and selects certain other operating parameters. If the timing mode is selected, the control word also sets a prescaler, which divides the system clock by either 16 or 256. The time-constant word is a value from 1 to 256.

During operation, the individual counter channel counts down from the preset time constant value. In counter mode operation the counter decrements on each of the CLK/TRG input pulses until zero count is reached. Each decrement is synchronized by the system clock. For counts greater than 256, more than one counter can be cascaded. At zero count, the down-counter is automatically reset with the time constant value.

**The timer mode determines time intervals as small as 3  $\mu$ s without additional logic or software timing loops. Time intervals are generated by dividing the system clock with a prescaler that decrements a preset down-counter.**

Thus, the time interval is an integral multiple of the clock period, the prescaler value (16 or 256), and the time constant that is preset in the down-counter. A timer is triggered automatically when its time constant value is programmed, or by an external CLK/TRG input.

Three channels have two outputs that occur at zero count. The first output is a zero-count/timeout pulse at the ZC/TO output. The fourth channel (Channel 3) does not have a ZC/TO output; interrupt request is the only output available from Channel 3.

The second output is Interrupt Request ( $\overline{INT}$ ), which occurs if the channel has its interrupt enabled during programming. When the Z80 CPU acknowledges Interrupt Request, the Z80 CTC places an interrupt vector on the data bus.

The four channels of the Z80 CTC are fully prioritized and fit into four contiguous slots in a standard Z80 daisy-chain interrupt structure. Channel 0 is the highest priority and Channel 3 the lowest. Interrupts can be individually enabled (or disabled) for each of the four channels.

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## INTERNAL STRUCTURE

The CTC has four major elements, as shown in Figure 3.

- CPU bus I/O
- Channel control logic
- Interrupt logic
- Counter/timer circuits

**CPU Bus I/O.** The CPU bus I/O circuit decodes the address inputs, and interfaces the CPU data and control signals to the CTC for distribution on the internal bus.

**Internal Control Logic.** The CTC internal control logic controls overall chip operating functions such as the chip enable, reset, and read/write logic.

**Interrupt Logic.** The interrupt control logic ensures that the CTC interrupts interface properly with the Z80 CPU interrupt system. The logic controls the interrupt priority of the CTC as a function of the IEI signal. If IEI is High, the CTC has priority. During interrupt processing, the interrupt logic holds IEO Low, which inhibits the interrupt operation on lower priority devices. If the IEI input goes Low, priority is relinquished and the interrupt logic drives IEO Low.

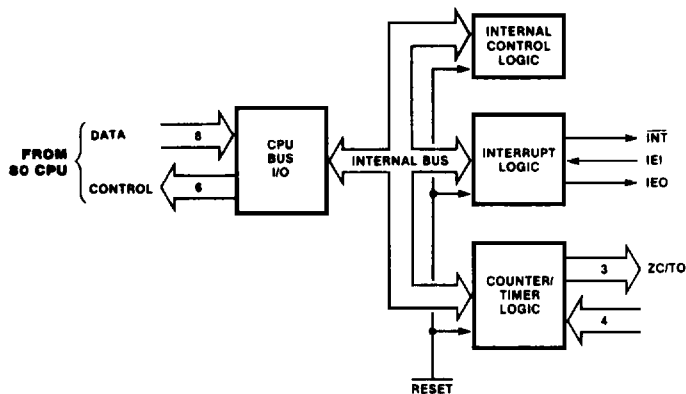


Figure 3. Functional Block Diagram

If a channel is programmed to request an interrupt, the interrupt logic drives IEO Low at the zero count, and generates an INT signal to the Z80 CPU. When the Z80 CPU responds with interrupt acknowledge ( $\overline{M1}$  and  $\overline{IORQ}$ ), then the interrupt logic arbitrates the CTC internal priorities, and the interrupt control logic places a unique interrupt vector on the data bus.

If an interrupt is pending, the interrupt logic holds IEO Low. When the Z80 CPU issues a Return From Interrupt (RETI) instruction, each peripheral device decodes the first byte ( $ED_{16}$ ). If the device has a pending interrupt, it raises IEO (High) for one  $\overline{M1}$  cycle. This ensures that all lower priority devices can decode the entire RETI instruction and reset properly.

**Counter/Timer Circuits.** The CTC has four independent counter/timer circuits, each containing the logic shown in Figure 4.

**Channel Control Logic.** The channel control logic receives the 8-bit channel control word when the counter/timer channel is programmed. The channel control logic decodes the control word and sets the following operating conditions:

- Interrupt enable (or disable)
- Operating mode (timer or counter)
- Timer mode prescaler factor (16 or 256)
- Active slope for CLK/TRG input
- Timer mode trigger (automatic or CLK/TRG input)
- Time constant data word to follow
- Software reset

**Time Constant Register.** When the counter/timer channel is programmed, the time constant register receives and stores an 8-bit time constant value, which can be anywhere from 1 to 256 (0 = 256). This constant is automatically loaded into the down-counter when the counter/timer channel is initialized, and subsequently after each zero count.

**Prescaler.** The prescaler, which is used only in timer mode, divides the system clock frequency by a factor of either 16 or 256. The prescaler output clocks the down-counter during timer operation. The effect of the prescaler on the down-counter is a multiplication of the system clock period by 16 or 256. The prescaler factor is programmed by bit 5 of the channel control word.

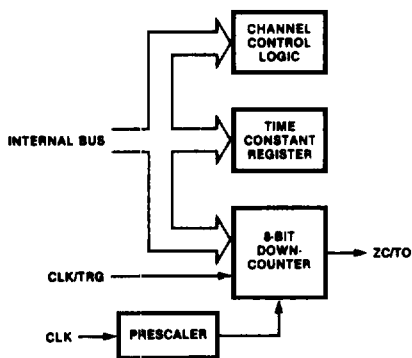


Figure 4. Counter/Timer Block Diagram

**Down-Counter.** Prior to each count cycle, the down-counter is loaded with the time constant register contents. The counter is then decremented one of two ways, depending on operating mode:

- By the prescaler output (timer mode)
- By the trigger pulses into the CLK/TRG input (counter mode)

Without disturbing the down-count, the Z80 CPU can read the count remaining at any time by performing an I/O read operation at the port address assigned to the CTC channel. When the down-counter reaches the zero count, the ZC/TO

output generates a positive-going pulse. When the interrupt is enabled, zero count also triggers an interrupt request signal ( $\overline{\text{INT}}$ ) from the interrupt logic.

## PIN DESCRIPTION

**$\overline{\text{CE}}$ .** *Chip Enable* (input, active Low). When enabled the CTC accepts control words, interrupt vectors, or time constant data words from the data bus during an I/O write cycle; or transmits the contents of the downcounter to the CPU during an I/O read cycle. In most applications this signal is decoded from the eight least significant bits of the address bus for any of the four I/O port addresses that are mapped to the four counter-timer channels.

**CLK.** *System Clock* (input). Standard single-phase Z80 system clock.

**CLK/TRG<sub>0</sub>-CLK/TRG<sub>3</sub>.** *External Clock/Timer Trigger* (input, user-selectable active High or Low). Four pins corresponding to the four Z80 CTC channels. In counter mode, every active edge on this pin decrements the downcounter. In timer mode, an active edge starts the timer.

**CS<sub>0</sub>-CS<sub>1</sub>.** *Channel Select* (inputs active High). Two-bit binary address code selects one of the four CTC channels for an I/O write or read (usually connected to A<sub>0</sub> and A<sub>1</sub>).

**D<sub>0</sub>-D<sub>7</sub>.** *System Data Bus* (bidirectional, 3-state). Transfers all data and commands between the Z80 CPU and the Z80 CTC.

**IEI.** *Interrupt Enable In* (input, active High). A High indicates that no other interrupting devices of higher priority in the daisy chain are being serviced by the Z80 CPU.

**IEO.** *Interrupt Enable Out* (output, active High). High only if IEI is High and the Z80 CPU is not servicing an interrupt from any Z80 CTC channel. IEO blocks lower priority devices from interrupting while a higher priority interrupting device is being serviced.

**$\overline{\text{INT}}$ .** *Interrupt Request* (output, open drain, active Low). Low when any Z80 CTC channel that has been programmed to enable interrupts as a zero-count condition in its downcounter.

**$\overline{\text{IORQ}}$ .** *Input/Output Request* (input from CPU, active Low). Used with  $\overline{\text{CE}}$  and  $\overline{\text{RD}}$  to transfer data and channel control words between the Z80 CPU and the Z80 CTC. During a write cycle,  $\overline{\text{IORQ}}$  and  $\overline{\text{CE}}$  are active and  $\overline{\text{RD}}$  inactive. The Z80 CTC does not receive a specific write signal; rather, it internally generates its own from the inverse of an active  $\overline{\text{RD}}$  signal. In a read cycle,  $\overline{\text{IORQ}}$ ,  $\overline{\text{CE}}$ , and  $\overline{\text{RD}}$  are active; the contents of the downcounter are read by the Z80 CPU. If  $\overline{\text{IORQ}}$  and  $\overline{\text{M1}}$  are both true, the CPU is acknowledging an interrupt request, and the highest priority interrupting channel places its interrupt vector on the Z80 data bus.

**M1.** *Machine Cycle One* (input from CPU, active Low). When  $\overline{\text{M1}}$  and  $\overline{\text{IORQ}}$  are active, the Z80 CPU is acknowledging an interrupt. The Z80 CTC then places an interrupt vector on the data bus if it has highest priority, and if a channel has requested an interrupt ( $\overline{\text{INT}}$ ).

**$\overline{\text{RD}}$ .** *Read Cycle Status* (input, active Low). Used in conjunction with  $\overline{\text{IORQ}}$  and  $\overline{\text{CE}}$  to transfer data and channel control words between the Z80 CPU and the Z80 CTC.

**RESET.** *Reset* (input active Low). Terminates all down-counts and disables all interrupts by resetting the interrupt bits in all control registers; the ZC/TO and the interrupt outputs go inactive; IEO reflects IEI; D<sub>0</sub>-D<sub>7</sub> go to the high-impedance state.

**ZC/TO<sub>0</sub>-ZC/TO<sub>2</sub>.** *Zero Count/Timeout* (output, active High). Three ZC/TO pins corresponding to Z80 CTC channels 2 through 0 (Channel 3 has no ZC/TO pin). In both counter and timer modes the output is an active High pulse when the downcounter decrements to zero.

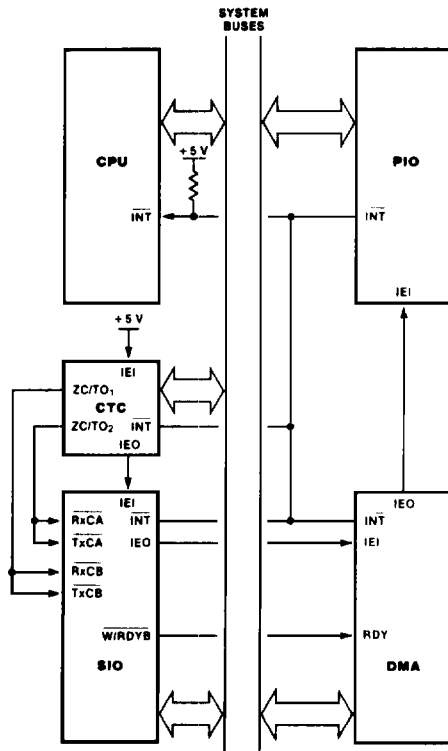


Figure 8. A Typical Z80 Environment

## ABSOLUTE MAXIMUM RATINGS

Voltages on  $V_{CC}$  with respect to  $V_{SS}$  . . . . .  $-0.3V$  to  $+7.0V$   
 Voltages on all inputs with respect  
 to  $V_{SS}$  . . . . .  $-0.3V$  to  $V_{CC} + 0.3V$   
 Storage Temperature . . . . .  $-65^{\circ}C$  to  $+150^{\circ}C$   
**Operating Case Temperature . . . . .  $-55^{\circ}C$  to  $+125^{\circ}C$**   
**Absolute Maximum Power Dissipation . . . . .  $1W$**

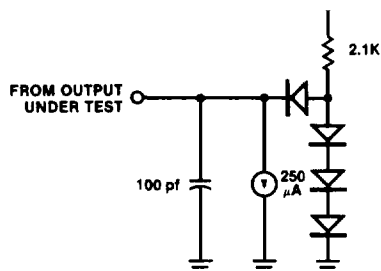
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above these indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## STANDARD TEST CONDITIONS

The characteristics below apply for the following test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin. Available operating temperature range is:

■ **M =  $-55^{\circ}C$  to  $+125^{\circ}C$ ,  $+4.50V \leq V_{CC} \leq 5.50V$**

The Ordering Information section lists package temperature ranges and product numbers. Refer to the Literature List for additional documentation. Package drawings are in the Package Information section.



## DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Test Condition
$V_{ILC}$	Clock Input Low Voltage	$-0.3^c$	$+0.45^a$	V	
$V_{IHC}$	Clock Input High Voltage	$V_{CC} - 0.6^a$	$V_{CC} + 0.3^c$	V	
$V_{IL}$	Input Low Voltage	$-0.3^c$	$+0.8^a$	V	
$V_{IH}$	Input High Voltage	$+2.2^a$	$V_{CC}^a$	V	
$V_{OL}$	Output Low Voltage		$+0.4^a$	V	$I_{OL} = 2.0\text{ mA}$
$V_{OH1}$	Output High Voltage	$+2.4^a$		V	$I_{OH} = -1.6\text{ mA}$
$V_{OH2}$	Output High Voltage	$V_{CC} - 0.8^a$		V	$I_{OH} = -250\ \mu\text{A}$
$I_{LI}$	Input Leakage Current		$\pm 10^a$	$\mu\text{A}$	$V_{IN} = 0.4$ to $V_{CC}$
$I_{LO}$	3-State Output Leakage Current in Float		$\pm 10^a$	$\mu\text{A}$	$V_{OUT} = 0.4$ to $V_{CC}$
$ICC_1$	Power Supply Current		$10^a$	mA	$V_{CC} = 5V$ $CLK = 6\text{ MHz}$ $V_{IH} = V_{CC} - 0.2V$ $V_{IL} = 0.2V$
$ICC_2$	Standby Supply Current		$100\ \mu\text{A}^a$	$\mu\text{A}$	$V_{CC} = 5V$ $CLK = (0)$
$I_{OHD}$	Darlington Drive Current	$-1.5^c$	$-5.0^c$	mA	$V_{IH} = V_{CC} - 0.2V$ $V_{IL} = 0.2V$ $V_{OH} = 1.5V$ $R_{EXT} = 1.1K\ \Omega$

Over specified temperature and voltage range.

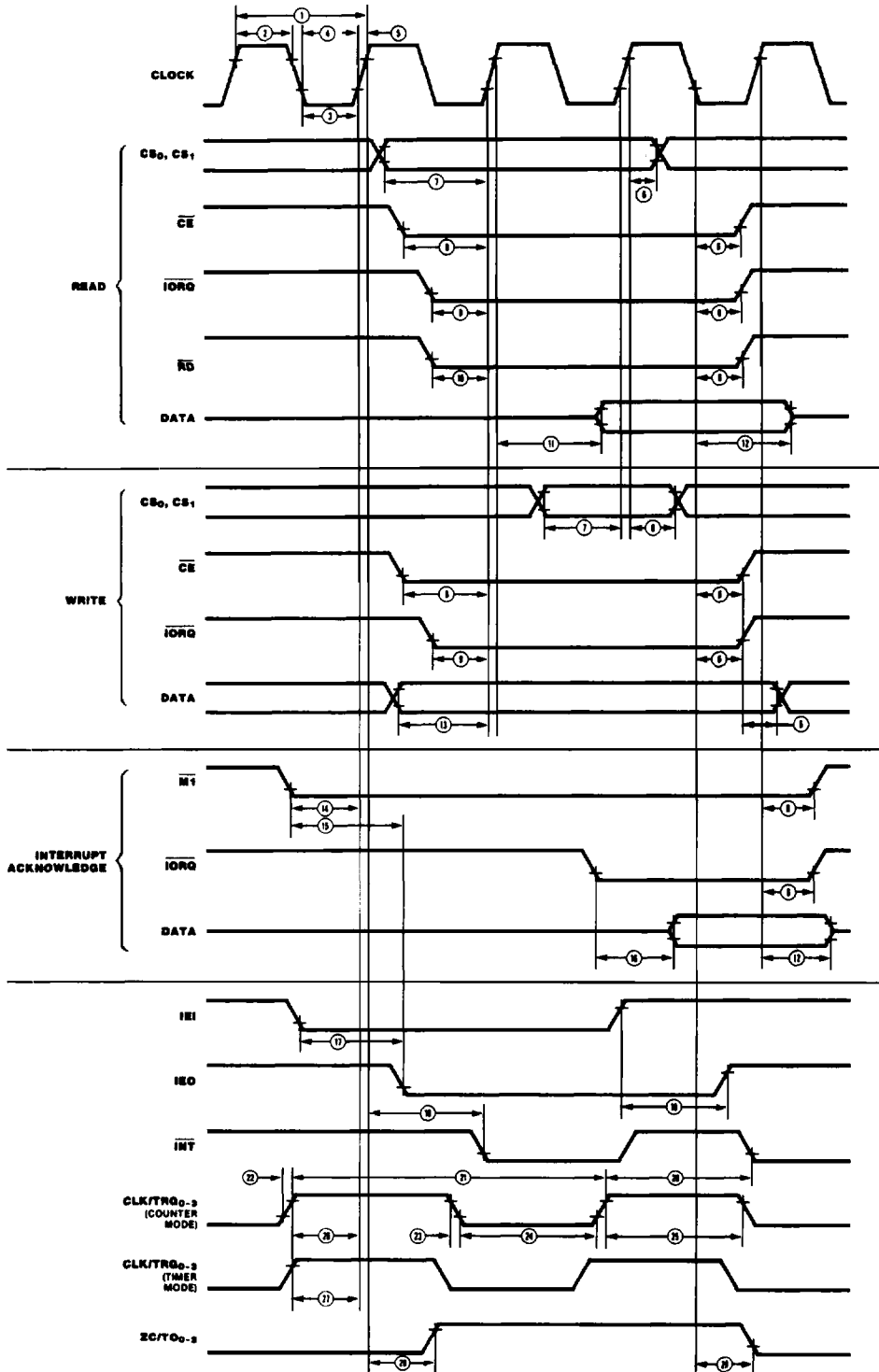
## CAPACITANCE

Symbol	Parameter	Max	Unit
CLK	Clock Capacitance	$10^c$	pf
$C_{IN}$	Input Capacitance	$10^c$	pf
$C_{OUT}$	Output Capacitance	$15^c$	pf

$T_A = 25^{\circ}C$ ,  $f = 1\text{ MHz}$   
 Unmeasured pins returned to ground

**NOTES:** 1. Parameter Test Status:  
 a. Tested  
 b. Guaranteed  
 c. Guaranteed by characterization/design  
 2.  $ICC_1$  is measured with 100pF capacitive only test load.

# AC CHARACTERISTICS



## AC CHARACTERISTICS (Continued)

No.	Symbol	Parameter	Z84C3006		Notes*
			Min(ns)	Max(ns)	
1	TcC	Clock Cycle Time	162 <sup>a</sup>	DC[1]	
2	TwCh	Clock Pulse Width (High)	65 <sup>a</sup>	DC	
3	TwCl	Clock Pulse Width (Low)	65 <sup>a</sup>	DC	
4	TfC	Clock Fall Time		20 <sup>c</sup>	
5	TrC	Clock Rise Time		20 <sup>c</sup>	
6	Th	All Hold Times		0 <sup>c</sup>	
7	TsCS(C)	CS to Clock ↑ Setup Time	100 <sup>a</sup>		
8	TsCE(C)	CE to Clock ↑ Setup Time	100 <sup>a</sup>		
9	TsIO(C)	IORQ ↓ to Clock ↑ Setup Time	70 <sup>a</sup>		
10	TsRD(C)	RD ↓ to Clock ↑ Setup Time	70 <sup>a</sup>		
11	TdC(DO)	Clock ↑ to Data Out Delay		130 <sup>a</sup>	[2]
12	TdRlr(DOz)	RD, IORQ ↓ to Data Out Float Delay		40 <sup>c</sup>	
13	TsDI(C)	Data In to Clock ↑ Setup Time	40 <sup>a</sup>		
14	TsM1(C)	M1 to Clock ↑ Setup Time	70 <sup>a</sup>		
15	TdM1(E0)	M1 ↓ to IEO ↓ Delay (Interrupt immediately preceding M1)		130 <sup>c</sup>	[3]
16	TdIO(DOI)	IORQ ↓ to Data Out Delay (INTA)		110 <sup>a</sup>	[2],[6]
17	TdIEI(IEOf)	IEI ↓ to IEO ↓ Delay		100 <sup>a</sup>	[3]
18	TdIEI(IEOr)	IEI ↑ to IEO ↑ Delay (after ED Decode)		110 <sup>a</sup>	[3]
19	TdC(INT)	Clock ↑ to INT ↓ Delay		TcC +120 <sup>a</sup>	[4]
20	TdCLK(INT)	CLK/TRG ↑ to INT ↓ tsCTR(C) satisfied tsCTR(C) not satisfied		(19)+(26) <sup>c</sup> (1)+(19)+(26) <sup>c</sup>	[5] [5]
21	TcCTR	CLK/TRG Cycle Time	(2TcC) <sup>c</sup>		
22	TrCTR	CLK/TRG Rise Time		40 <sup>a</sup>	
23	TfCTR	CLK/TRG Fall Time		40 <sup>a</sup>	
24	TwCTRI	CLK/TRG Width (Low)	120 <sup>c</sup>		
25	TwCTRh	CLK/TRG Width (High)	120 <sup>c</sup>		
26	TsCTR(Cs)	CLK/TRG ↑ to Clock ↑ Setup Time for Immediate Count	150 <sup>a</sup>		
27	TsCTR(Ct)	CLK/TRG ↑ to Clock ↑ Setup Time for enabling of Prescaler on following clock ↑	150 <sup>a</sup>		
28	TdC(ZC/TOr)	Clock ↑ to ZC/TO ↑ Delay		140 <sup>a</sup>	
29	TdC(ZC/TOf)	Clock ↓ to ZC/TO ↓ Delay		140 <sup>a</sup>	

\*RESET must be active for a minimum of 3 clock cycles

### NOTES

[1] TcC = TwCh + TwCl + TrC + TfC.

[2] Increase delay by 10 ns for each 50 pf increase in loading, 200 pf maximum for data lines, and 100 pf for control lines

[3] Increase delay by 2 ns for each 10 pf increase in loading, 100 pf maximum.

[4] Timer mode.

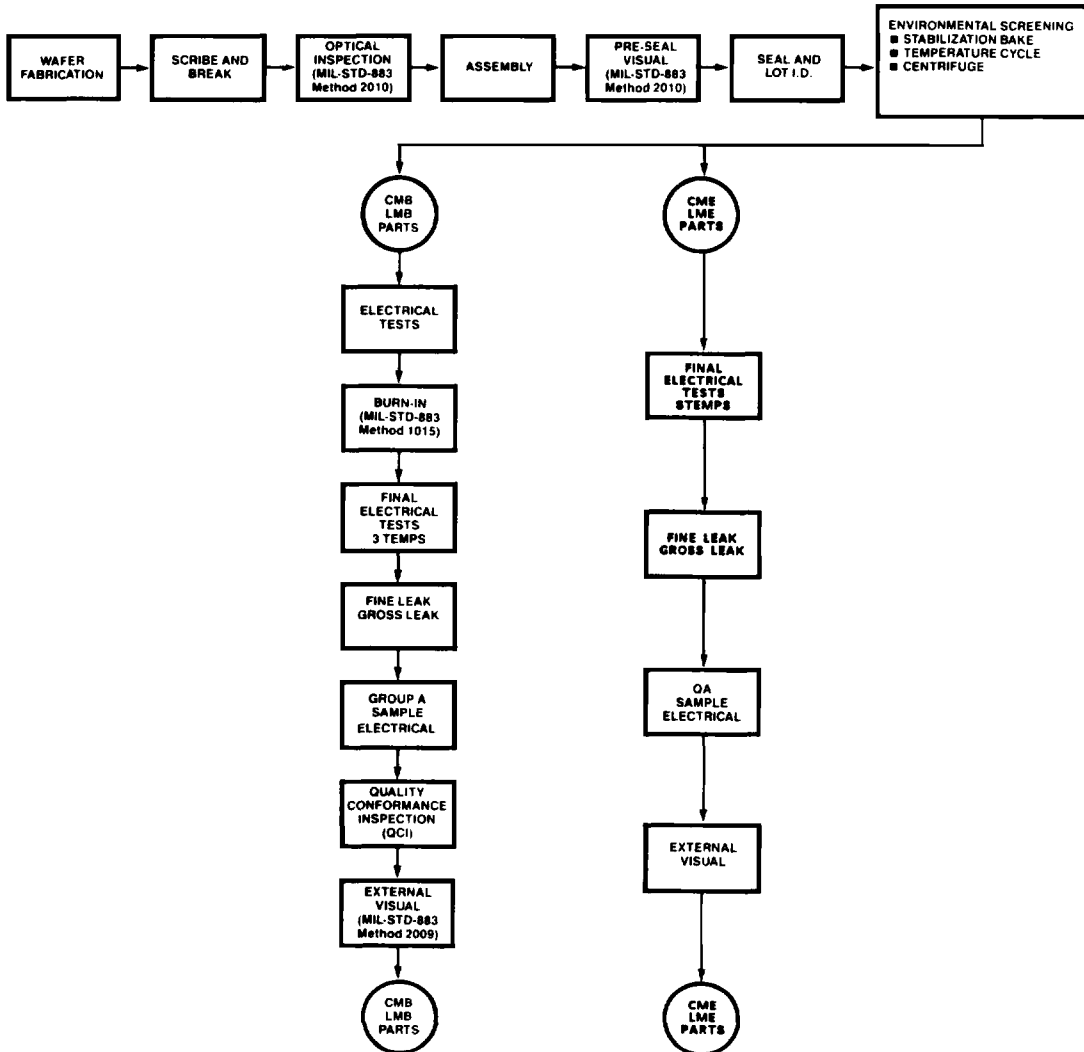
[5] Counter mode.

[6]  $2.5 TcC > (n-2) TdIEI(IEOf) + TdM1(IEO) + TsIEI(IEO) + TTL$  buffer delay, if any.

## MIL-STD-883 MILITARY PROCESSED PRODUCT

- Mil-Std-883 establishes uniform methods and procedures for testing microelectronic devices to insure the electrical, mechanical, and environmental integrity and reliability that is required for military applications.
- Mil-Std-883 Class B is the industry standard product assurance level for military ground and aircraft application.
- The total reliability of a system depends upon tests that are designed to stress specific quality and reliability concerns that affect microelectronic products.
- The following tables detail the 100% screening and electrical tests, sample electrical tests, and Qualification/Quality Conformance testing required.

### Zilog Military Product Flow



**Table I**  
**MIL-STD-883 Class B Screening Requirements**  
**Method 5004**

<b>Test</b>	<b>MIL-Std-883 Method</b>	<b>Test Condition</b>	<b>Requirement</b>	
Internal Visual	2010	Condition B	100%	
Stabilization Bake	1008	Condition C	100%	
Temperature Cycle	1010	Condition C	100%	
Constant Acceleration (Centrifuge)	2001	Condition E or D <sup>(Note 1)</sup> , Y <sub>1</sub> Axis Only	100%	
Initial Electrical Tests		Zilog Military Electrical Specification Static/DC T <sub>C</sub> = +25 °C	100%	
Burn-In	1015	Condition D <sup>(Note 2)</sup> , 160 hours, T <sub>A</sub> = +125 °C	100%	
Interim Electrical Tests		Zilog Military Electrical Specification Static/DC T <sub>C</sub> = +25 °C	100%	
PDA Calculation		PDA = 5%	100%	
Final Electrical Tests		Zilog Military Electrical Specification Static/DC T <sub>C</sub> = +125 °C, -55 °C Functional, Switching/AC T <sub>C</sub> = +25 °C	100%	
Fine Leak	1014	Condition B	100%	
Gross Leak	1014	Condition C	100%	
<b>Quality Conformance Inspection (QCI)</b>				
Group A	Each Inspection Lot	5005	(See Table II)	Sample
Group B	Every Week	5005	(See Table III)	Sample
Group C	Periodically <sup>(Note 3)</sup>	5005	(See Table IV)	Sample
Group D	Periodically <sup>(Note 3)</sup>	5005	(See Table V)	Sample
External Visual	2009			100%
QA—Ship				100%

**NOTES:**

1. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
2. In process of fully implementing of Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.
3. Performed periodically as required by Mil-Std-883, paragraph 1.2.1 b(17).

**Table II Group A  
Sample Electrical Tests  
MIL-STD-883 Method 5005**

<b>Subgroup</b>	<b>Tests</b>	<b>Temperature (T<sub>c</sub>)</b>	<b>LTPD Max Accept = 2</b>
<b>Subgroup 1</b>	Static/DC	+ 25 °C	2
<b>Subgroup 2</b>	Static/DC	+ 125 °C	3
<b>Subgroup 3</b>	Static/DC	- 55 °C	5
<b>Subgroup 7</b>	Functional	+ 25 °C	2
<b>Subgroup 8</b>	Functional	- 55 °C and + 125 °C	5
<b>Subgroup 9</b>	Switching/AC	+ 25 °C	2
<b>Subgroup 10</b>	Switching/AC	+ 125 °C	3
<b>Subgroup 11</b>	Switching/AC	- 55 °C	5

NOTES:

- The specific parameters to be included for tests in each subgroup shall be as specified in the applicable detail electrical specification. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test.
- A single sample may be used for all subgroup testing. Where required size exceeds the lot size, 100% inspection shall be allowed.
- Group A testing by subgroup or within subgroups may be performed in any sequence unless otherwise specified.

**Table III Group B**  
**Sample Test Performed Every Week to**  
**Test Construction and Insure Integrity of Assembly Process.**  
**MIL-STD-883 Method 5005**

<b>Subgroup</b>	<b>MIL-Std-883 Method</b>	<b>Test Condition</b>	<b>Quantity or LTPD/Max Accept</b>
<b>Subgroup 1</b> Physical Dimensions	2016		2/0
<b>Subgroup 2</b> Resistance to Solvents	2015		4/0
<b>Subgroup 3</b> Solderability	2003	Solder Temperature + 245°C ± 5°C	15 <sup>(Note 1)</sup>
<b>Subgroup 4</b> Internal Visual and Mechanical	2014		1/0
<b>Subgroup 5</b> Bond Strength	2011	C	15 <sup>(Note 2)</sup>
<b>Subgroup 6</b> <sup>(Note 3)</sup> Internal Water Vapor Content	1018	1000 ppm. maximum at + 100°C	3/0 or 5/1
<b>Subgroup 7</b> <sup>(Note 4)</sup> Seal 7a) Fine Leak 7b) Gross Leak	1014	7a) B 7b) C	5
<b>Subgroup 8</b> <sup>(Note 5)</sup> Electrostatic Discharge Sensitivity	3015	Zilog Military Electrical Specification Static/DC T <sub>C</sub> = + 25°C A = 20-2000V B = >2000V Zilog Military Electrical Specification Static/DC T <sub>C</sub> = + 25°C	15/0

**NOTES:**

1. Number of leads inspected selected from a minimum of 3 devices.
2. Number of bond pulls selected from a minimum of 4 devices.
3. Test applicable only if the package contains a dessicant.
4. Test not required if either 100% or sample seal test is performed between final electrical tests and external visual during Class B screening.
5. Test required for initial qualification and product redesign.

**Table IV Group C**  
**Sample Test Performed Periodically to Verify Integrity of the Die.**  
**MIL-STD-883 Method 5005**

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
<b>Subgroup 1</b>			
Steady State Operating Life	1005	Condition D <sup>(Note 1)</sup> , 1000 hours at + 125°C	5
End Point Electrical Tests		Zilog Military Electrical Specification T <sub>C</sub> = + 25°C, + 125°C, - 55°C	
<b>Subgroup 2</b>			
Temperature Cycle	1010	Condition C	
Constant Acceleration (Centrifuge)	2001	Condition E or D <sup>(Note 2)</sup> , Y <sub>1</sub> Axis Only	
Seal	1014		15
2a) Fine Leak		2a) Condition B	
2b) Gross Leak		2b) Condition C	
Visual Examination	1010 or 1011		
End Point Electrical Tests		Zilog Military Electrical Specification T <sub>C</sub> = + 25°C, + 125°C, - 55°C	

NOTE:

1. In process of fully implementing Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.
2. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.

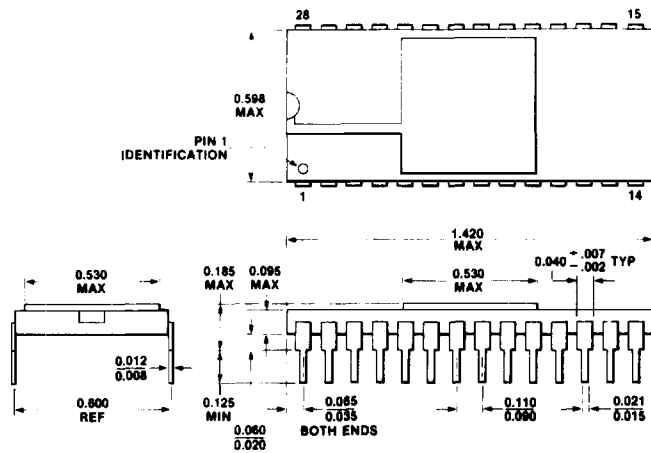
**Table V Group D**  
**Sample Test Performed Periodically to Insure Integrity of the Package.**  
**MIL-STD-883 Method 5005**

<b>Subgroup</b>	<b>Mil-Std-883 Method</b>	<b>Test Condition</b>	<b>Quantity or LTPD/Max Accept</b>
<b>Subgroup 1</b> Physical Dimensions	2016		15
<b>Subgroup 2</b> Lead Integrity	2004	Condition B <sub>2</sub> or D <sup>(Note 1)</sup>	15
<b>Subgroup 3</b> Thermal Shock	1011	Condition B minimum, 15 cycles minimum	
Temperature Cycling	1010	Condition C, 100 cycles minimum	15
Moisture Resistance	1004		
Seal	1014		
3a) Fine Leak		3a) Condition B	
3b) Gross Leak		3b) Condition C	
Visual Examination	1004 or 1010		
End Point Electrical Tests		Zilog Military Electrical Specification T <sub>C</sub> = +25°C, +125°C, -55°C	
<b>Subgroup 4</b> Mechanical Shock	2002	Condition B minimum	
Vibration Variable Frequency	2007	Condition A minimum	
Constant Acceleration (Centrifuge)	2001	Condition E or D <sup>(Note 2)</sup> , Y <sub>1</sub> Axis Only	15
Seal	1014		
4a) Fine Leak		4a) Condition B	
4b) Gross Leak		4b) Condition C	
Visual Examination	1010 or 1011		
End Point Electrical Tests		Zilog Military Electrical Specification T <sub>C</sub> = +25°C, +125°C, -55°C	
<b>Subgroup 5</b> Salt Atmosphere	1009	Condition A minimum	
Seal	1014		15
5a) Fine Leak		5a) Condition B	
5b) Gross Leak		5b) Condition C	
Visual Examination	1009		
<b>Subgroup 6</b> Internal Water Vapor Content	1018	5,000 ppm. maximum water content at +100°C	3/0 or 5/1
<b>Subgroup 7</b> <sup>(Note 3)</sup> Adhesion of Lead Finish	2025		15 <sup>(Note 4)</sup>
<b>Subgroup 8</b> <sup>(Note 5)</sup> Lid Torque	2024		5/0

NOTES:

- |  |  |
|--|--|
| 1. Lead Integrity Condition D for leadless chip carriers.  | 3. Not applicable to leadless chip carriers. |
| 2. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams. | 4. LTPD based on number of leads.            |
|  | 5. Not applicable for solder seal packages.  |

# PACKAGE INFORMATION



28-Pin Ceramic Package (DIP)

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## ORDERING INFORMATION

CMOS Z80 CTC  
28-pin DIP  
6 MHz  
Z84C3006CMB  
Z84C3006CME

### Codes

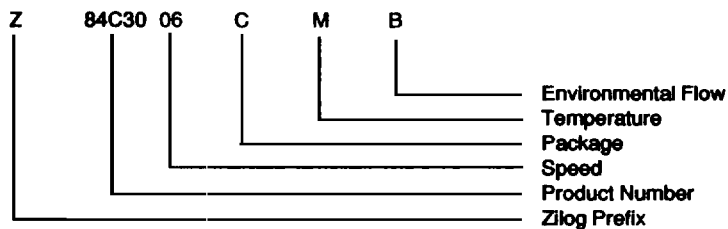
**PACKAGE**  
C = Ceramic

**TEMPERATURE**  
M = -55°C to +125°C

**ENVIRONMENTAL**  
E = Hermetic Standard  
B = 833 Class B Military

### Example:

Z84C3006CMB is a CMOS 8430, 6MHz, Ceramic -55°C to 125°C, 883C Standard Flow



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All specifications (parameters) are subject to change without notice. The applicable Zilog test documentation will specify which parameters are tested.

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