

# SED1742/44

- CMOS 160-bit Segment Driver
- High Voltage LCD Driver

## ■ DESCRIPTION

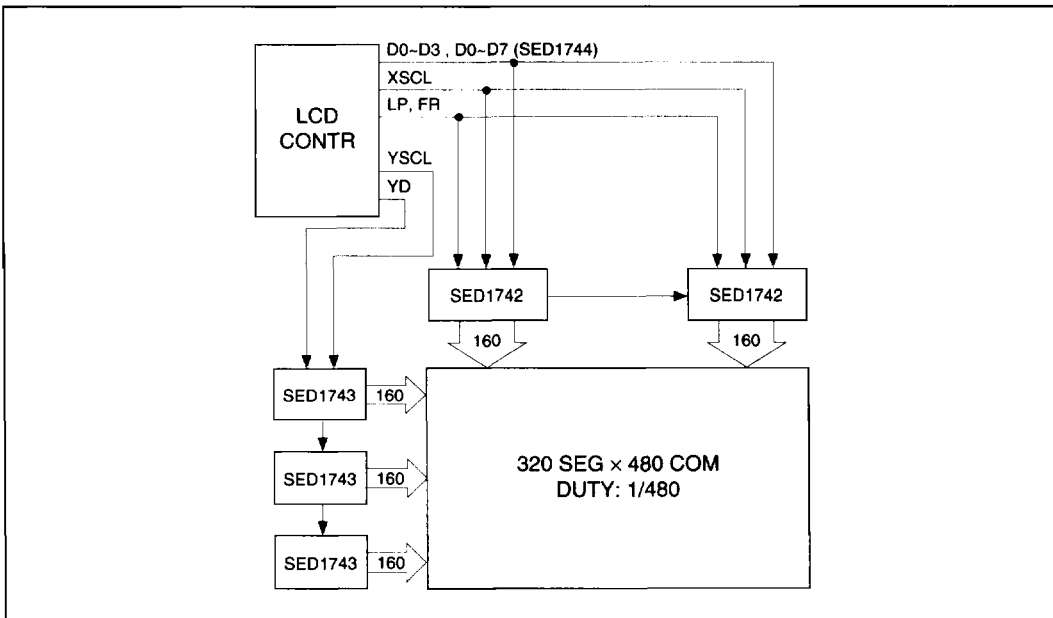
The SED1742/SED1744 is a 160 dot matrix LCD segment (column) driver for driving high-capacity LCD panels at duty cycles higher than 1/100 (up to 1/500). The LSI features a wide range of LCD voltages. The upper and lower LCD drive voltages (V0, V5) are independent of the chip supplies. This enables the LCD drive bias voltages to be supplied from an external source. The device uses a daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver.

The SED1742/44 is used in conjunction with the SED1743 (160-bit common driver) to drive a large-capacity dot matrix LCD panel.

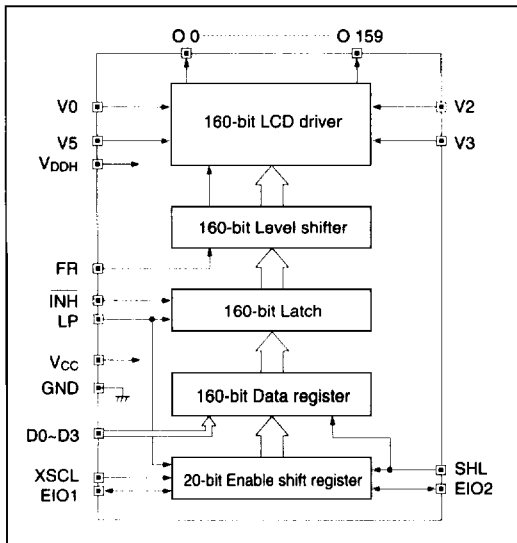
## ■ FEATURES

- Low-power high-speed CMOS technology
- 160-bit segment (column) driver
- High-speed data bus .... 4-bit (SED1742)  
8-bit (SED1744)
- Duty cycle ..... 1/100 to 1/500
- Adjustable LCD drive voltages
- Unbiased display off function
- Adjustable offset bias of the LCD according to VDDH and GND
- Shift clock frequency .... 12MHz max at VDD = 5V
- Ability to adjust offset bias of the LCD source from VDD
- Daisy chain enable support
- No enable signal by controller is required
- Wide range of LCD voltage .... 14 to 40V
- Supply voltage ..... 2.7 to 5.5V
- Package ..... TAB (ToA)  
Au bump (D1E)

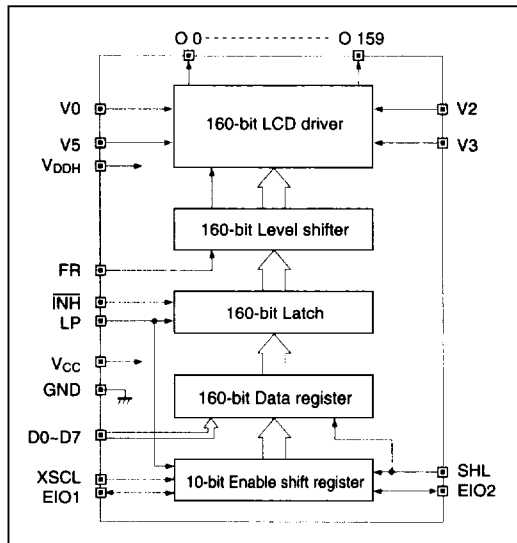
## ■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM  
● SED1742



● SED1744



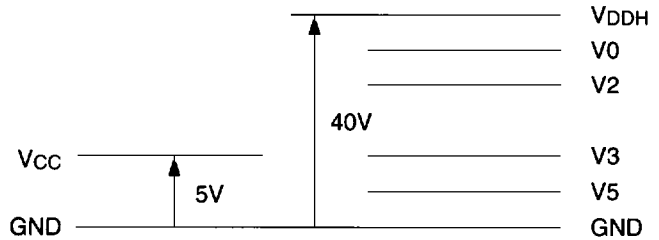
■ PIN DESCRIPTION

Pin Name	I/O	Function	Q'ty																																														
O0 to 159	—	LCD crystal segment (column) output The output varies at the LP trailing edge.	160																																														
D0 to D3 (SED1742)	I	Display data input	4																																														
D0 TO D7 (SED1744)	I	Display data input	8																																														
XSCL	I	Display data shift clock input (triggered at the trailing edge)	1																																														
LP	I	Display data latch pulse input (triggered at the trailing edge)	1																																														
EI01, EI02	I/O	Enable I/O. Set to input or output according to SHL input level. The output is reset at the LP input and set to "L" when a 160-bit data fetch is complete.	2																																														
SHL	I	<p>Shift direction selection and EIO terminal I/O control input (SED1744) When the data (a, b, .. g, h) (i, .. o, p) ... (s, t, .. y, z) are input in this sequence to the terminals (D0, D1, .. D7), the relation between the data and the segment output is as shown in the table below.</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th rowspan="2">SHL</th> <th colspan="6">O (SEG Output)</th> <th colspan="4">EIO</th> </tr> <tr> <th>159</th> <th>158</th> <th>157</th> <th>156</th> <th>155</th> <th>.....</th> <th>2</th> <th>1</th> <th>0</th> <th>1</th> <th>2</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>a</td> <td>b</td> <td>c</td> <td>d</td> <td>e</td> <td>.....</td> <td>x</td> <td>y</td> <td>z</td> <td>Output</td> <td>Input</td> </tr> <tr> <td>H</td> <td>z</td> <td>y</td> <td>x</td> <td>w</td> <td>v</td> <td>.....</td> <td>c</td> <td>b</td> <td>a</td> <td>Input</td> <td>Output</td> </tr> </tbody> </table> <p>Note: The relation between the data and the segment output is determined independently of the number of shift locks.</p>	SHL	O (SEG Output)						EIO				159	158	157	156	155	.....	2	1	0	1	2	L	a	b	c	d	e	.....	x	y	z	Output	Input	H	z	y	x	w	v	.....	c	b	a	Input	Output	1
SHL	O (SEG Output)						EIO																																										
	159	158	157	156	155	.....	2	1	0	1	2																																						
L	a	b	c	d	e	.....	x	y	z	Output	Input																																						
H	z	y	x	w	v	.....	c	b	a	Input	Output																																						
FR	I	Input of signal to AC electrify the liquid crystal drive output	1																																														
Vcc, GND	Power Source	Logic power source. GND: 0 V; Vcc: +3, +5 V	2																																														
V0, V2, V3, V5 VDDH	Power Source	Liquid crystal drive power source VDDH: +14 V to 40 V; GND: 0 V VDDH ≥ V0 > V2 ≥ 7/9 VDDH, 2/9 VDDH ≥ V3 > V5 ≥ GND	5																																														
INH	I	Forced blank input The signal forces the output to be set to V5 level at the "L" level.	1																																														
TEST		Test input normally fixed at "L" level.	1																																														

■ ELECTRICAL CHARACTERISTICS  
 ● Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage range (1)	V <sub>CC</sub>	-0.3 to +7.0	V
Supply voltage for LCD (1)	V <sub>DDH</sub>	-0.3 to +45.0	V
Supply voltage for LCD (2)	V <sub>0</sub> , V <sub>2</sub> , V <sub>3</sub> , V <sub>5</sub>	GND -0.3 to V <sub>DDH</sub> +0.3	V
Input voltage (4)	V <sub>I</sub>	GND -0.3 to V <sub>CC</sub> +0.3	V
Output voltage	V <sub>O</sub>	GND -0.3 to V <sub>CC</sub> +0.3	V
EIO output current	IO1	20	mA
Operating temperature	T <sub>opr</sub>	-20 to +75	°C
Storage temperature 1 (3)	T <sub>stg1</sub>	-65 to +150	°C
Storage temperature 2 (3)	T <sub>stg2</sub>	-55 to +150	°C
Logic supply	V <sub>CC</sub>	3*	V
Segment driver supply voltage range	V <sub>DDH</sub>	14 to 28*	V

\* T<sub>a</sub> = 25°C



- Notes:
1. The voltage is based at GND = 0 V
  2. Voltage V<sub>0</sub>, V<sub>2</sub>, V<sub>3</sub> and V<sub>5</sub> should satisfy the condition: V<sub>DDH</sub> ≥ V<sub>0</sub> ≥ V<sub>2</sub> ≥ V<sub>3</sub> ≥ V<sub>5</sub> ≥ GND.
  3. The storage temperature 1 is specified for a single chip and the storage temperature 2 is for TCP mounting.
  4. **WARNING:** The LSI may be externally broken if the logic system power source floats or decreases below V<sub>CC</sub> = 2.9 V while voltage is applied to the liquid crystal drive system power source. Special care should be taken for the power source sequence when turning the system power on and off.

● DC Electrical Characteristics

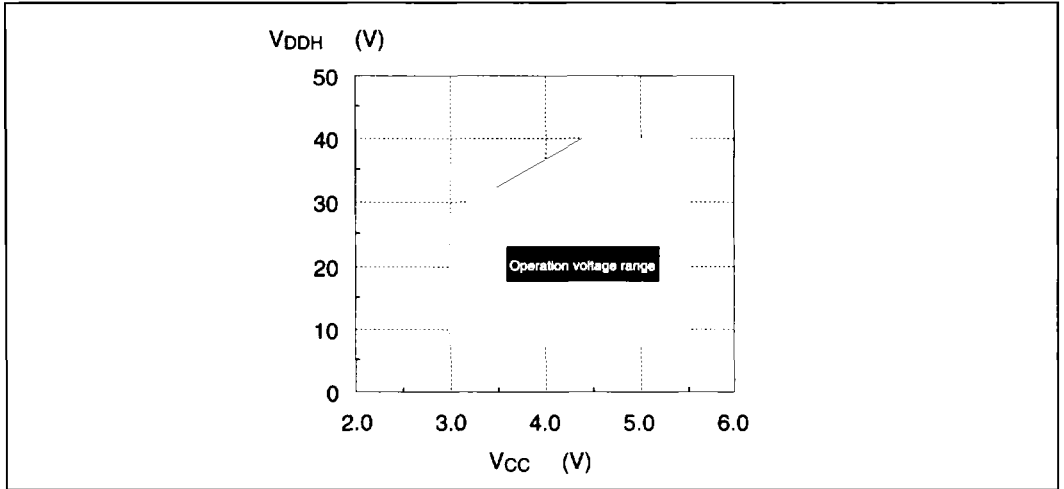
(Unless stated otherwise GND=V5=0V, Vcc= +5.0V±10%, Ta = -20 to 75°C)

Parameter	Symbol	Condition		Terminal	Min	Typ	Max	Unit
Logic supply voltage (1)	VCC			VCC	3.0	5.0	5.5	V
Operation voltage recommended	VDDH			VDDH	14.0	—	40.0	V
Segment driver input supply voltage	VDDH	Function		VDDH	8.0	—	—	V
Segment driver input supply voltage (2)	V0	Value recommended		V0	VDDH-2.5	—	VDDH	V
Segment driver input supply voltage (2)	V2	Value recommended		V2	7/9VDDH	—	—	V
Segment driver input supply voltage (2)	V3, V5	Value recommended		V3, V5	GND	—	2/9VDDH	V
High-level input voltage	VIH	VCC = 3.0 to 5.5 V		EIO1, EIO2, D0 to D3: SED1742 D0 to D7: SED1744 XSCL, LP, SHL, FR, INH	0.8VCC	—	—	V
Low-level input voltage	VIL				—	—	0.2VCC	V
High-level output voltage	VOH	VCC = 3 to 5.5 V	IOH = -0.6 mA	EIO1, EIO2	VCC-0.4	—	—	V
Low-level output voltage	VOL		IOL = 0.6 mA		—	—	0.4	V
Low-level input leakage current	ILI	GND ≤ VIN ≤ VCC		D0 to D3: SED1742 D0 to D7: SED1744 LP, FR, XSCL, SHL, INH	—	—	2.0	μA
Input: leakage current output	ILI/O	GND ≤ VIN ≤ VCC		EIO1, EIO2	—	—	5.0	μA
Static current	IGND	VDDH = 14.0 to 40.0 V VIH = VCC, VIL = GND		GND	—	—	25	μA
Output resistance	RSEG	ΔVon = 0.5V condition recommended	VDDH=+30.0V	O0 to O159	—	0.9	2.5	kΩ
			VDDH=+20.0V		—	1.0	3.0	
Average Operation current consumed (1)	ICC	VCC = +5.0 V, VIH = VCC, VIL = GND, fXSCL = 5.38 MHz, fLP = 33.6 kHz, fFR = 70 Hz Input data: Display checked, No load ----- VCC = +3.0 V; Other conditions: same as VCC = +5.0 V		VCC	—	0.4	1.2	mA
					—	0.2	0.6	
Average Operation current consumed (2)	IDDH	VDDH = V0 = +30.0 V, VCC = +5.0 V, V3 = +4.0 V, V2 = +26.0 V, V5 = 0.0 V; Other conditions: same as VCC = +5.0 V		VDDH	—	0.5	1.5	mA
Input capacitance	CI	Freq.=1 MHz, Ta = 25°C Single chip		D0 to D3: SED1742 D0 to D7: SED1744 LP, FR, XSCL, SHL, INH	—	—	8	pF
I/O terminal capacity	CI/O			EIO1, EIO2	—	—	15	pF

- Notes: 1. The voltage is based at GND=0V.  
 2. Voltage V0, V2, and V3 should satisfy the condition: VDDH>V0>V2>V3>V5>GND

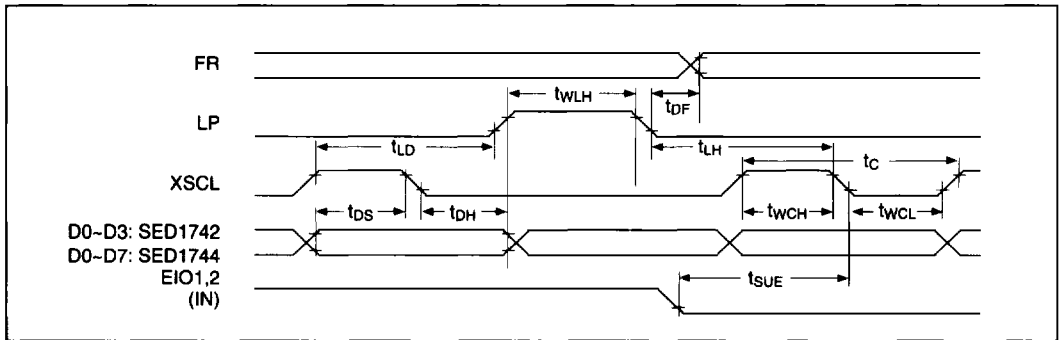
● Operating Voltage Range  $V_{CC}$ – $V_{DDH}$

The maximum LCD supply voltage,  $V_{DDH}$  depends on  $V_{CC}$  as shown in the following figure. Specify the  $V_{DDH}$  voltage within the  $V_{CC}$ – $V_{DDH}$  operation.



● AC Electrical Characteristics

○ Input Timing Characteristics



Note: Adjust the timing of the LP pulse input at high-speed operation, excluding one clock of XSCl.

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $T_a = -20$  to  $75^\circ\text{C}$ )

Parameter	Symbol	Condition	Min	Typ	Max	Unit
XSCl cycle	$t_c$		83	—	—	ns
XSCl high-level pulse width	$t_{wCH}$		30	—	—	ns
XSCl low-level pulse width	$t_{wCL}$		30	—	—	ns
Data setup time	$t_{DS}$		30	—	—	ns
Data hold time	$t_{DH}$		30	—	—	ns
XSCl → LP rise time	$t_{LD}$		–5	—	—	ns
LP → XSCl breaking time	$t_{LH}$		60	—	—	ns
LP high-level pulse width (1)	$t_{WLH}$		45	—	—	ns
FR delay allowance time	$t_{DF}$		–300	—	300	ns
EIO setup time	$t_{SUE}$		35	—	—	ns

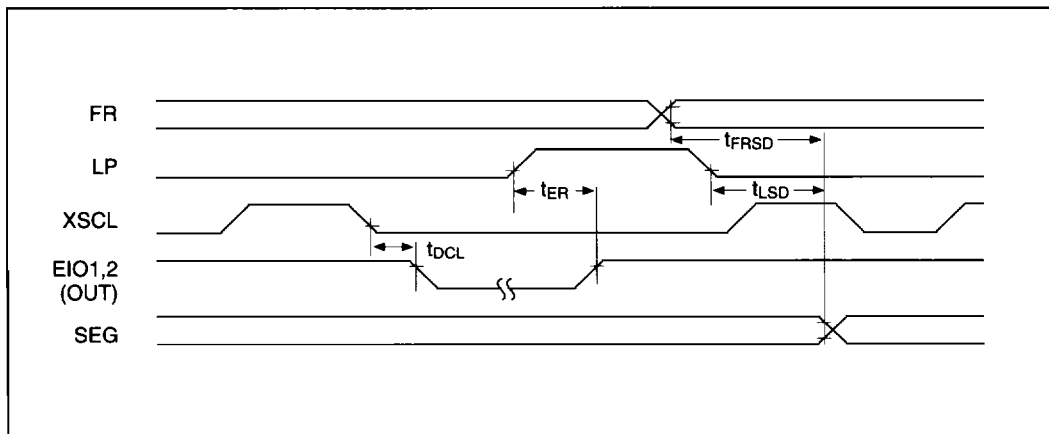
Note:  $t_{WLH}$  defines the time duration when the LP is “H” and the XSCl is “L”.

(VCC = 3.0 to 4.5 V, Ta = -20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
XSCL cycle	tc		125	—	—	ns
XSCL high-level pulse width	twCH		50	—	—	ns
XSCL low-level pulse width	twCL		50	—	—	ns
Data setup time	tdS		50	—	—	ns
Data hold time	tdH		30	—	—	ns
XSCL → LP rise time	tlD		0	—	—	ns
LP → XSCL breaking time	tlH		120	—	—	ns
LP high-level pulse width (1)	twLH		90	—	—	ns
FR delay allowance time	tdF		-600	—	600	ns
EIO setup time	tsUE		70	—	—	ns

Note: twLH defines the time duration when the LP is "H" and the XSCL is "L"

o Output Timing Characteristics



(VCC = +5.0 V ±10%, VDDH = 14.0 to 40.0 V)

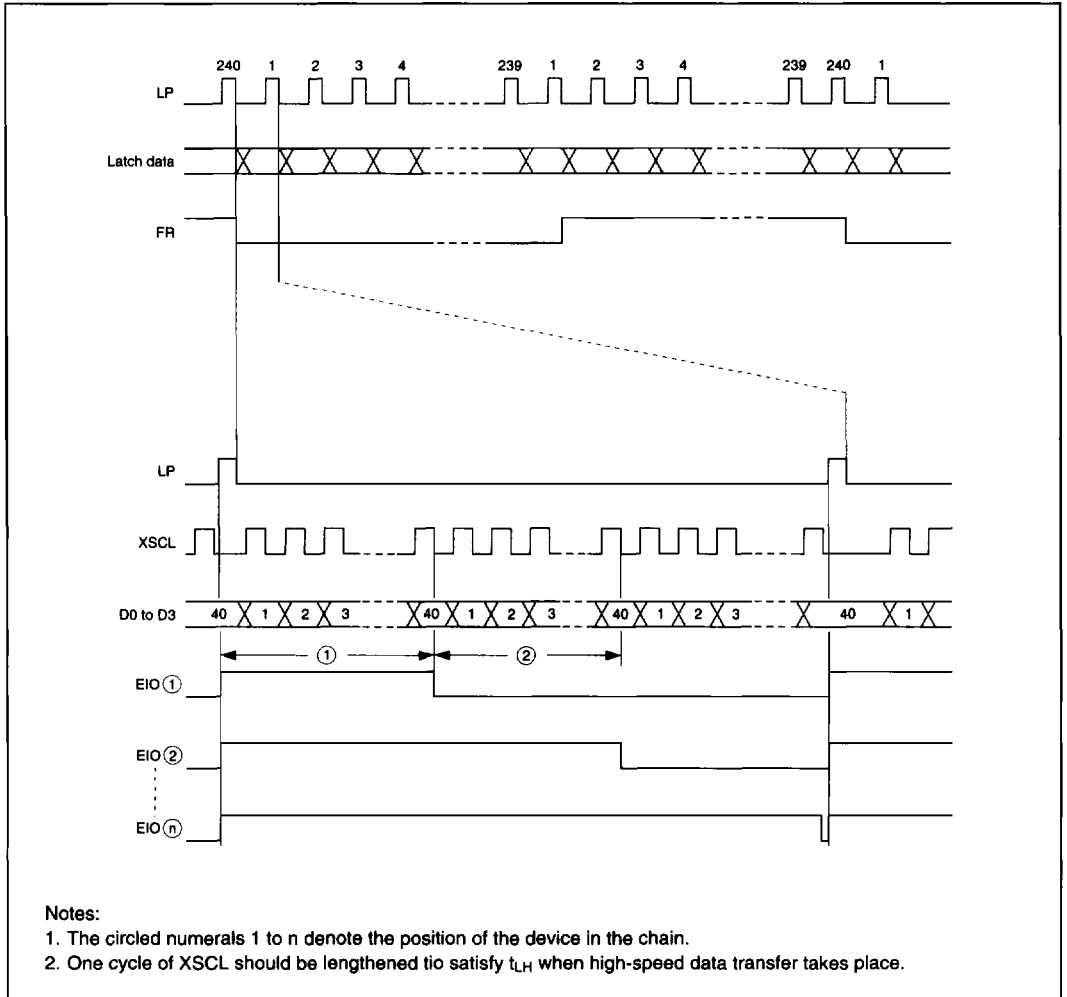
Parameter	Symbol	Condition	Min	Typ	Max	Unit
EIO reset time	tER	CL = 15 pF (EIO)	—	—	120	ns
EIO output delay time	tdCL		—	—	45	ns
LP → SEG output delay time	tlSD	CL = 100 pF (On)	—	—	200	ns
FR → SEG output delay time	tFRSD		—	—	400	ns

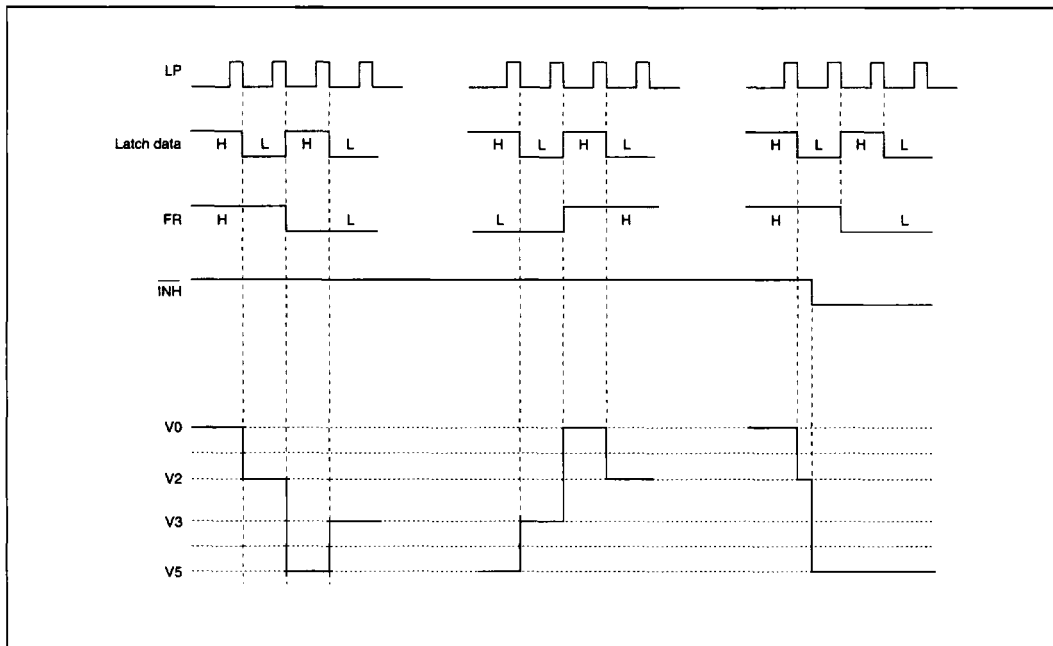
(VCC = 3.0 to 4.5 V, VDDH = 14.0 to 28.0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
EIO reset time	tER	CL = 15 pF (EIO)	—	—	240	ns
EIO output delay time	tdCL		—	—	72	ns
LP → SEG output delay time	tlSD	CL = 100 pF (On)	—	—	400	ns
FR → SEG output delay time	tFRSD		—	—	800	ns

● Timing Diagrams

- 1/240 Duty Cycle





■ **FUNCTIONAL DESCRIPTION**

● **Enable Shift Register**

The enable shift register is a bi-directional shift register, where the shift direction is selected by SHL. SHL is also used to latch data from the data bus into the data register. The effect of SHL on the shift direction and on the input data sequence is shown in the following table.

**Data Sequence and Shift Direction**

SHL	LCD Outputs							Shift Direction	
	O159	O158	O157	...	O2	O1	O0	EIO1	EIO2
L	a	b	c	...	x	y	z	Output	Input
H	z	y	x	...	c	b	a	Input	Output

When the enable signal is inactive, the SED1742 is in standby mode with the internal clock stopped and the data bus held LOW. When multiple SED1742s are used, the enable input of the first device should be connected to ground and the enable input of each successive device should be connected to the enable output of the preceding device.

When 160 data bits have been latched into the SED1742, the enable output edge goes LOW, eliminating the need for an external control circuit.

● **Data Register**

The data register converts the input data into parallel display driver data under the control of the enable shift register.

■ **APPLICATION NOTES**

● **Voltage Levels**

The recommended method of generating the LCD drive voltages, V0 to V5, is with a voltage divider between VDDH and VGND, buffered with voltage followers.

The lower drive level, V5, is not necessarily at VGND, and separate pins are used for the voltage levels when op-amps are used. A maximum voltage differential between V5 and VGND of 2.5V is recommended since the driver efficiency decreases as the differential increases. Connect V5 to GND when not using op-amps.

The resistances of the voltage divider resistors should be as low as possible and within power supply constraints.

Note that fluctuations in IODH can cause dips in the VDDH supply. The device will be damaged if the voltage dips below the point where the relationship  $V_{DDH}(V0) \geq V2 \geq V3 \geq V5 \geq VGND$  breaks down. A stabilized power supply may be required when using the resistor network.

● **Data Latch**

The data latch latches the data into the level shifter on the falling edge of LP.

● **Level Shifter**

The level shifter converts the logic-level signals from the latch into the LCD driver input voltage levels.

● **LCD Drivers**

The LCD drivers generate the AC LCD drive waveforms. The output voltages are determined by the polarity of the FR signal, as shown in the following table.

**Driver Output Voltage**

$\overline{iNH}$	Input Data	FR	Output Voltage
H	H	H	V0 (VDDH)
		L	V5
	L	H	V2
		L	V3
L	X	X	V5

x = don't care

- **Power-Up and Power-Down Precautions**

As the driver circuitry operates at high voltage, care should be taken when applying and removing power to the SED1742 to prevent damage. If the driver supply is applied when the logic supply is either not connected or below 2.9V, excess current will flow into the SED1742 and damage the device. Normal operation is guaranteed if the correct power-up and power-down sequences are followed.

**Power-Up Sequence:**

Power should be applied to Vcc before, or at the same time as, power is applied to the driver circuitry.

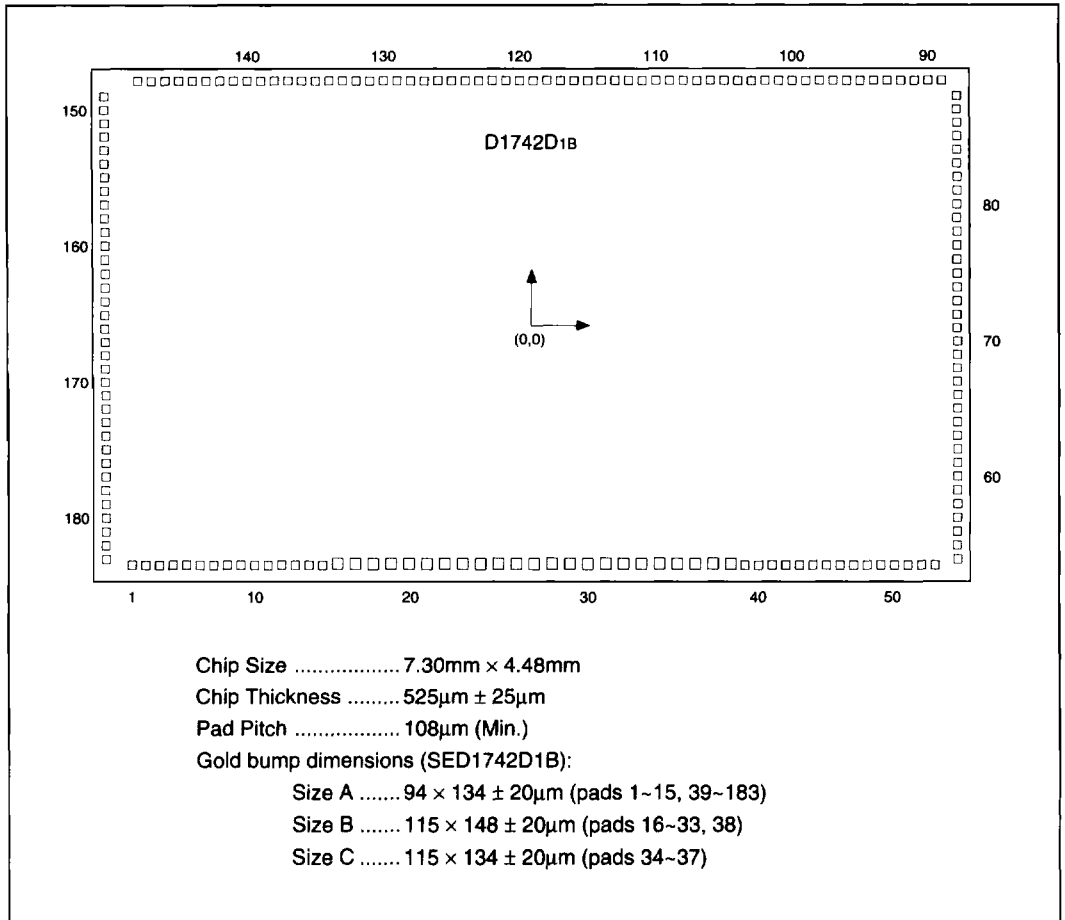
**Power-Down Sequence:**

Power should be removed from Vcc after, or at the same time as, power is removed from the driver circuitry.

The SED1742 can also be damaged if the LCD output drivers start operating before the driver supplies stabilize. INH should be held LOW to hold the driver outputs at V5 until the driver supplies have stabilized.

As an extra precaution, insert a fast-blow fuse in series with the driver supply.

■ PAD LAYOUT FOR SED1742D1B



unit: μm

■ PAD COORDINATES

Pad		Coordinates	
No.	Name	X	Y
1	O145	-3228	-2064
2	O146	-3120	-2064
3	O147	-3012	-2064
4	O148	-2903	-2064
5	O149	-2795	-2064
6	O150	-2687	-2064
7	O151	-2578	-2064
8	O152	-2470	-2064
9	O153	-2362	-2064
10	O154	-2253	-2064
11	O155	-2145	-2064
12	O156	-2037	-2064

Pad		Coordinates	
No.	Name	X	Y
13	O157	-1929	-2064
14	O158	-1820	-2064
15	O159	-1712	-2064
16	EIO2	-1550	-2058
17	EIO1	-1417	-2058
18	GND	-1284	-2058
19	D0	-1151	-2058
20	D1	-1018	-2058
21	D2	-885	-2058
22	D3	-752	-2058
23	NC	-619	-2058
24	NC	-486	-2058

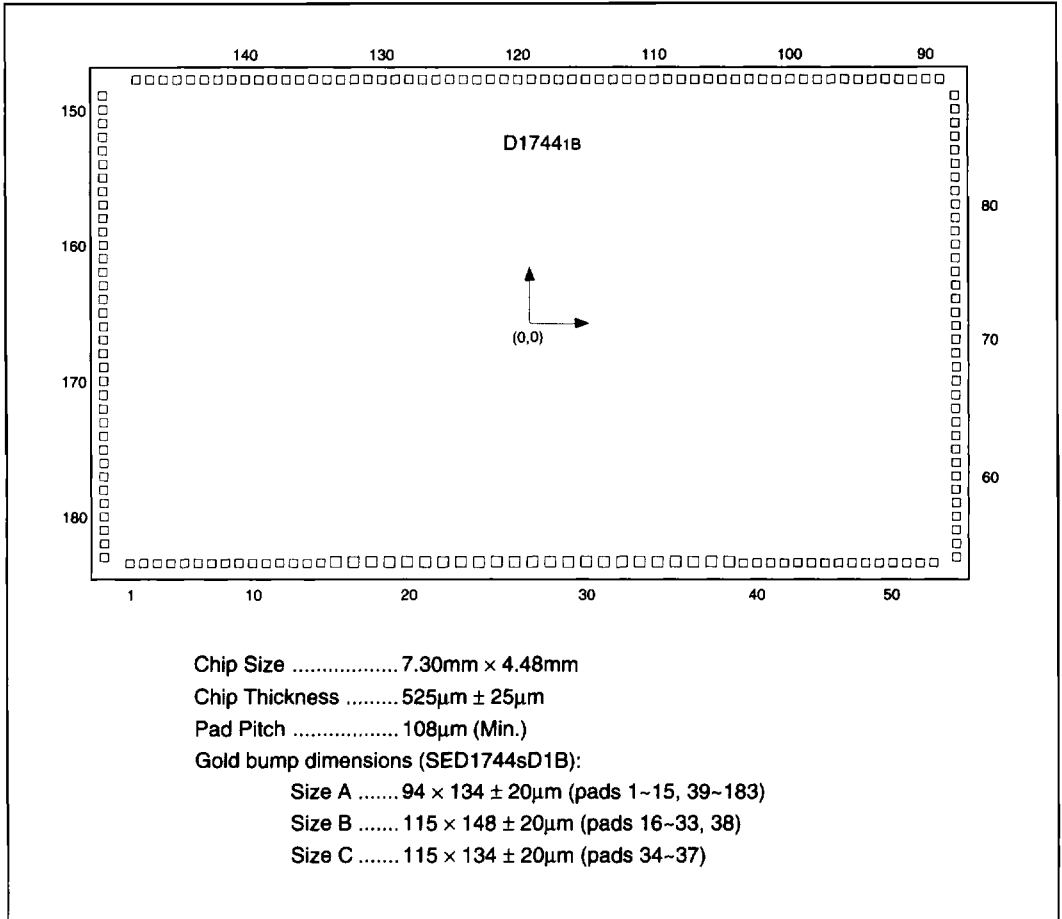
Pad		Coordinates	
No.	Name	X	Y
25	NC	-353	-2058
26	NC	-220	-2058
27	SHL	-87	-2058
28	XSCL	46	-2058
29	TEST	179	-2058
30	INH	312	-2058
31	LP	445	-2058
32	V <sub>CC</sub>	578	-2058
33	FR	711	-2058
34	V5	872	-2026
35	V3	1034	-2026
36	V2	1195	-2026

Pad		Coordinates	
No.	Name	X	Y
37	V0	1357	-2026
38	VDDH	1550	-2058
39	O0	1712	-2064
40	O1	1820	-2064
41	O2	1929	-2064
42	O3	2037	-2064
43	O4	2145	-2064
44	O5	2253	-2064
45	O6	2362	-2064
46	O7	2470	-2064
47	O8	2578	-2064
48	O9	2687	-2064
49	O10	2795	-2064
50	O11	2903	-2064
51	O12	3012	-2064
52	O13	3120	-2064
53	O14	3228	-2064
54	O15	3474	-1841
55	O16	3474	-1733
56	O17	3474	-1625
57	O18	3474	-1516
58	O19	3474	-1408
59	O20	3474	-1300
60	O21	3474	-1191
61	O22	3474	-1083
62	O23	3474	-975
63	O24	3474	-866
64	O25	3474	-758
65	O26	3474	-650
66	O27	3474	-542
67	O28	3474	-433
68	O29	3474	-325
69	O30	3474	-217
70	O31	3474	-108
71	O32	3474	0
72	O33	3474	108
73	O34	3474	217
74	O35	3474	325
75	O36	3474	433
76	O37	3474	542
77	O38	3474	650
78	O39	3474	758
79	O40	3474	866
80	O41	3474	975
81	O42	3474	1083
82	O43	3474	1191
83	O44	3474	1300
84	O45	3474	1408
85	O46	3474	1516

Pad		Coordinates	
No.	Name	X	Y
86	O47	3474	1625
87	O48	3474	1733
88	O49	3474	1841
89	O50	3195	2064
90	O51	3087	2064
91	O52	2978	2064
92	O53	2870	2064
93	O54	2762	2064
94	O55	2553	2064
95	O56	2545	2064
96	O57	2437	2064
97	O58	2328	2064
98	O59	2220	2064
99	O60	2112	2064
100	O61	2004	2064
101	O62	1895	2064
102	O63	1787	2064
103	O64	1679	2064
104	O65	1570	2064
105	O66	1462	2064
106	O67	1354	2064
107	O68	1245	2064
108	O69	1137	2064
109	O70	1029	2064
110	O71	921	2064
111	O72	812	2064
112	O73	704	2064
113	O74	596	2064
114	O75	487	2064
115	O76	379	2064
116	O77	271	2064
117	O78	162	2064
118	O79	54	2064
119	O80	-54	2064
120	O81	-162	2064
121	O82	-271	2064
122	O83	-379	2064
123	O84	-487	2064
124	O85	-596	2064
125	O86	-704	2064
126	O87	-812	2064
127	O88	-921	2064
128	O89	-1029	2064
129	O90	-1137	2064
130	O91	-1245	2064
131	O92	-1354	2064
132	O93	-1462	2064
133	O94	-1570	2064
134	O95	-1679	2064

Pad		Coordinates	
No.	Name	X	Y
135	O96	-1787	2064
136	O97	-1895	2064
137	O98	-2004	2064
138	O99	-2112	2064
139	O100	-2220	2064
140	O101	-2328	2064
141	O102	-2437	2064
142	O103	-2545	2064
143	O104	-2653	2064
144	O105	-2762	2064
145	O106	-2870	2064
146	O107	-2978	2064
147	O108	-3087	2064
148	O109	-3195	2064
149	O110	-3474	1841
150	O111	-3474	1733
151	O112	-3474	1625
152	O113	-3474	1516
153	O114	-3474	1408
154	O115	-3474	1300
155	O116	-3474	1191
156	O117	-3474	1083
157	O118	-3474	975
158	O119	-3474	866
159	O120	-3474	758
160	O121	-3474	650
161	O122	-3474	542
162	O123	-3474	433
163	O124	-3474	325
164	O125	-3474	217
165	O126	-3474	108
166	O127	-3474	0
167	O128	-3474	-108
168	O129	-3474	-217
169	O130	-3474	-325
170	O131	-3474	-433
171	O132	-3474	-542
172	O133	-3474	-650
173	O134	-3474	-758
174	O135	-3474	-866
175	O136	-3474	-975
176	O137	-3474	-1083
177	O138	-3474	-1191
178	O139	-3474	-1300
179	O140	-3474	-1408
180	O141	-3474	-1516
181	O142	-3474	-1625
182	O143	-3474	-1733
183	O144	-3474	-1841

■ PAD LAYOUT FOR SED1744D<sub>1B</sub>



unit: μm

■ PAD COORDINATES

Pad		Coordinates	
No.	Name	X	Y
1	O145	-3228	-2064
2	O146	-3120	-2064
3	O147	-3012	-2064
4	O148	-2903	-2064
5	O149	-2795	-2064
6	O150	-2687	-2064
7	O151	-2578	-2064
8	O152	-2470	-2064
9	O153	-2362	-2064
10	O154	-2253	-2064
11	O155	-2145	-2064
12	O156	-2037	-2064

Pad		Coordinates	
No.	Name	X	Y
13	O157	-1929	-2064
14	O158	-1820	-2064
15	O159	-1712	-2064
16	EIO2	-1550	-2058
17	EIO1	-1417	-2058
18	GND	-1284	-2058
19	D0	-1151	-2058
20	D1	-1018	-2058
21	D2	-885	-2058
22	D3	-752	-2058
23	D4	-619	-2058
24	D5	-486	-2058

Pad		Coordinates	
No.	Name	X	Y
25	D6	-353	-2058
26	D7	-220	-2058
27	SHL	-87	-2058
28	XSC1	46	-2058
29	TEST	179	-2058
30	INH	312	-2058
31	LP	445	-2058
32	V <sub>CC</sub>	578	-2058
33	FR	711	-2058
34	V5	872	-2026
35	V3	1034	-2026
36	V2	1195	-2026

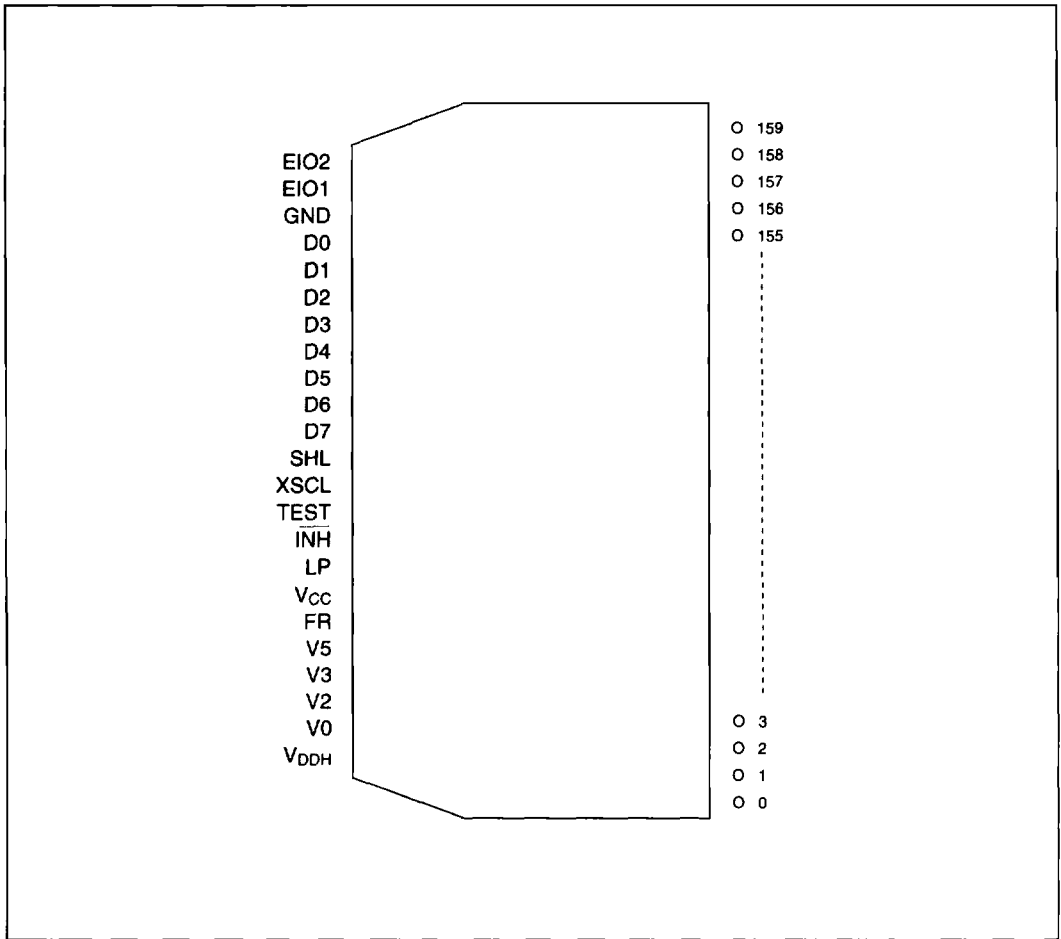
Pad		Coordinates	
No.	Name	X	Y
37	V0	1357	-2026
38	VDDH	1550	-2058
39	O0	1712	-2064
40	O1	1820	-2064
41	O2	1929	-2064
42	O3	2037	-2064
43	O4	2145	-2064
44	O5	2253	-2064
45	O6	2362	-2064
46	O7	2470	-2064
47	O8	2578	-2064
48	O9	2687	-2064
49	O10	2795	-2064
50	O11	2903	-2064
51	O12	3012	-2064
52	O13	3120	-2064
53	O14	3228	-2064
54	O15	3474	-1841
55	O16	3474	-1733
56	O17	3474	-1625
57	O18	3474	-1516
58	O19	3474	-1408
59	O20	3474	-1300
60	O21	3474	-1191
61	O22	3474	-1083
62	O23	3474	-975
63	O24	3474	-866
64	O25	3474	-758
65	O26	3474	-650
66	O27	3474	-542
67	O28	3474	-433
68	O29	3474	-325
69	O30	3474	-217
70	O31	3474	-108
71	O32	3474	0
72	O33	3474	108
73	O34	3474	217
74	O35	3474	325
75	O36	3474	433
76	O37	3474	542
77	O38	3474	650
78	O39	3474	758
79	O40	3474	866
80	O41	3474	975
81	O42	3474	1083
82	O43	3474	1191
83	O44	3474	1300
84	O45	3474	1408
85	O46	3474	1516

Pad		Coordinates	
No.	Name	X	Y
86	O47	3474	1625
87	O48	3474	1733
88	O49	3474	1841
89	O50	3195	2064
90	O51	3087	2064
91	O52	2978	2064
92	O53	2870	2064
93	O54	2762	2064
94	O55	2553	2064
95	O56	2545	2064
96	O57	2437	2064
97	O58	2328	2064
98	O59	2220	2064
99	O60	2112	2064
100	O61	2004	2064
101	O62	1895	2064
102	O63	1787	2064
103	O64	1679	2064
104	O65	1570	2064
105	O66	1462	2064
106	O67	1354	2064
107	O68	1245	2064
108	O69	1137	2064
109	O70	1029	2064
110	O71	921	2064
111	O72	812	2064
112	O73	704	2064
113	O74	596	2064
114	O75	487	2064
115	O76	379	2064
116	O77	271	2064
117	O78	162	2064
118	O79	54	2064
119	O80	-54	2064
120	O81	-162	2064
121	O82	-271	2064
122	O83	-379	2064
123	O84	-487	2064
124	O85	-596	2064
125	O86	-704	2064
126	O87	-812	2064
127	O88	-921	2064
128	O89	-1029	2064
129	O90	-1137	2064
130	O91	-1245	2064
131	O92	-1354	2064
132	O93	-1462	2064
133	O94	-1570	2064
134	O95	-1679	2064

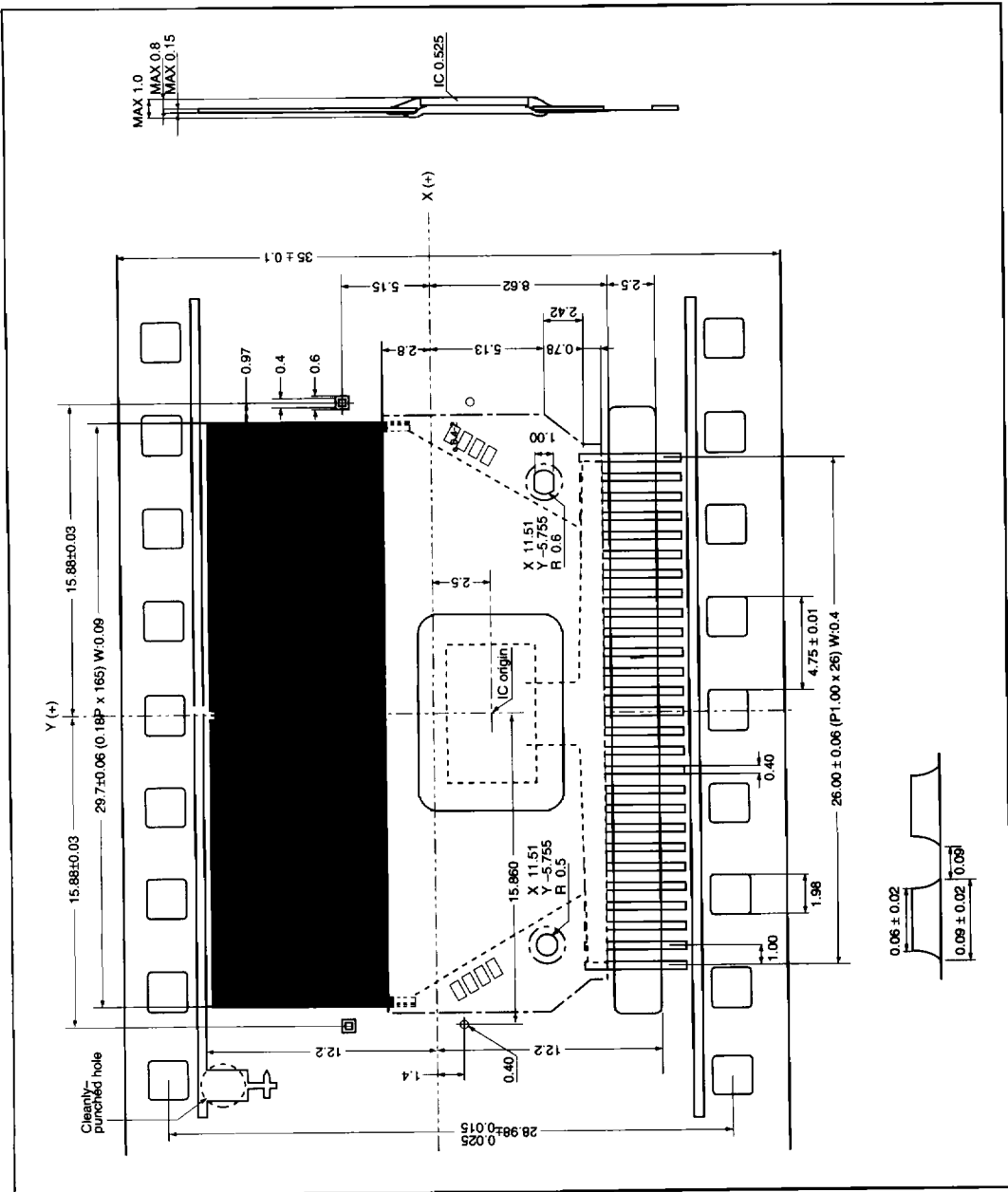
Pad		Coordinates	
No.	Name	X	Y
135	O96	-1787	2064
136	O97	-1895	2064
137	O98	-2004	2064
138	O99	-2112	2064
139	O100	-2220	2064
140	O101	-2328	2064
141	O102	-2437	2064
142	O103	-2545	2064
143	O104	-2653	2064
144	O105	-2762	2064
145	O106	-2870	2064
146	O107	-2978	2064
147	O108	-3087	2064
148	O109	-3195	2064
149	O110	-3474	1841
150	O111	-3474	1733
151	O112	-3474	1625
152	O113	-3474	1516
153	O114	-3474	1408
154	O115	-3474	1300
155	O116	-3474	1191
156	O117	-3474	1083
157	O118	-3474	975
158	O119	-3474	866
159	O120	-3474	758
160	O121	-3474	650
161	O122	-3474	542
162	O123	-3474	433
163	O124	-3474	325
164	O125	-3474	217
165	O126	-3474	108
166	O127	-3474	0
167	O128	-3474	-108
168	O129	-3474	-217
169	O130	-3474	-325
170	O131	-3474	-433
171	O132	-3474	-542
172	O133	-3474	-650
173	O134	-3474	-758
174	O135	-3474	-866
175	O136	-3474	-975
176	O137	-3474	-1083
177	O138	-3474	-1191
178	O139	-3474	-1300
179	O140	-3474	-1408
180	O141	-3474	-1516
181	O142	-3474	-1625
182	O143	-3474	-1733
183	O144	-3474	-1841

■ SED1742 TAPE-CARRIER PACKAGE

● Tape-Carrier Pinout

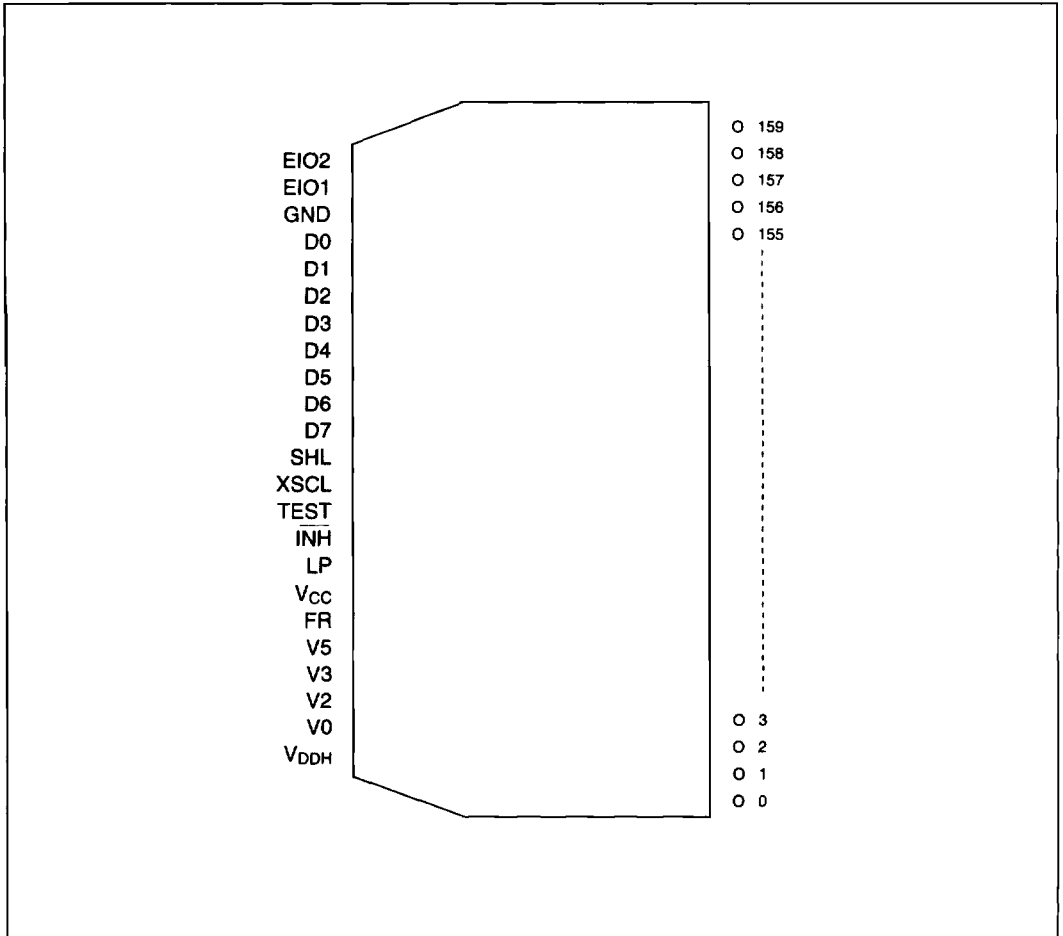


● Tape-Carrier Dimensions



■ SED1744 TAPE-CARRIER PACKAGE

● Tape-Carrier Pinout



● Tape-Carrier Dimensions

