

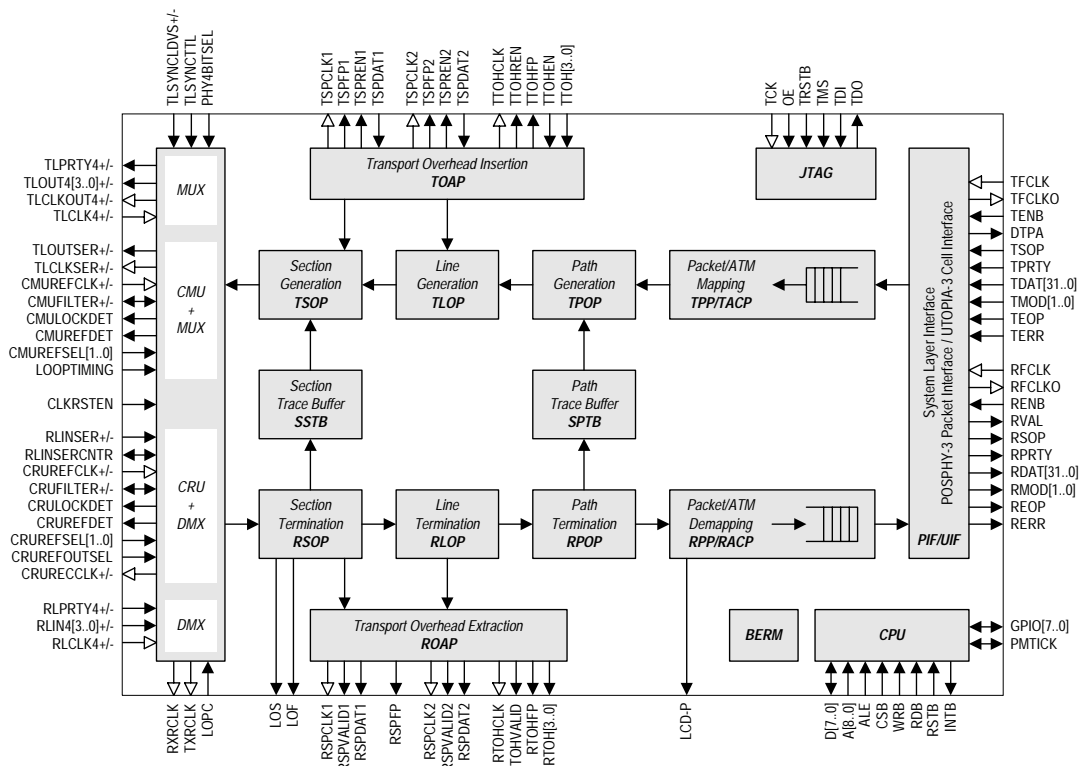
Preliminary Datasheet SC9142

STS-48c Packet/ATM Over SONET/SDH Device With Integrated Mux/Demux and Clock and Data Recovery

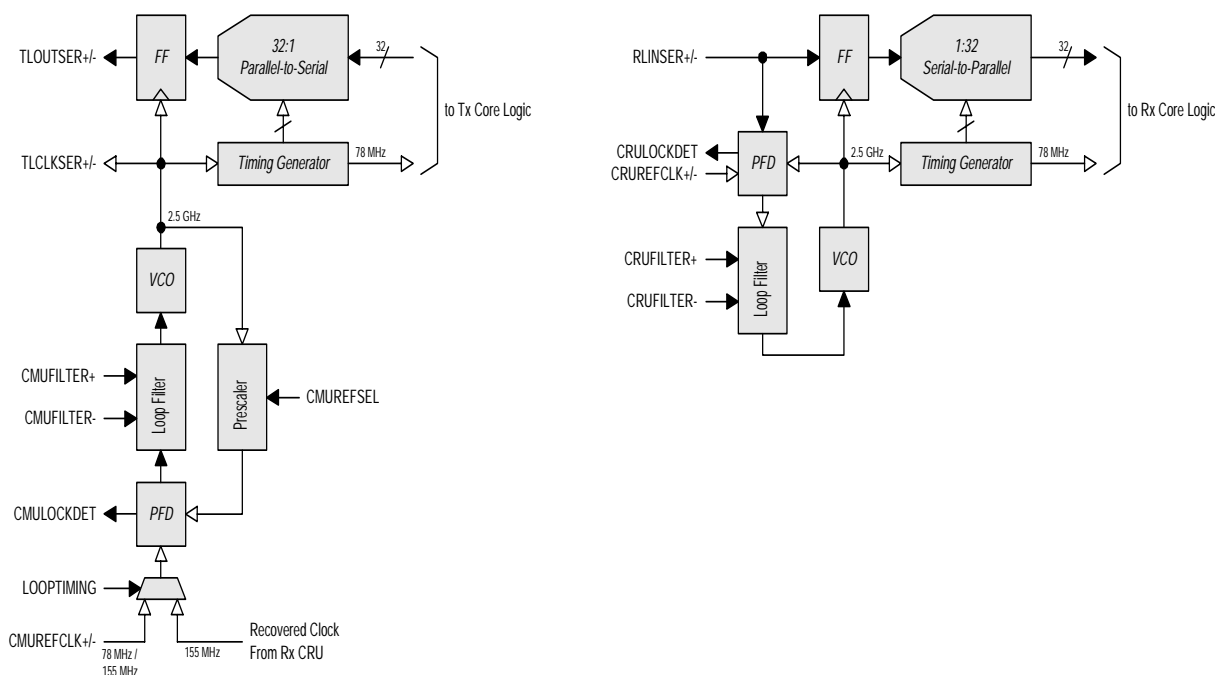
Features

- Dual Mode STS-48c/STM-16c to Packet/ATM Framing Device for User Network Interface and Network Node Interface Applications
- Integrated 2.5 Gbps Clock and Data Recovery and Serial Clock and Data Output with Power-down Mode.
- Selectable Reference Clock Frequencies and Sources for Transmit and Receive datapaths
- Terminates and Generates Full SONET/SDH Section, Line, and Path Layers
- Dedicated Ports for Section/Line Overhead Access (Extraction/Insertion)
- Extensive SONET/Packet/Cell Performance Monitoring Features
- Programmable Packet/Cell Filtering and Discarding Functionalities
- Industry Compliant Drop Side Packet/Cell Interface for Single-PHY Applications
- 4-bit OIF Compliant Line Interface to be used for STS-192 applications
- +1.8V and +3.3V Power Supply
- Compliant with SONET and SDH Requirements as Stated in ANSI T1.105, Bellcore GR-253-CORE and ITU-T G.707 Documents
- Compliant with PPP in HDLC-like Framing as Defined in IETF RFC 1619/1661/1662

VSC9142 Block Diagram



Integrated PHY Block Diagram



Functional Overview

The VSC9142 is a dual mode SONET/SDH to Packet/ATM framing device that integrates the physical layer components of 2.5 Gbps clock and data recovery and serialization/deserialization into a single device. In the Packet over SONET (POS) mode, this device can be used in equipment interconnecting IP/PPP/HDLC data over public or private SONET/SDH networks. Similarly, in the ATM over SONET (ATM) mode, this device can be used in equipment interconnecting ATM switches. In addition, the VSC9142 can be used in various applications involving LAPS (X.85/Y.1321) and Ethernet over SONET/SDH protocols.

Features of the VSC9142 includes: full insertion/extraction of the transport overhead, bit error rate and extensive SONET/packet/cell performance monitoring, packet/cell filtering and discarding functionalities, JTAG TAP controller, and an 8-bit CPU interface with 8 general purpose I/O ports.

The high-speed component provides data and clock in the transmit direction, and selectable reference clock frequencies and sources for both the transmit and receive directions. The VSC9142 can facilitate both internal and external looptiming applications and also provides a 4-bit LVDS interface in both transmit and receive direction for use in STS-192 applications. When using the 4-bit interface, the serializing/deserializing blocks of the VSC9142 can be shut down for power savings.

This highly integrated device provides a complete low-power physical layer solution on a single chip for Packet/ATM over SONET/SDH at the STS-48 rate.

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Line Interface

- A parity bit, programmable for even/odd parity, is provided each for the incoming and outgoing datapaths.
- A reference clock output derived from the receive clock input can be programmed to be 8kHz, 19MHz, 38MHz, or 78MHz frequency locked to the receive clock.
- A reference clock output derived from the transmit clock input can be programmed to be 8kHz, 19MHz, 38MHz, or 78MHz frequency locked to the transmit clock.
- A Loss of Optical Carrier (LOPC) input signal is provided for monitoring and alarm purposes.
- Interface select (PHY4BITSEL) which selects between the 4-bit and serial interfaces.
- Only one interface can be used at any time either the serial interface or the 4-bit LVDS interface.
- Power Down Option for the unused interface which is done by connecting the positive power supply pins of the unused block into GND .
- Selectable CMU Reference Clock for the serial interface
- Selectable CRU Reference Clock for the serial interface .
- CMU Loss Of Lock Indicator for the serial interface.
- CRU Loss Of Lock Indicator for the serial interface.
- CMU no Reference Clock Indicator for the serial interface.
- CRU no Reference Clock Indicator for the serial interface.
- On chip Mux in the receive direction that selects either the recovered CRU clock or an external clock reference (under loss of serial input data) and sent it to the CRU clock output.
- Internal and external looptiming are available between the CRU and the CMU.

Receive Section Overhead Processor (RSOP)

- Two mechanisms for frame alignment are provided. One is based on searching for A1/A2 framing patterns and the other uses an external frame pulse (RLFP). The latter is intended for STS-192 applications.
- 12/24/48-bit A1/A2 framing patterns are supported.
- Out Of Frame (OOF) and Loss Of Frame (LOF) alarm condition are detected.
- The incoming data stream is optionally descrambled using the generating polynomial $1 + x^6 + x^7$ with a sequence length of 127.
- Section BIP-8 (B1) errors are detected and accumulated. Both individual and block mode accumulation of B1 error indications are supported.
- The incoming data stream, before descrambling, is monitored for absence of transitions or “all-zero patterns”. The Loss Of Signal (LOS) detection and termination criterias are programmable.

- It is possible to force insertion of all “1” in the data stream, except for the Section overhead. The Line AIS (AIS-L) condition may be automatically inserted in case of LOS, LOF, or Loss of Optical Carrier (LOPC) alarm events.
- It is possible to extract the entire Section overhead through the Receive Overhead Access Port (ROAP).
- The J0, E1, F1, and D1-D3 bytes can be extracted from the Section overhead and inserted into bytes on the special purpose ports of the ROAP.

Receive Line Overhead Processor (RLOP)

- The Line Remote Defect Indication (RDI-L) and Line Alarm Indication Signal (AIS-L) alarms carried in the K2 byte are extracted and filtered. The filter constants are programmable.
- Line BIP-384 errors carried in the B2 bytes are detected and accumulated. Both individual and block mode accumulation of B2 errors are supported.
- Line REI error indications carried in the M1 byte are accumulated. Both individual and block mode accumulation of M1 error indications are supported.
- The Synchronization Status carried in the S1 byte is extracted and filtered. Unstable and mismatch alarms are supported. The filter constants are programmable.
- The Automatic Protection Switching (APS) bytes, K1 and K2, are extracted and filtered. Unstable alarm is supported. The filter constants are programmable.
- It is possible to extract the entire Line overhead through the ROAP.
- The D4-D12, S1, E2, K1-K2 bytes can be extracted from the Line overhead and inserted into bytes on the special purpose ports of the ROAP.

Receive Path Overhead Processor (RPOP)

- The H1 and H2 pointer bytes are detected and interpreted according to ANSI T1.105 and ITU-T G.707. The mechanism is programmable to support both SONET and SDH. Path Alarm Indication Signal (AIS-P) and Loss of Pointer (LOP-P) alarm declarations are provided. Several pointer functions are also provided for diagnostic purposes.
- The H1 and H2 pointer bytes are monitored for Concatenation Indication (CI). Loss of Pointer (LOPX) and AIS (AISX) alarm declarations are provided.
- Path BIP-8 errors carried in the B3 byte are detected and accumulated. Both individual and block mode accumulation of B3 errors are supported.
- Path REI error indications carried in the G1 byte are detected and accumulated. Up to 64000 individual errors can be detected per second. Both individual and block mode accumulation of Path REI error indications are supported.
- The Path RDI carried in the G1 byte is detected and programmable.
- The Signal Label carried in the C2 byte is detected, alarmed and is programmable.

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Receive Packet Processor (RPP)

- The byte value used to identify the HDLC Flag Sequence is programmable.
- The detection and discarding of invalid frames are programmable.
- The expected Control Escape byte value and the Octet Destuffing Masking byte are programmable.
- The expected Address and Control Field values are programmable.
- The Protocol Field declaration and processing is programmable.
- The Abort Sequence is detected in the incoming HDLC frames.
- The received Frame Check Sequence (FCS) field is verified. The FCS checksum is calculated using either a 16-bit, CRC-CCITT generating polynomial $1 + x^5 + x^{12} + x^{16}$, or a 32-bit, CRC-32 generating polynomial $1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$.
- The received data is descrambled with the self synchronizing scrambler (SSS) polynomial $1 + x^{43}$. Full and/or partial descrambling can be independently enabled/disabled.
- Long and short packet checking are provided and are programmable.
- Self Describing Padding is supported and programmable.
- The storage of the PPP Protocol Field in the Rx FIFO may be enabled/disabled.
- The size of the Rx FIFO size is 4095 words, which may accommodate storage for a total of 16380 PPP Protocol/Information Field bytes.
- The definition of received “errored” HDLC frames is programmable. For these errored HDLC frames two different procedures can be applied.
- A filtering function is provided to perform packet discartion and error marking based on a set of programmable labels. There are four programmable label matching triggers, and one compliment word matching trigger that functions the packet discard and TERR marking.
- The following statistics are provided in the performance monitoring 32-bit counters:
 - Received Aborted HDLC frames
 - Received FCS errored HDLC frames
 - Received Empty HDLC frames
 - Received HDLC frames where Address-and-Control-Field-Compression was found
 - Received Long packets
 - Received Short packets
 - Received Invalid Frames
 - Received bytes pre-octet destuffing
 - Received bytes post-octet destuffing
 - Received number of frames excluding Invalid Frames
 - Packets discarded by label filtering
 - Packets error-marked by label filtering

- Packets stored in the Rx FIFO
- Packets stored in the Rx FIFO that are error marked
- Packet bytes stored in the Rx FIFO
- Number of received PPP padding bytes
- The SPE Transparent Mode is provided to allow all of the SPE payload to pass directly to the Rx FIFO without further processing.

Receive ATM Cell Processor (RACP)

- Cell Delineation is provided using shortened cyclic code with a generating polynomial $1 + x + x^2 + x^8$. The coset polynomial $1 + x^2 + x^4 + x^8$ can be added to the calculated HEC check bits before comparison.
- Single-bit header error correction is supported. The dropping of cells during single or multiple error detection is programmable.
- The 48 byte information field is descrambled with a self-synchronizing descrambler polynomial $1 + x^{43}$. Descrambling can be enabled/disabled.
- Cells can be filtered based on a programmable cell header pattern in the GFC, PTI, or CLP fields.
- The number of correctable and uncorrectable HEC errors detected, and the number of cells written to the Rx FIFO are monitored.
- The Rx FIFO can accommodate storage of eight ATM cells.

Drop Side Interface (POS/ATM Interface)

- A parity bit, programmable for even/odd parity, is provided for each transmit and receive datapaths.
- The Drop Side Interface provides an industry compliant packet interface for POS operations.
- The packet interface supports word-level and packet-level transfer modes.
- The DTPA signal is provided to indicate the waterlevel of the Tx FIFO counted at word level and is programmable.
- It is possible to force reset/flush the contents in the Tx FIFO via the CPU interface.
- It is possible to force reset/flush the contents in the Rx FIFO via the CPU interface.
- The Drop Side Interface provides a Single-PHY UTOPIA-3 interface for ATM operations.
- Two formats of the ATM cells are supported: 52 byte cell or 56 byte cell containing the HEC.
- The UTOPIA-3 interface supports both word-level and cell-level flow control.

Transmit ATM Cell Processor (TACP)

- The ATM cells are mapped into the STS-48c SPE or equivalent SDH VC-16-16c. Programmable idle/unassigned cells are inserted into the cell stream.
- The 48 byte information field is scrambled with a self-synchronizing descrambler polynomial $1 + x^{43}$. Scrambling can be enabled/disabled.

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- The HEC generator performs a CRC-8 calculation over the first four header octets using the generating polynomial $1 + x + x^2 + x^8$. The coset polynomial $1 + x^2 + x^4 + x^6$ can be added to the result. The HEC is optionally inserted into the fifth octet of the header of cells read from the Tx FIFO.
- The Tx FIFO can accommodate storage of eight ATM cells.

Transmit Packet Processor (TPP)

- The inserted HDLC Flag Sequence byte and the minimum number of Flag Sequence bytes separating HDLC frames are programmable.
- The insertion of the Address and Control fields can be controlled by the HDLC Address-and-Control-Field-Compression mechanism.
- The Address Field inserted after the beginning Flag Sequence is programmable.
- The Control Field inserted after the the Address Field is programmable.
- The Frame Check Sequence (FCS) can be generated using either a 16-bit, CRC-CCITT generating polynomial $1 + x^5 + x^{12} + x^{16}$, or a 32-bit CRC-32 generating polynomial $1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$.
- Octet Stuffing, or “escaping”, can be applied after the FCS generation and partial scrambling, if enabled. The Control Escape byte and the Octet Stuffing Masking byte are programmable. The Asyc-Control-Character-Map (ACCM) can accommodate a maximum of 5 byte values. Each value can be individually enabled/disabled.
- The transmitted data is scrambled with a self-synchronizing scrambler (SSS) polynomial $1 + x^{43}$. Full and/or partial scrambling can be independently enabled/disabled.
- The PPP Protocol Field can be generated internally or extracted from the transmit FIFO. The size and value of the inserted Protocol Field are programmable when generated internally.
- The Tx FIFO is programmable in the range from 1 to 4095 words or 16380 bytes of data storage. All valid packet bytes stored in the Tx FIFO are read out and mapped into the PPP Protocol/Information Fields of generated PPP/HDLC frames.
- Two Tx PIF packet transfer modes are supported: packet transfer mode and word transfer mode.
- The TXF_ERR signal is provided to force insertion of errors into the FCS, or to force abort the transmitted HDLC frame.
- It is possible to force XOR'ing of the transmitted Address, Control or Protocol Fields with a programmable mask value via the CPU interface for diagnostic purposes.
- The following statistics are provided in the performance monitoring 32-bit counters:
 - Bytes read from Tx FIFO
 - Transmitted good HDLC frames (non-aborted, non-FCS errored)
 - Transmitted Aborted HDLC frames
 - Transmitted FCS Errored HDLC frames

- Long packets read from Tx FIFO
- Short packets read from Tx FIFO
- Transmitted empty HDLC frames
- Bytes pre octet-stuffing (excluding Abort sequences)
- Bytes post octet-stuffing (excluding Abort sequences)
- The SPE Transparent Mode is provided to allow the Tx FIFO content to be passed directly into the SPE payload without further processing.

Transmit Path Overhead Processor (TPOP)

- The H1 and H2 pointer byte values are programmable to support both SONET and SDH. Several pointer functions are provided for diagnostics purposes. The remaining 47 H1 and H2 bytes are programmable.
- The Path BIP-8 is computed and placed in the B3 byte of the current frame. It is possible to insert B3 errors for diagnostic purposes.
- The number of Path BIP-8 errors detected in the Receive Path Overhead Processor (RPOP) is backreported as Path REI in the G1 byte. Both individual and block mode backreporting for G1 are supported.
- It is possible to enable/disable RDI-P insertion for each of the following alarms: LOS, LOF, AIS-L, AIS-P, LOP-P, TIM-P, UNEQ-P, LCD-P and PLM-P. Both the latest and earlier definitions of RDI-P are supported.
- The Path Signal Label (C2) byte value is programmable.
- The Path Trace (J1) byte value is programmable.
- The F2, H4, Z3, Z4, and Z5 bytes are programmable.

Transmit Line Overhead Processor (TLOP)

- It is possible to insert programmable sets of K1 and K2 bytes into the outgoing data stream.
- RDI-L can be automatically inserted during the detection of an LOS, LOF, or AIS-L alarm in the receive data stream.
- The Line BIP-384 code is computed and placed in the B2 bytes of the current frame. It is possible to insert B2 errors for diagnostics purposes.
- The number of Line BIP-384 errors detected in the Receive Line Overhead Processor (RLOP) is backreported as Line REI in the M1 byte. Up to 255 errors can be backreported per frame in individual mode. Both individual and block mode backreporting for M1 are supported. It is possible to insert M1 error indications for diagnostics purposes.
- The Synchronization Status value inserted in the S1 byte is programmable.
- Bytes input to the special purpose ports of the Transmit Overhead Access Port (TOAP) can be inserted into the D4-D12, E2, S1, K1 and K2 bytes of the outgoing Line overhead.
- All bytes in the line overhead that are reserved for national or future international standardization use can be overwritten with 0x00.

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- The H1, H2, and H3 bytes from the Transmit Overhead Access Port (TOAP) can be inserted into the H1, H2, and H3 overhead bytes, or applied as an error mask to the H1, H2, and H3 overhead bytes.

Transmit Section Overhead Processor (TSOP)

- It is possible to forced insert all "1"s into the data stream, before scrambling, with the exception of the section overhead. The AIS-L condition can be automatically inserted through activity from the special purpose serial interfaces.
- The Section BIP-8 code is computed and can be placed in the B1 byte of the current frame. It is possible to insert B1 errors for diagnostics purposes.
- The A1 and A2 framing bytes can be inserted into the frame. It is also possible to introduce bit errors in the framing word.
- The J0 byte supports both SONET and SDH formats. The J0 byte can be programmed to a fixed value for interworking with older equipment implementing the C1 identification byte.
- The Z0 growth bytes supports both SONET and SDH formats. The Z0 bytes can be programmed to carry the C1 identification bytes for interworking with older equipment.
- The outgoing data stream is optionally scrambled using the generating polynomial $1 + x^6 + x^7$ with a sequence length of 127.
- It is possible to force insert all "0"s in the outgoing data stream after scrambling for diagnostic purposes (LOS).
- Bytes input to the special purpose ports of the TOAP can be inserted into the D1-D3, E1, F1 and J0 bytes of the outgoing Section overhead.
- All bytes in the section overhead that are reserved for national or future international standardization use can be overwritten with 0x00.
- A frame pulse is provided for the outgoing data stream and is programmable.

Receive Overhead Access Port (ROAP)

- Two identical, but independent, special purpose ports are provided for the extraction of special purpose bytes from the SONET/SDH transport overhead and of certain SONET/SDH alarms specific to automatic protection switching (APS) applications.
- The frame pulse RSPFP is synchronized to the receive drop side frame pulses RXFPOUTA-D.
- The entire section/line transport overhead can be extracted from the serial output port RTOH[3..0].

Transmit Overhead Access Port (TOAP)

- Two identical, but independent, special purpose ports are provided for the insertion of special purpose bytes into the SONET/SDH transport overhead and of certain SONET/SDH alarms specific to automatic protection switching (APS) applications.
- The entire transport overhead is captured from the serial input ports TTOH[3..0]. The captured data can be selectively inserted into the corresponding overhead bytes of the transmitted SONET/SDH frame.

SONET/SDH Section Trace Buffers (SSTB)

- Three different Section Trace Message (J0) formats are supported in both transmit and receive directions: one byte (SONET) message, 16 byte (SDH) message, and 64 byte (SONET CLLI) message.
- The received section trace message is checked for persistency. A mismatch alarm is supported.

CPU Interface

- All configuration bits are both writeable and readable and can be accessed regardless of the device clock source status, except for the reset state. Configuration bits include selection bits, interrupt masking bits, and programmable counter/control values.
- Eight programmable General Purpose Input/Output (GPIO) ports are available for monitoring and controlling external signals. All GPIOs support bistable interrupts when configured as input ports.
- Clock activity monitors are implemented for all input clocks.

Bit Error Rate Monitoring

- Bit error rate monitoring is based on the Line BIP (B2) error code and is capable of measuring BERs down to 10^{-10} .
- There are four independent BER monitors with individual accumulation periods and alarm thresholds.
- A saturation threshold is implemented for each BER monitor to specify the maximum number of errors that can be accumulated per frame.
- The BER Signal Degrade (BER-SD) alarm is based on BER monitors 1 and 2.
- The BER Signal Fail (BER-SF) alarm is based on BER monitors 3 and 4.

JTAG

- Standard IEEE 1149.1 compliant JTAG interface.

Loopback Modes

- Equipment loopback is supported by looping the output from the Transmit Section Overhead Processor (TSOP), in the transmit direction, back to the input of the Receive Section Overhead Processor (RSOP), in the receive direction.
- Facility loopback is supported by looping the data received on the receive Line Side Interface back to the transmit Line Side Interface.
- Section loopback is supported by looping the output from the Receive Section Overhead Processor (RSOP) in the receive direction back to the input of the Transmit Section Overhead Processor (TSOP), in the transmit direction.
- Line loopback is supported by looping the output from the Receive Line Overhead Processor (RLOP) in the receive direction back to the input of the Transmit Line Overhead Processor (TLOP), in the transmit direction.
- Drop side loopback is supported by looping the output from the Tx FIFO to the input of the Rx FIFO. This loopback is supported for both packet and ATM cell mode.

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AC Characteristics

Figure 1: Tx Serial Line Interface Timing Dependencies

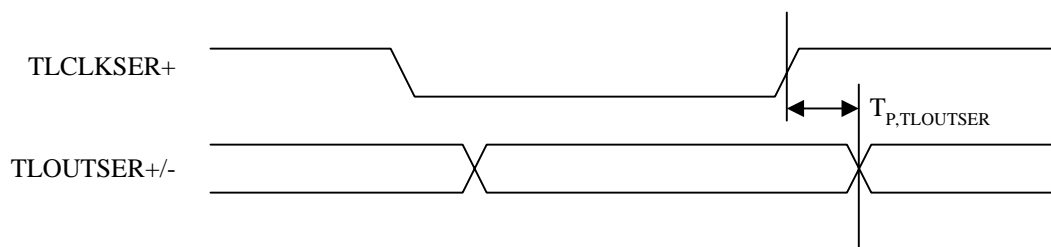


Table 1: Tx Serial Line Interface

| Symbol | Description | Min | Max | Unit |
|---------------------|--|-----|------|------|
| $f_{TLCLKSER}$ | TLCLKSER+/- clock frequency (nominal) | - | 2488 | MHz |
| $T_{dc, TLCLKSER}$ | TLCLKSER+/- duty cycle | | | % |
| $T_{r/f, TLCLKSER}$ | TLCLKSER+/- rise/fall time (20-80%) | | | ps |
| $T_{p, TLOUTSER}$ | TLCLKSER+ rising edge to TLOUTSER+/- valid | -75 | +75 | ps |
| T_{JS} | Output Data Jitter RMS | | 4 | ps |
| $T_{JS, Peak}$ | Output Data Jitter Peak-to-Peak | | 40 | ps |

CMU Reference Clock Frequencies are 155 MHz, 311 Mhz, and 622 MHz
Jitter tested to SONET specifications with 2ps RMS jitter on the Reference Clock

Figure 2: Rx Parallel Line Interface Timing Dependencies

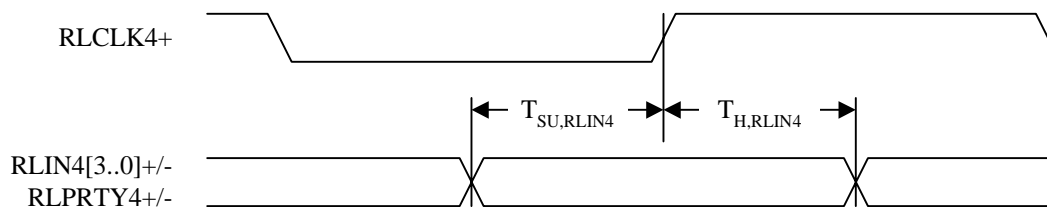


Table 2: Rx Parallel Line Interface

| Symbol | Description | Min | Max | Unit |
|----------------------|--|------|--------|------|
| f_{RLCLK4} | RLCLK4+/- clock frequency (nominal) | - | 622.08 | MHz |
| $T_{dc, RLCLK4}$ | RLCLK4+/- duty cycle | 45 | 55 | % |
| $T_{r/f, RLCLK4}$ | RLCLK4+/- rise/fall time (20-80%) | | | ps |
| $T_{jitter, RLCLK4}$ | RLCLK4+/- cycle-to-cycle | -100 | +100 | |
| $T_{su, RLIN4}$ | RLIN4[3..0]+/-, RLPRTY4+/- setup time to RLCLK4+ rising edge | +300 | - | ps |
| $T_{h, RLIN4}$ | RLIN4[3..0]+/-, RLPRTY4+/- hold time to RLCLK4+ rising edge | +300 | - | ps |

Figure 3: Tx Parallel Line Interface Timing Dependencies

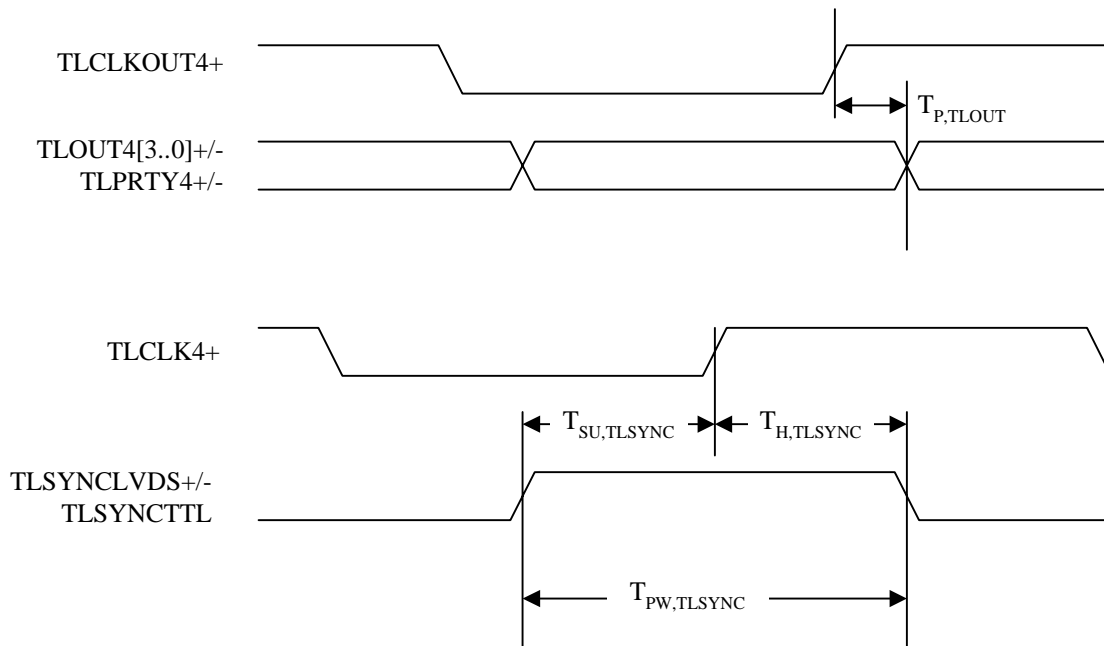


Table 3: Tx Parallel Line Interface

| Symbol | Description | Min | Max | Unit |
|----------------------|---|------|--------|------|
| $f_{TLCLKOUT4}$ | TLCLKOUT4+/- clock frequency (nominal) | - | 622.08 | MHz |
| $T_{dc, TLCLKOUT4}$ | TLCLKOUT4+/- duty cycle | 40 | 60 | % |
| $T_{r/f, TLCLKOUT4}$ | TLCLKOUT4+/- rise/fall time (20-80%) | | | ps |
| $T_{p, TLOUT}$ | TLCLKOUT4+ rising edge to TLOUT4[3..0]+/-, TLPRTY4+/- valid | -200 | +200 | ps |
| f_{TLCLK4} | TLCLK4+/- clock frequency (nominal) | - | 622.08 | MHz |
| $T_{dc, TLCLK4}$ | TLCLK4+/- duty cycle | 45 | 55 | % |

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Table 3: Tx Parallel Line Interface

| | | | | |
|----------------------|---|---------------|------|----|
| $T_{r/f, TLCLK4}$ | TLCLK4+/- rise/fall time (20-80%) | | | ps |
| $T_{jitter, TLCLK4}$ | TLCLK4+/- cycle-to-cycle jitter | -100 | +100 | ps |
| $T_{su, TLSYNC}$ | TLSYNC setup time to TLCLK4+ rising edge ¹⁾ | +300 | - | ps |
| $T_h, TLSYNC$ | TLSYNC hold time from TLCLK4+ rising edge ¹⁾ | +300 | - | ps |
| $T_{PW, TLSYNC}$ | TLSYNC pulse width | $8/f_{TLCLK}$ | - | ns |

¹⁾ *TLSYNCLVDS may be asynchronous. In this case the pulse width needs to be at least 9 TLCLK periods when f_{TLCLK} is 622.08 MHz.
TLSYNCTTL is asynchronous. For proper sampling the pulse width needs to be at least 9 TLCLK periods when f_{TLCLK} is 622.08 MHz.*

Figure 4: Rx Drop Interface Timing Dependencies

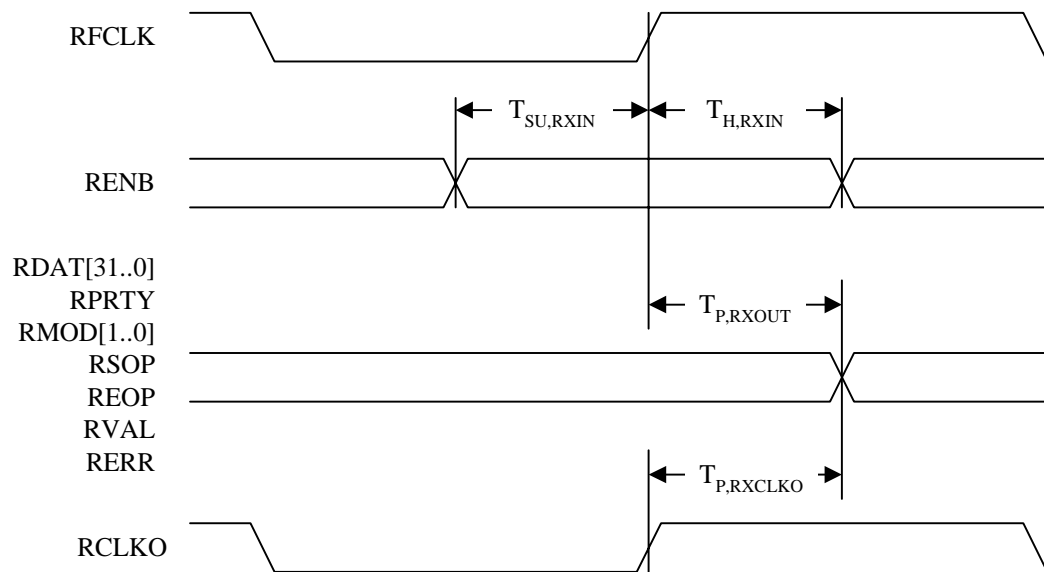


Table 4: Rx Drop Interface

| Symbol | Description | Min | Max | Unit |
|------------------|--------------------------------------|--|-----|------|
| f_{RFCLK} | RFCLK Clock Frequency (nominal) | 50 | 104 | MHz |
| dc_{RFCLK} | RFCLK Duty Cycle | 40 | 60 | % |
| $T_{R/F, RFCLK}$ | RFCLK Rise/Fall Time | - | 2.0 | ns |
| dc_{RFCLKO} | RFCLKO Duty Cycle | $dc_{RFCLK} - (1.0 \text{ ns} \times f_{RFCLK})\%$ | | % |
| $T_{SU, RXIN}$ | RENB Setup Time to RFCLK Rising Edge | 2.0 | - | ns |
| $T_{H, RXIN}$ | RENB Hold Time to RFCLK Rising Edge | 0.5 | - | ns |

Table 4: Rx Drop Interface

| Symbol | Description | Min | Max | Unit |
|-----------------|---|-----|-----|------------------|
| $T_{P, RXOUT}$ | RFCLK Rising Edge to RDATA[31..0], RPRTY, RMOD[1..0], RSOP, REOP, RVAL and RERR Valid | 1.0 | 6.0 | ns ¹⁾ |
| | | 0.5 | 4.2 | ns ²⁾ |
| $T_{P, RXCLKO}$ | RFCLKO Rising Edge RDATA[31..0], RPRTY, RMOD[1..0], RSOP, REOP, RVAL and RERR Valid | 0.0 | 1.5 | ns ³⁾ |

¹⁾ Output times are for 25 pF load.
²⁾ Output times are for 5 pF load.
³⁾ Output times are for 5 to 15 pF load.

Figure 5: Tx Drop Interface Timing Dependencies

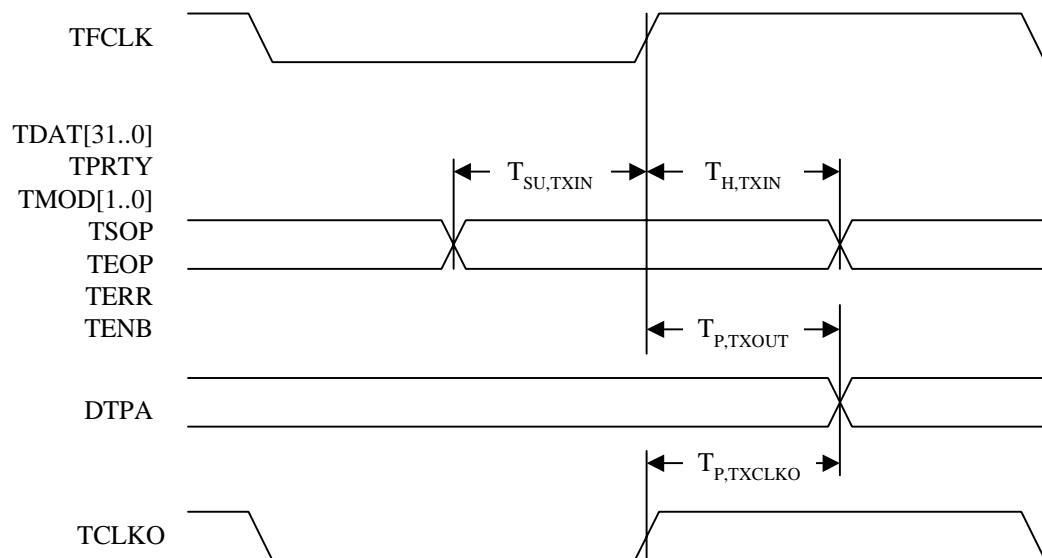


Table 5: Tx Drop Interface

| Symbol | Description | Min | Max | Unit |
|------------------|---|--|-----|------|
| f_{TFCLK} | TFCLK Clock Frequency | 50 | 104 | MHz |
| dc_{TFCLK} | TFCLK Duty Cycle | 40 | 60 | % |
| $T_{R/F, TFCLK}$ | TFCLK Rise/Fall Time | - | 2.0 | ns |
| dc_{TFCLKO} | TFCLKO Duty Cycle | $dc_{TFCLK} - (1.0 \text{ ns} \times f_{TFCLK})\%$ | | % |
| $T_{SU, TXIN}$ | TDAT[31..0], TPRTY, TMOD[1..0], TSOP, TEOP, TERR and TENB Setup Time to TFCLK Rising Edge | 2.0 | - | ns |
| $T_{H, TXIN}$ | TDAT[31..0], TPRTY, TMOD[1..0], TSOP, TEOP, TERR and TENB Hold Time to TFCLK Rising Edge | 0.5 | - | ns |

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Table 5: Tx Drop Interface

| Symbol | Description | Min | Max | Unit |
|------------------------|-----------------------------------|-----|-----|------------------|
| T _{P, TXOUT} | TFCLK Rising Edge to DTPA Valid | 1.0 | 6.0 | ns ¹⁾ |
| | | 0.5 | 4.2 | ns ²⁾ |
| T _{P, TXCLKO} | TFCLKO Rising Edge to DTPA Valid. | 0.0 | 1.5 | ns ³⁾ |

¹⁾ Output times are for 25 pF load.
²⁾ Output times are for 5 pF load.
³⁾ Output times are for 5 to 15 pF load.

Figure 6: Rx Overhead Access Port Timing Dependencies

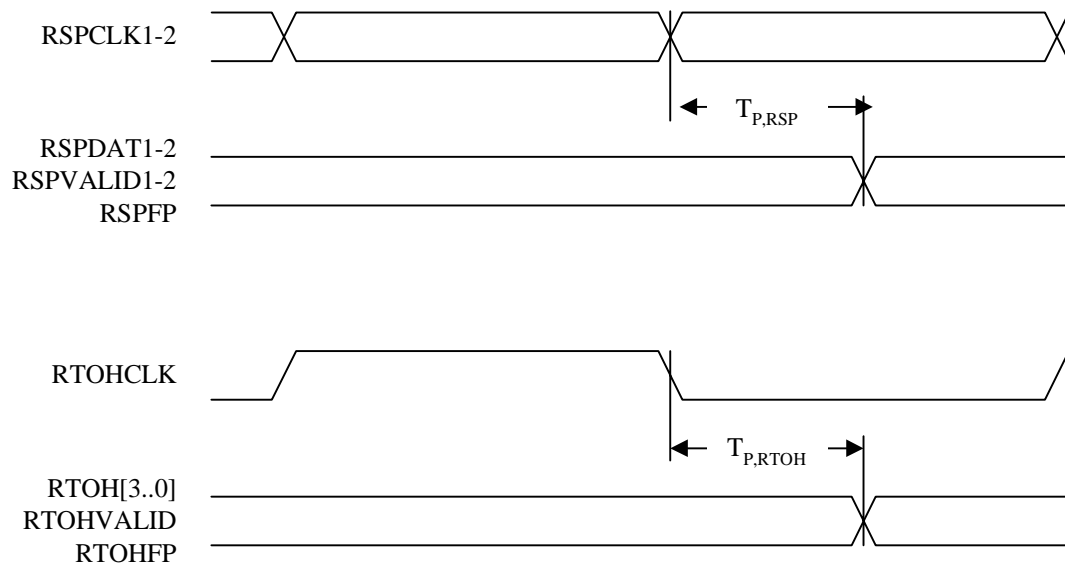


Table 6: Rx Overhead Access Port

| Symbol | Description | Min | Max | Unit |
|---------------------------|--|------|-------|------|
| f _{RSPCLK} | RSPCLK1-2 Clock Frequency (optionally gapped) | - | 2.16 | MHz |
| dc _{RSPCLK} | RSPCLK1-2 Duty Cycle | 40 | 60 | % |
| T _{R/F, RSPCLK} | RSPCLK1-2 Rise/Fall Time | - | 2.0 | ns |
| T _{P, RSP} | RSPCLK1-2 Rising/Falling Edge ²⁾ to RSPDAT1-2, RSPVALID1-2, RSPFP Valid | -6.0 | +15.0 | ns |
| f _{RTOHCLK} | RTOHCLK Clock Frequency (nominal) | - | 38.88 | MHz |
| dc _{RTOHCLK} | RTOHCLK Duty Cycle | 40 | 60 | % |
| T _{R/F, RTOHCLK} | RTOHCLK Rise/Fall Time | - | 2.0 | ns |

Table 6: Rx Overhead Access Port

| Symbol | Description | Min | Max | Unit |
|---------------|--|------|------|------|
| $T_{P, RTOH}$ | RTOHCLK Rising/Falling Edge ³⁾ to RTOH[0..3], RTOHVALID, RTOHFP Valid | -3.0 | +7.0 | ns |

²⁾ Active edge of clock is programmable for group of inputs for each independent port.

³⁾ Active edge of clock is programmable for group of inputs.

All output times are for 50 pF load.

Figure 7: Tx Overhead Access Port Timing Dependencies

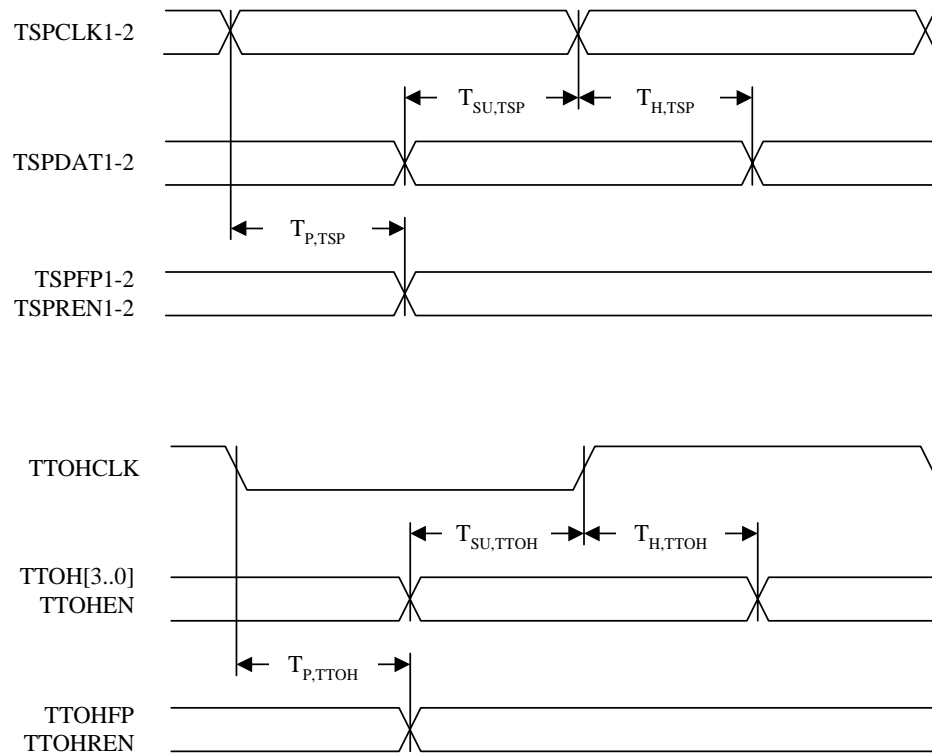


Table 7: Tx Overhead Access Port

| Symbol | Description | Min | Max | Unit |
|-------------------|---|------|------|------|
| f_{TSPCLK} | TSPCLK1-2 Clock Frequency (optionally gapped) | - | 2.16 | MHz |
| dc_{TSPCLK} | TSPCLK1-2 Duty Cycle | 40 | 60 | % |
| $T_{R/F, TSPCLK}$ | TSPCLK1-2 Rise/Fall Time | - | 2.0 | ns |
| $T_{SU, TSP}$ | TSPDAT1-2 Setup Time to TSPCLK1-2 Rising/Falling Edge ⁵⁾ | 25.0 | - | ns |
| $T_{H, TSP}$ | TSPDAT1-2 Hold Time to TSPCLK1-2 Rising/Falling Edge ⁵⁾ | 0 | - | ns |

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Table 7: Tx Overhead Access Port

| Symbol | Description | Min | Max | Unit |
|--------------------|--|-------|-------|------|
| $T_{P, TSP}$ | TSPCLK1-2 Rising/Falling Edge ⁶⁾ to TSPREN1-2, TSPFP1-2 Valid | -10.0 | +20.0 | ns |
| $f_{TTOHCLK}$ | TTOHCLK Clock Frequency (nominal) | - | 38.88 | MHz |
| $dc_{TTOHCLK}$ | TTOHCLK Duty Cycle | 40 | 60 | % |
| $T_{R/F, TTOHCLK}$ | TTOHCLK Rise/Fall Time | - | 2.0 | ns |
| $T_{SU, TTOH}$ | TTOH[0..3], TTOHEN Setup Time to TTOHCLK Rising/Falling Edge ⁷⁾ | 15.0 | - | ns |
| $T_{H, TTOH}$ | TTOH[0..3], TTOHEN Hold Time to TTOHCLK Rising/Falling Edge ⁷⁾ | -1.0 | - | ns |
| $T_{P, TTOH}$ | TTOHCLK Rising/Falling Edge ⁸⁾ to TTOHREN, TTOHFP Valid | -3.0 | +7.0 | ns |

⁵⁾ Active edge of clock is programmable for group of inputs for each independent port.
⁶⁾ Active edge of clock is programmable for group of outputs for each independent port.
⁷⁾ Active edge of clock is programmable for group of inputs.
⁸⁾ Active edge of clock is programmable for group of outputs.
 All output times are for 50 pF load.

Figure 8: JTAG Interface Timing Dependencies

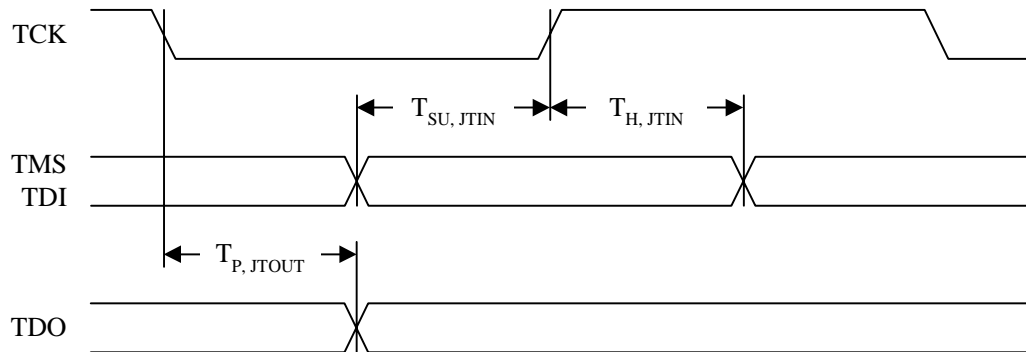


Table 8: JTAG Interface

| Symbol | Description | Min | Max | Unit |
|----------------|---------------------------------------|-----|-----|------|
| f_{TCK} | TCK Frequency | - | 1 | MHz |
| dc_{TCK} | TCK Duty Cycle | 40 | 60 | % |
| $T_{SU, JTIN}$ | TMS/TDI Setup Time to TCK Rising Edge | 50 | - | ns |
| $T_{H, JTIN}$ | TMS/TDI Hold Time to TCK Rising Edge | 50 | - | ns |
| $T_{P, JOUT}$ | TCK Falling Edge to TDO Valid | 1.5 | 50 | ns |

Figure 9: CPU Read Access Timing Dependencies

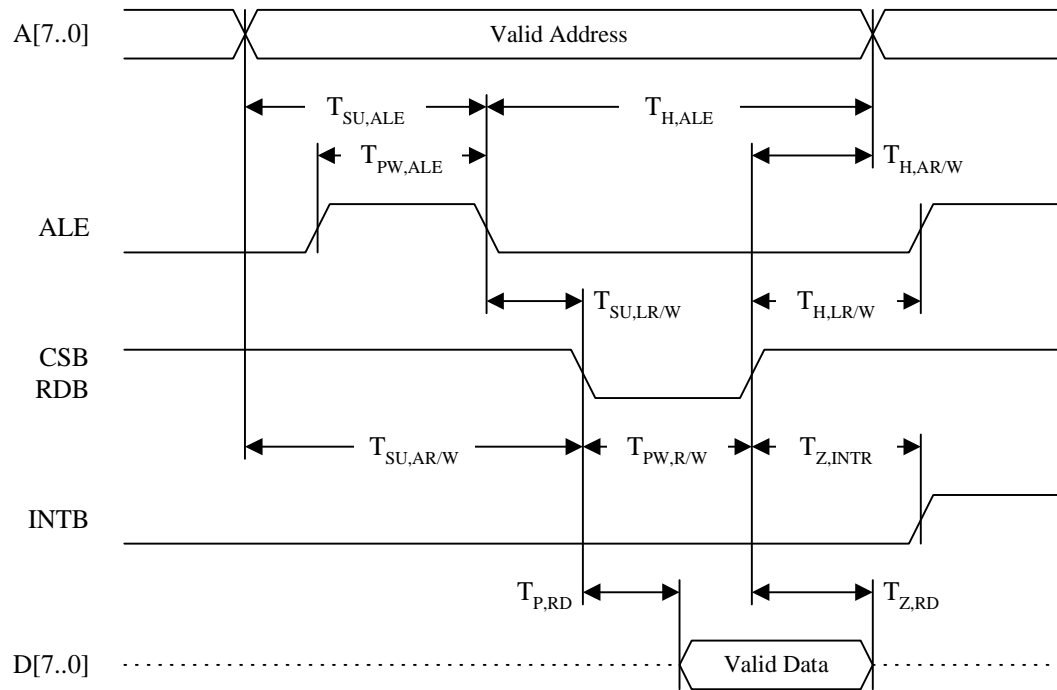
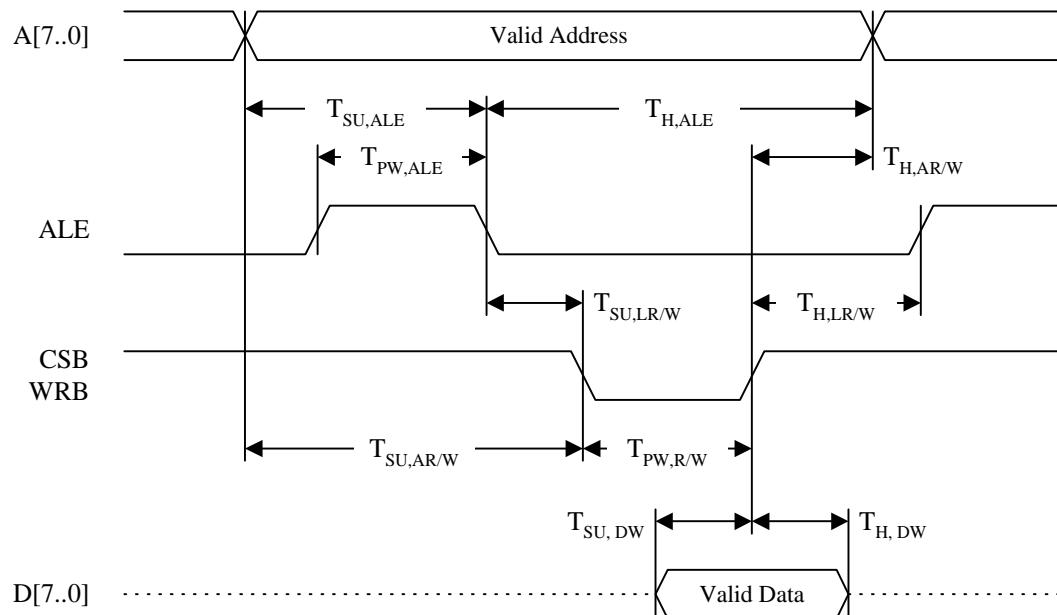


Figure 10: CPU Write Access Timing Dependencies



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Table 9: CPU Read/Write Access

| <i>Symbol</i> | <i>Description</i> | <i>Min</i> | <i>Max</i> | <i>Unit</i> |
|-----------------------|---|------------|------------|-------------|
| T _{SU, ALE} | Address to Address Latch Setup Time | 10 | - | ns |
| T _{H, ALE} | Address to Address Latch Hold Time | 10 | - | ns |
| T _{PW, ALE} | Address Latch Pulse Width | 20 | - | ns |
| T _{SU, LR/W} | Latch to Valid Read/Write Setup Time | 0 | - | ns |
| T _{H, LR/W} | Latch to Valid Read/Write Hold Time | 5 | - | ns |
| T _{SU, AR/W} | Address to Valid Read/Write Setup Time | 10 | - | ns |
| T _{H, AR/W} | Address to Valid Read/Write Hold Time | 10 / 5 | - | ns |
| T _{PW, R/W} | Valid Read/Write Pulse Width | 20 / 25 | - | ns |
| T _{SU, DW} | Data to Valid Write Setup Time | 20 | - | ns |
| T _{H, DW} | Data to Valid Write Hold Time | 10 | - | ns |
| T _{P, RD} | Valid Read to Valid Data Propagation Delay | | 80 | ns |
| T _{Z, RD} | Valid Read Negated to Output Tristate | 1 | 25 | ns |
| T _{Z, INT} | Valid Read Negated to Interrupt Release/Pull-down | | 100 | ns |

All output times are for 100 pF load.

DC Characteristics

| Parameters | Description | Min | Max | Units | Conditions |
|---------------------|------------------------------------|-----------------------|-----------------------|-------|---|
| V _{OH} | Output HIGH voltage (TTL) | V _{DDO} -0.2 | — | V | V _{DD} =Min, V _{DDO} =Min, I _{OH} = -0.2, -0.4, -0.6, -0.8, -1.2, -1.6.mA. |
| V _{OH} | Output HIGH voltage (TTL) | V _{DDO} -0.5 | — | V | V _{DD} =Min, V _{DDO} =Min, I _{OH} = -2, -4, -6, -8, -12, -16.mA. |
| V _{OL} | Output LOW voltage (TTL) | — | 0.2 | V | V _{DD} =Min, V _{DDO} =Min, I _{OL} = 0.2, 0.4, 0.6, 0.8, 1.2, 1.6.mA. |
| V _{OL} | Output LOW voltage (TTL) | — | 0.4 | V | V _{DD} =Min, V _{DDO} =Min, I _{OL} = 2, 4, 6, 8, 12, 6.mA |
| V _{IH} | Input HIGH voltage (TTL) | 2.0 | V _{DDO} +0.5 | V | Guaranteed Logic HIGH Level |
| V _{IL} | Input LOW voltage (TTL) | -0.3 | 0.8 | V | Guaranteed Logic LOW Level |
| I _{IH} | Input high current (TTL) | — | +/- 1 | μA | V _{DD} =MAX |
| I _{IL} | Input low current (TTL) | — | +/- 1 | μA | V _{DD} =MAX |
| V _{OCM} | O/P Common Mode Range (LVDS) | TBD | TBD | mV | TBD |
| ΔV _{OUT50} | Differential Output Voltage (LVDS) | TBD | TBD | mV | TBD |
| V _{ICM} | I/P Common Mode Range (LVDS) | TBD | TBD | mV | TBD |
| ΔV _{IN} | Differential Input Voltage (LVDS) | TBD | TBD | mV | TBD |
| I _{IP} | Input current (LVDS) | TBD | TBD | μA | TBD |
| V _{OCM} | O/P Common Mode Range (PECL) | TBD | TBD | mV | TBD |
| ΔV _{OUT50} | Differential Output Voltage (PECL) | TBD | TBD | mV | TBD |
| V _{ICM} | I/P Common Mode Range (PECL) | TBD | TBD | mV | TBD |
| ΔV _{IN} | Differential Input Voltage (PECL) | TBD | TBD | mV | TBD |
| I _{IP} | Input current (PECL) | TBD | TBD | μA | TBD |

Power Dissipation

| Parameter | Description | (Typ) | (Max) | Units |
|------------------|---------------------------|-------|-------|-------|
| I _{3.3} | 3.3V power supply current | 368 | 435 | mA |
| I _{1.8} | 1.8V power supply current | 730 | 875 | mA |
| P _D | Power dissipation | 2.5 | 3.0 | W |

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Absolute Maximum Ratings(1)

| | |
|--|----------------------------|
| Power Supply Voltage (V_{DD}) Potential to GND | -0.5V to +4V |
| DC Input Voltage (LVDS inputs) | -0.5V to $V_{DD} + 0.5V$ |
| DC Input Voltage (TTL inputs) | -0.5V to $V_{DD33} + 0.5V$ |
| DC Output Voltage (TTL Outputs)..... | -0.5V to $V_{DD} + 0.5V$ |
| Output Current (TTL Outputs) | +/-50mA |
| Output Current (LVDS Outputs) | +/-50mA |
| Case Temperature Under Bias | -55° to +125°C |
| Storage Temperature..... | -65°C to +150°C |
| Maximum Input ESD (Human Body Model) | 2000 V |

Note: Caution: Stresses listed under "Absolute Maximum" may cause permanent damage. Functionality at or exceeding the values listed does not affect device reliability.

Recommended Operating Conditions

| | |
|---|--------------|
| Power Supply Voltage (V_{DD}) | +3.3V ±10 % |
| Power Supply Voltage | +1.8V ±10 % |
| Operating Temperature Range* (T)..... | -24° to 95°C |

* Lower limit and upper limit of specifications are in ambient temperature with no air flow.

Package Pin Description

| Signal | Name | I/O | Type | Description |
|-----------------|------------------------------|-----|------|---|
| RLCLK+/- | Parallel Line Receive clock | I | LVDS | Clock reference for the 2.5Gb/s receive flow carried in RLI N[3..0]. The clock frequency is nominally 622MHz equivalent to STS-48/STM-16 operation (4-bit interface). |
| RLIN[3..0]+/- | Parallel Line Receive Data | I | LVDS | Parallel data bus for the incoming STS-48/STM-16 data stream. RLIN [3] is the most significant bit. RLIN[3] is the first arriving bit on the serial data stream is sampled on the rising edge of RLCLK+ (4-bit interface). |
| RLPRTY+/- | Parallel Line Receive Parity | I | LVDS | Parity input (even/odd parity) for the parallel receive line data, RLIN[3..0]. RLPRTY is sampled on the rising edge of RLCLK+ (4-bit interface). |
| CRURECCLK+/- | CRU Recovered Clock | O | PECL | The recovered clock (2.5Gb/s) scaled to the frequency selected by CRUREFSEL[1..0]. |
| CRUREFSEL[1..0] | CRU Reference Clock Select | I | TTL | Selects the frequency of the CRU reference clock. Bit1 Bit0. 0 0 : 622MHz 0 1 : 311MHz 1 0 : 155MHz 1 1 : 78MHz |
| CRUREFDET | CRU Reference Clock Detect | O | TTL | Reference frequency detect is active high. When this alarm is high it means that the REFCLK input doesn't switch. Status and Interrupt also available through CPU access. |
| CRULOCKDET | CRU Lock Detect | O | TTL | CRU Lock detect is active high. When this alarm is high it means that the REFCLK is in the lock range. Status and interrupt also available through CPU access. |
| CRUFILTER+/- | CRU Loop filter | I | PECL | External CRU loop filter pins. The true loop filter pin is connected via 0.1uF capacitor to the complement loop filter pin. |
| CRUREFCLK+/- | Reference frequency | I | PECL | Differential reference clock input to the CRU. |
| RLINSERCNTR +/- | Input Data Center Tap | | | RLINSER+/- will have 100 ohms termination with a center tap connection @ 50 ohms |
| RLINSER+/- | Input Data | I | CML | High speed differential data input. |
| CLKRSTEN | Clock Reset Enable | I | TTL | If CLKRSTEN is asserted, all primary clock outputs (TXRCLK, RXRCLK, RSPCLK1, RSPCLK2, RTOHCLK, TSPCLK1, TSPCLK2, and TTOHCLK) will halt during master reset. If CLKRSTEN is deasserted, all primary clock outputs will be running during device master reset. |

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| Signal | Name | I/O | Type | Description |
|------------------|-------------------------------------|-----|-------------|---|
| LOOPTIMING | Internal Looptiming Enable | I | TTL | Selects (CMU reference frequency) from CMUREFCLK (77.76MHz / 155.52MHz) or recovered clock from the receive CRU (155.52MHz). The value of this pin is XOR'ed with a CPU register to generate LOOPTIME1 |
| CMUREFSEL [1..0] | CMU Reference Clock Select | I | TTL | Selects the frequency of the CMU reference clock. Bit1 Bit0. 0 0 : 622MHz 0 1 : 311MHz 1 0 : 155MHz 1 1 : 78MHz |
| CMUREFDET | CRU Reference Clock Detect | O | TTL | Reference frequency detect is active high. When this alarm is high it means that the REFCLK input doesn't switch. Status and Interrupt also available through CPU access. |
| CMULOCKDET | CMU Lock Detect | O | TTL | CMU Lock detect is active high. When this alarm is high it means that the REFCLK is in the lock range. Status and Interrupt also available through CPU access. |
| CMUFILTER+/- | CMU Loop Filter | I | - | External CMU loop filter pins. The true loop filter pin is connected via 0.1uF capacitor to the complement loop filter pin. |
| CMUREFCLK +/- | CMU Reference Clock | I | TTL | Differential reference clock to the CMU |
| TLCLKSER +/- | Transmit Clock output | O | TTL | High speed clock output(2.5Gb/s), it is used for retiming the high speed data output |
| TLOUTSER+/- | Transmit Data output | O | PECL or CML | High speed data Clock output |
| TLCLK +/- | Parallel Line Transmit Clock | I | LVDS | Clock reference for the 2.5Gb/s transmit flow carried in TLOUT[3...0]. The clock frequency is nominally 622MHz equivalent to STS-48/STM-16operation (4-bit interface) |
| TLCLKOUT +/- | Parallel Line Transmit Looped Clock | | LVDS | Looped TLCLK signal Timing for this clock is defined with reference to the TLOUT data bus signals. The clock frequency is nominally 622MHz equivalent to STS-48/STM-16 operation (4-bit interface). |
| TLOUT [3..0]+/- | Parallel Line Transmit Data | O | LVDS | Parallel data bus for the outgoing STS-48/STM-16 data stream. TLOUT[3] is the most significant bit. TLOUT[3] is the first transmitted bit on the serial data stream. TLOUT[3...0] is generated on the rising edge of the incoming TLCLK+ (4-bit interface). |

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| <i>Signal</i> | <i>Name</i> | <i>I/O</i> | <i>Type</i> | <i>Description</i> |
|---------------|-------------------------------------|------------|-------------|--|
| TLPRTY +/- | Parallel Line Transmit Parity | O | LVDS | Parity output (even/odd parity) for the parallel transmit data, TLOUT[3...0] is generated on the rising edge of the incoming TLCLK+ (4-bit interface). |
| TLSYNCLDVS+/- | Synchronization | I | LVDS | Can only be used when 4-bit interface is active. |
| TLSYNCTTL | Synchronization | I | TTL | TLSYNC is used for synchronously resetting the device transmit processor only. TLSYNC is intended for use in STS-192/STM-64 applications. |
| PHY4BITSEL | Interface Select | I | TTL | Select between the 4-bit and serial interfaces. Only one of the two can be used at any time. This can also be configured through the CPU interface. |
| LOPC | Loss of Optical Carrier | I | TTL | LOPC is monitored and changes in the signal status may cause generation of an interrupt. This allows monitoring of optical failures via the device CPU interface. When LOPC is asserted, the receive processor is optionally clocked by the transmit clock (derived from TLCLK). |
| RXRCLK | Receive Reference Clock | O | TTL | Reference clock derived from RLCLK in a 78MHz/38MHz/19MHz/8kHz version. |
| TXRCLK | Transmit Reference Clock | O | TTL | Reference clock derived from TLCLK in a 78MHz/38MHz/19MHz/8kHz version. |
| LOS | Loss Of Signal | O | TTL | Status signal indicating if Loss Of Signal (LOS) has been detected. The LOS status is also available in an internal status register bit. The signal is active high. |
| LOF | Loss Of Frame | O | TTL | Status signal indicating if Loss Of Frame (LOF) has been detected. The LOF status is also available in an internal status register bit. The signal is active high. |
| LCD-P | Loss of Cell Delineation | O | TTL | This signal is asserted when the cell delineation state machine is not in SYNC state. This alarm indication is also available via internal register access. |
| RSPFP | Receive Special Purpose Frame Pulse | O | TTL | Frame reference for special purpose serial output ports RSPDAT _x . The frame pulse is a one clock cycle wide pulse coincident with the first bit on the serial dataActive high. RSPFP changes on the falling edge of RSPCLK _x . $x = [1,2]$. |
| RSPCLK1 | Receive Special Purpose Clock 1 | O | TTL | Clock reference for receive special purpose serial output port 1. The clock is a 2.16MHz, 50% duty-cycle signal (optionally gapped to match the bandwidth of RSPDAT1). |
| RSPDAT1 | Receive Special Purpose Data 1 | O | TTL | Data output for special purpose serial port 1. RSPDAT1 changes on the falling edge of RSPCLK1. |

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| <i>Signal</i> | <i>Name</i> | <i>I/O</i> | <i>Type</i> | <i>Description</i> |
|---------------|--|------------|-------------|---|
| RSPVALID1 | Receive Special Purpose Valid 1 | O | TTL | Valid qualifier for special purpose serial port 1. RSPVALID1 is asserted (programmable level) when there is valid data on RSPDAT1. RSPVALID1 changes on the falling edge of RSPCLK1. |
| RSPCLK2 | Receive Special Purpose Clock 2 | O | TTL | Clock reference for receive special purpose serial output port 2. The clock is a 2.16MHz, 50% duty-cycle signal (optionally gapped to match the bandwidth of RSPDAT2). |
| RSPDAT2 | Receive Special Purpose Data 2 | O | TTL | Data output for special purpose serial port 2. RSPDAT2 changes on the falling edge of RSPCLK2. |
| RSPVALID2 | Receive Special Purpose Valid 2 | O | TTL | Valid qualifier for special purpose serial port 2. RSPVALID2 is asserted (programmable level) when there is valid data on RSPDAT2. RSPVALID2 changes on the falling edge of RSPCLK2. |
| RTOHCLK | Receive Transport Overhead Clock | O | TTL | Clock reference for the receive transport overhead port. The clock is a 38.88MHz, 50% duty-cycle signal. |
| RTOHVALID | Receive Transport Overhead Valid | O | TTL | Valid qualifier for the receive transport overhead port. RTOHVALID is asserted (programmable level) when there is valid data on RTOH[3..0]. RTOHVALID changes on the falling edge of RTOHCLK. |
| RTOHFP | Receive Transport Overhead Frame Pulse | O | TTL | Frame reference for the receive transport overhead port. RTOHFP is a one clock cycle wide pulse coincident with the first bit(s) of the first A1 being output on RTOH[3..0]. RTOHFP changes on the falling edge of RTOHCLK. |
| RTOH[3..0] | Receive Transport Overhead Data | O | TTL | Data output for the receive transport overhead (section and line) bytes extracted from the incoming STS-48 signal. RTOH[3..0] changes on the falling edge of RTOHCLK. Mode 1: RTOH[3] carries the transport overhead from STS-12 #1 (first interleaved STS-12), RTOH[2] carries the transport overhead from STS-12 #2, etc. Mode 2: RTOH[3..0] carries the entire transport overhead in the order the overhead bytes are received. The most significant nibble (first received) is output first. RTOH[3] is most significant bit. |
| TSPCLK1 | Transmit Special Purpose Clock 1 | O | TTL | Clock reference for the transmit special purpose serial port 1. The clock is a 2.16MHz, 50% duty-cycle signal (optionally gapped to match the bandwidth of TSPDAT1). |

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| <i>Signal</i> | <i>Name</i> | <i>I/O</i> | <i>Type</i> | <i>Description</i> |
|---------------|--|------------|-------------|---|
| TSPFP1 | Transmit Special Purpose Frame Pulse 1 | O | TTL | Frame reference for the special purpose serial output port TSPDAT1. Mode 1 (TSPCLK1 continuous): The frame pulse is a one clock cycle wide pulse indicating the start of a new data stream on TSPDAT1. When TSPFP1 is asserted, the first bit of TSPDAT1 is sampled on the second rising edge thereafter. TSPFP1 changes on the falling edge of TSPCLK1. Mode 2 (TSPCLK1 gapped): The frame pulse is a one clock cycle wide pulse (variable width due to the gapped clock) indicating the start of a new data stream on TSPDAT1. When TSPFP1 is asserted, the first bit of TSPDAT1 is sampled on the second rising edge thereafter. TSPFP1 changes on the falling edge of TSPCLK1. |
| TSPREN1 | Transmit Special Purpose Read Enable 1 | O | TTL | Read enable signal for the TSPDAT1 data stream. The response latency from TSPREN1 is asserted until TSPDAT1 is sampled is programmable. TSPREN1 changes on the falling edge of TSPCLK1. |
| TSPDAT1 | Transmit Special Purpose Data 1 | I | TTL | Serial data input for transmit special purpose port 1. TSPDAT1 is sampled on the rising edge of TSPCLK1. |
| TSPCLK2 | Transmit Special Purpose Clock 2 | O | TTL | Clock reference for the transmit special purpose serialport 2. The clock is a 2.16MHz, 50% duty-cycle signal (optionally gapped to match the bandwidth of TSPDAT2). |
| TSPFP2 | Transmit Special Purpose Frame Pulse 2 | O | TTL | Frame reference for the special purpose serial output port TSPDAT2. Mode 1 (TSPCLK2 continuous): The frame pulse is a one clock cycle wide pulse indicating the start of a new data stream on TSPDAT2. When TSPFP2 is asserted, the first bit of TSPDAT_2 is sampled on the second rising edge thereafter. TSPFP2 changes on the falling edge of TSPCLK2. Mode 2 (TSPCLK2 gapped): The frame pulse is a one clock cycle wide pulse (variable width due to the gapped clock) indicating the start of a new data stream on TSPDAT2. When TSPFP2 is asserted, the first bit of TSPDAT2 is sampled on the second rising edge thereafter. TSPFP2 changes on the falling edge of TSPCLK2. |
| TSPREN2 | Transmit Special Purpose Read Enable 2 | O | TTL | Read enable signal for the TSPDAT2 data stream. The response latency from TSPREN2 is asserted until TSPDAT2 is sampled is programmable. TSPREN2 changes on the falling edge of TSPCLK2. |
| TSPDAT2 | Transmit Special Purpose Data 2 | I | TTL | Serial data input for transmit special purpose port 2. TSPDAT2 is sampled on the rising edge of TSPCLK2. |
| TTOHCLK | Transmit Transport Overhead Clock | O | TTL | Clock reference for the transmit transport overhead port. The clock is a 38.88MHz, 50% duty-cycle signal. |

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| Signal | Name | I/O | Type | Description |
|------------|---|-----|------|---|
| TTOHFP | Transmit Transport Overhead Frame Pulse | O | TTL | Frame reference for the transmit transport overhead port. TTOHFP is a one clock cycle wide pulse indicating the start of a new data stream on TTOH[3..0]. The response latency from TTOHFP is asserted until the first bit on TTOH[3..0] is sampled is programmable (see TTOHREN). TTOHFP changes on the falling edge of TTOHCLK. |
| TTOHREN | Transmit Transport Overhead Read Enable | O | TTL | Read enable signal for the TTOH[3..0] data stream. The response latency from TTOHREN is asserted until TTOH[3..0] is sampled is programmable. TTOHREN changes on the falling edge of TTOHCLK. |
| TTOHEN | Transmit Transport Overhead Enable | I | TTL | <p>Enable signal for the TTOH[3..0] data stream. If TTOHEN is asserted, the corresponding byte will be inserted in the corresponding transport overhead byte of the outgoing STS-48 data stream.</p> <p>Mode 1: Transport overhead for each of the four STS-12 channels will be input in bit-serial format on the four data inputs (see TTOH[3..0] description). If TTOHEN is asserted during the first bit of an overhead byte, the corresponding overhead byte on TTOH[3] will be enabled, if TTOHEN is asserted during the third bit of an overhead byte, the corresponding overhead byte on TTOH[2] will be enabled (similar for TTOHEN assertion during fifth and seventh bits).</p> <p>Mode 2: Transport overhead for the entire STS-48 is input as 4-bit nibbles on the TTOH[3..0] port (see TTOH[3..0] description). If TTOHEN is asserted during the first nibble of an overhead byte, the corresponding overhead byte is enabled.</p> <p>Note: The transmit section and line processing blocks can selectively overwrite/modify overhead bytes inserted through the TTOH interface.</p> |
| TTOH[3..0] | Transmit Transport Overhead Data | I | TTL | <p>Data input for the transport overhead (section and line) bytes to be inserted in the outgoing STS-48 signal. TTOH[3..0] is sampled on the rising edge of TTOHCLK.</p> <p>Mode 1: TTOH[3] carries the transport overhead for STS-12 #1 (first interleaved STS-12), TTOH[2] carries the transport overhead for STS-12 #2, etc.</p> <p>Mode 2: TTOH[3..0] carries the entire STS-48 transport overhead in the order the overhead bytes are to be inserted. The most significant nibble (first received) is input first. TTOH[3] is the most significant bit.</p> |
| D[7..0] | CPU Data | B | TTL | Bidirectional data bus is used to transfer data for microcontroller read/write access to internal UNI registers. |
| A[8..0] | CPU Address | I | TTL | Address bus selects specific internal registers during register read/write access. |

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| <i>Signal</i> | <i>Name</i> | <i>I/O</i> | <i>Type</i> | <i>Description</i> |
|---------------|-------------------------------|------------|-------------|--|
| ALE | CPU Address Latch Enable | I | TTL | Controls internal latching of the address bus signals. When low the address bus A[8..0] is latched internal. When high the internal address bus latches are transparent. This will allow for interfacing to a multiplexed address/data. The ALE signal has an internal pull-up resistor. |
| CSB | CPU Chip Select (active low) | I | TTL | Must always be asserted during register read/write access cycles. The CSB signal is used in conjunction with either the RDB or the WRB signal. The CSB signal has an internal pull-up resistor. |
| WRB | CPU Write Enable (active low) | I | TTL | Used for register write operations. The D[7..0] content is written into the by A[8..0] selected register when WRB and CSB are both asserted (low). The WRB signal has an internal pull-up resistor. |
| RDB | CPU Read Enable (active low) | I | TTL | Used for register read operations. The D[7..0] will drive register content of the by A[8..0] selected register when RDB and CSB are both asserted (low). The RDB signal has an internal pull-up resistor. |
| INTB | CPU Interrupt (active low) | O | TTL | Asserted when an internal interrupt source is pending and the interrupt is unmasked (enabled). The INTB signal is deasserted when the interrupt pending bits have been cleared. The INTB is an open drain signal. |
| RSTB | Chip Reset (active low) | I | TTL | Asynchronous reset of the device. The device is held in a reset state while the RSTB signal is low. The signal is triggered with an internal pull-up resistor. All outputs are tristated when RSTB is asserted. |
| PMTICK | Performance Monitoring Tick | B | TTL | Output. Asserted when the internal PMTICK timer generates a tick for latching performance counters in the device. Input: A low-to-high transition will (optionally) trigger latching of performance monitoring counters in the device. |
| GPIO[7..0] | General Purpose Input/Output | BI | TTL | Individually configurable as inputs or outputs. Intended for controlling monitoring external devices. |
| TDO | JTAG Test Data Output | O | TTL | This signal carries test data out of the device via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. The TDO signal is a tristate output which is inactive except when data scan shifting is in progress. |
| TDI | JTAG Test Data Input | I | TTL | The signal carries test data into the device via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an internal pull-up resistor. |
| TCK | JTAG Test Clock | I | TTL | This signal provides timing for test operations that are carried out using the IEEE P1149.1 test access port. |
| TMS | JTAG Test Mode Select | I | TTL | This signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an internal pull-up resistor. |

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| Signal | Name | I/O | Type | Description |
|--|--|-----|------|--|
| TRSTB | JTAG Test Reset (active low) | I | TTL | This signal provides an asynchronous test access port reset via the IEEE P1149.1 test access port. TRSTB is a schmitt triggered input with an internal pull-up resistor. |
| OE | Chip Output Enable (active high) | I | TTL | When deasserted (set low), all TTL device outputs are tristated. The OE signal has an internal pull-up. |
| <i>POS Mode:</i> TDAT[31..0] <i>ATM Mode:</i> TUDATA[31..0] | Transmit Packet Data Bus / UTOPIA Transmit Data Bus | I | TTL | <i>POS Mode:</i> Four-octet true data driven from Packet to PHY layer. TDAT[31] is MSB. Packets are aligned to 32 bit TDAT boundary. <i>ATM Mode:</i> Four-octet true data driven from ATM to PHY layer. TUDATA[31] is MSB. |
| <i>POS Mode:</i> TPRTY <i>ATM Mode:</i> TUPRTY | Transmit Bus Parity / UTOPIA Transmit Bus Parity | I | TTL | <i>POS Mode:</i> TPRTY is the odd/even (programmable, default odd) parity bit over TDAT[31..0]. The signal is only valid when asserted simultaneously with TENB. <i>ATM Mode:</i> TUPRTY is the odd/even (programmable, default odd) parity bit over TUDATA[31..0], driven by the ATM layer. The signal is only valid when asserted simultaneously with TUNB*. |
| <i>POS Mode:</i> TMOD[1..0] | Transmit Word Modulo | I | TTL | <i>POS Mode only:</i> Data Qualifier. Qualifier for the four TDAT bytes. Defines which of the four TDAT bytes contains valid data when TEOP and TENB are asserted. Non-EOP words always contains 4 valid TDAT bytes. |
| <i>POS Mode:</i> TSOP <i>ATM Mode:</i> TUSOC | Transmit Start Of Packet / UTOPIA Transmit Start Of Cell | I | TTL | <i>POS Mode:</i> Active high signal asserted by the packet layer when TDAT contains the first valid byte of the packet. The signal is invalid when asserted simultaneously with TENB. The packet interface can be operated without using this signal. <i>ATM Mode:</i> Start Of Cell. Active high signal asserted by the ATM layer when TUDATA contains the first valid byte of the cell. The signal is only valid when asserted simultaneously with TUNB*. |

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| <i>Signal</i> | <i>Name</i> | <i>I/O</i> | <i>Type</i> | <i>Description</i> |
|--|---|------------|-------------|--|
| <i>POS Mode:</i> TEOP | Transmit End Of packet | I | TTL | <i>POS Mode only:</i> Is asserted by the packet layer when TDAT contains the last valid byte of the packet. The signal is only valid when asserted simultaneously with TENB. Active high signal. |
| <i>POS Mode:</i> DTPA <i>ATM Mode:</i> TUFULL*/ TUCLAV | Transmit Polled-PHY Packet Available / Transmit Full/Cell Available | O | TTL | <i>POS Mode:</i> DTPA transitions high when a programmable minimum number of bytes are available in the Tx FIFO. Once high, the DTPA indicates that the Tx FIFO is not full. WHEN DTPA transitions low, it optionally indicates that the Tx FIFO is full or near full. <i>ATM Mode:</i> For UTOPIA flow control. The TUFULL* definition applies to word level flow control, and TUCLAV definition applies to cell level flow control. |
| <i>POS Mode:</i> TERR | Transmit Error Indicator | I | TTL | <i>POS Mode only:</i> May be used to force HDLC frame abortion of insertion of FCS error in the transmitted HDLC/PPP frames. The TERR value is only relevant for the TEOP marked word, and ignored for all other word writes. |
| <i>POS Mode:</i> TENB <i>ATM Mode:</i> TUENB* | Transmit Write Enable / Transmit Write Enable | I | TTL | <i>POS Mode:</i> Active low signal asserted by the packet layer during cycles when TDAT contains valid packet data. <i>ATM Mode:</i> Active low signal asserted by the ATM layer during cycles when TUDATA contains valid cell data. |
| <i>POS Mode:</i> TFCLK <i>ATM Mode:</i> TUCLK | Transmit FIFO Write Clock / Transmit Write Clock | I | TTL | <i>POS Mode:</i> Transfer/synchronization clock provided by the packet layer to the PHY layer for synchronizing transfers on TDAT. <i>ATM Mode:</i> Transfer/synchronization clock provided by the ATM layer to the PHY layer for synchronizing transfers on TUDATA. |
| <i>POS Mode:</i> TFCLKO <i>ATM Mode:</i> TUCLKO | Transmit FIFO Write Clock Looped / Transmit Clock Looped | O | TTL | <i>POS Mode:</i> The TFCLK input looped back out. <i>ATM Mode:</i> The TUCLK input looped back out. |

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| Signal | Name | I/O | Type | Description |
|--|---|-----|------|---|
| <i>POS Mode:</i> RDAT[31..0] <i>ATM Mode:</i> RUDATA[31..0] | Receive Packet Data Bus / Receive Cell Data Bus | O | TTL | <i>POS Mode:</i> Four-octet true data driven from PHY to packet layer. RDAT[31] is MSB. Packets are aligned to 32 bit RDAT boundary. <i>ATM Mode:</i> Four-octet wide data driven from PHY to ATM layer. RUDATA[31] is the MSB. |
| <i>POS Mode:</i> RPRTY <i>ATM Mode:</i> RUPRTY | Receive Bus Parity / Receive Bus Parity | O | TTL | <i>POS Mode:</i> RXPRTY is the odd/even (programmable, default odd) parity bit over RDAT[31..0]. <i>ATM Mode:</i> RUPRTY is the odd/even (programmable, default odd) parity for RUDATA[31..0]. |
| <i>POS Mode:</i> RMOD[1..0] | Receive Word Module | O | TTL | <i>POS Mode only:</i> Data Qualifier. Qualifier for the four RDAT bytes. Defines which of the four RDAT bytes contains valid data. This signal is ignored when REOP is not asserted. |
| <i>POS Mode:</i> RSOP <i>ATM Mode:</i> RUSOC | Receive Start Of Packet / Receive Start Of Cell | O | TTL | <i>POS Mode:</i> Start Of Packet. Is asserted when TDAT contains the first valid byte of the packet. Active high signal. The interface can be operated without using this signal. <i>ATM Mode:</i> Active high signal asserted by the PHY layer when RUDATA contains the first valid byte of a cell. To support multiple PHY configurations. |
| <i>POS Mode:</i> REOP | Receive End Of Packet | O | TTL | <i>POS Mode only:</i> End Of Packet. Is asserted when RDAT contains the last valid byte of the packet. Active high signal. |

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| <i>Signal</i> | <i>Name</i> | <i>I/O</i> | <i>Type</i> | <i>Description</i> |
|---|--|------------|-------------|--|
| <i>POS Mode:</i> RVAL <i>ATM Mode:</i> RUEMPTY*/ RUCLAV | Receive Data Valid / Receive Empty/ Cell Available. | O | TTL | <i>POS Mode:</i> RVAL indicates the validity of the receive data signals. When RVAL is high, the receive signals (RDAT, RSOP, REOP, RMOD, RXPRTY and RERR) are valid. When RVAL is low, all receive signals are invalid and must be disregarded. RVAL will transition low on a FIFO empty condition or on an end of packet. No data will be removed from the receive FIFO while RVAL is deasserted. Once deasserted, RVAL will remain deasserted until current PHY has been deselected. <i>ATM Mode:</i> For UTOPIA flow control. The RUEMPTY* definition applies to word level flow control, and RUCLAV definition applies to cell level flow control. |
| <i>POS Mode:</i> RERR | Receive Error Indicator | O | TTL | <i>POS Mode only:</i> Indicates if the packet contained an error (e.g. Abort/FCS error). This is an active high signal which is asserted during an EOP word. |
| <i>POS Mode:</i> RENB <i>ATM Mode:</i> RUENB | Receive Read Enable / UTOPIA Read Enable | I | TTL | <i>POS Mode:</i> Active low signal asserted by the packet layer to indicate that RVAL, RSOP, RPRTY, RDAT[31..0], RMOD[1..0], REOP, and RERR output signals will be sampled at the end of the next cycle. <i>ATM Mode:</i> Active low signal asserted by the ATM layer to indicate that RUDATA, RUSOC and RPRTY will be sampled at the end of the next cycle. |
| <i>POS Mode:</i> RFCLK <i>ATM Mode:</i> RUCLK | Receive FIFO Write Clock / Receive Clock | I | TTL | <i>POS Mode:</i> Clock. Transfer/synchronization clock provided by the packet layer to the PHY layer for synchronizing transfers on TDAT. <i>ATM Mode:</i> Clock. Transfer/synchronization clock provided by the ATM layer to the PHY layer for synchronizing transfers on RUDATA. |
| <i>POS Mode:</i> RFCLKO <i>ATM Mode:</i> RUCLKO | Receive FIFO Write Clock Looped / Receive Clock Looped | O | TTL | <i>POS Mode:</i> Looped clock. The RXCLK input looped back out. <i>ATM Mode:</i> The RUCLK looped back out. |

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Package Pin List

| Signal | BGA Pin | Signal | BGA Pin | Signal | BGA Pin |
|-----------|---------|-----------|---------|-----------|---------|
| VSSO | A1 | VSSI | A2 | TDAT[20] | A3 |
| TDAT[25] | A4 | VSSI | A5 | TDAT[30] | A6 |
| TMOD[1] | A7 | VSSO | A8 | DTPA | A9 |
| TFCLK | A10 | VSSI | A11 | TTOHREN | A12 |
| TSPFP1 | A13 | VSSO | A14 | TSPDAT1 | A15 |
| TSPCLK1 | A16 | VSSO | A17 | RTOHFP | A18 |
| RSPCLK1 | A19 | VSSO | A20 | RTOH[0] | A21 |
| VSSOR | A22 | VSSI | A23 | VSSI | A24 |
| VSSO | B1 | VSSI | B2 | TDAT[19] | B3 |
| TDAT[22] | B4 | TDAT[27] | B5 | TDAT[28] | B6 |
| TMOD[0] | B7 | VDDO | B8 | TERR | B9 |
| TFCLKO | B10 | TSPREN2 | B11 | TSPFP2 | B12 |
| TSPCLK2 | B13 | VDDO | B14 | TSPREN1 | B15 |
| RTOHCLK | B16 | RSPVALID2 | B17 | RSPCLK2 | B18 |
| RTOHVALID | B19 | RTOH[2] | B20 | TXRCLK | B21 |
| VSSIR | B22 | VSSO | B23 | VSSI | B24 |
| TDAT[16] | C1 | TDAT[17] | C2 | VDDO | C3 |
| TDAT[21] | C4 | TDAT[24] | C5 | TDAT[26] | C6 |
| TDAT[29] | C7 | TPRTY | C8 | TSOP | C9 |
| TENB | C10 | NC_1 | C11 | TTOHFP | C12 |
| TTOHCLK | C13 | TTOHEN | C14 | TTOH[3] | C15 |
| TTOH[1] | C16 | RSPDAT2 | C17 | RSPFP | C18 |
| RTOH[3] | C19 | RSVALID1 | C20 | VDDOR | C21 |
| RLPRTY4- | C22 | RLPRTY4+ | C23 | RLCLK4+ | C24 |
| TDAT[12] | D1 | TDAT[13] | D2 | TDAT[14] | D3 |
| VDDI | D4 | TDAT[18] | D5 | TDAT[23] | D6 |
| VDDI | D7 | VDDO | D8 | TDAT[31] | D9 |
| TEOP | D10 | VDDI | D11 | NC_2 | D12 |
| TSPDAT2 | D13 | VDDI | D14 | TTOH[2] | D15 |
| TTOH[0] | D16 | VDDO | D17 | VDDI | D18 |
| RTOH[1] | D19 | RSPDAT1 | D20 | VDDO | D21 |
| RLIN4[0]- | D22 | RLIN4[1]+ | D23 | RLCLK4- | D24 |
| VSSO | E1 | TDAT[9] | E2 | TDAT[10] | E3 |
| TDAT[15] | E4 | RLIN4[0]+ | E21 | RLIN4[1]- | E22 |
| RLIN4[3]- | E23 | VSSI | E24 | TDAT[6] | F1 |
| TDAT[7] | F2 | TDAT[8] | F3 | TDAT[11] | F4 |
| RLIN4[2]- | F21 | RLIN4[2]+ | F22 | RLIN4[3]+ | F23 |

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| <i>Signal</i> | <i>BGA Pin</i> | <i>Signal</i> | <i>BGA Pin</i> | <i>Signal</i> | <i>BGA Pin</i> |
|---------------|----------------|-----------------|----------------|-----------------|----------------|
| RLINSER- | F24 | TDAT[3] | G1 | TDAT[4] | G2 |
| TDAT[5] | G3 | VDDI | G4 | VDDIR | G21 |
| VDDOR | G22 | VSSOR | G23 | RLINSER+ | G24 |
| VSSO | H1 | VDDO | H2 | TDAT[2] | H3 |
| VDDO | H4 | VSSOA_ DEMUX | H21 | VDDOA_ DEMUX | H22 |
| RLINSERMID | H23 | VSSI | H24 | RDAT[30] | J1 |
| RDAT[31] | J2 | TDAT[0] | J3 | TDAT[1] | J4 |
| CRUREFCLK- | J21 | CRUREFCLK+ | J22 | VSSOA_CRU | J23 |
| CRURECCLK+ | J24 | RDAT[26] | K1 | RDAT[27] | K2 |
| RDAT[28] | K3 | RADT[29] | K4 | VSSO | K21 |
| CRUFILTER+ | K22 | VDDOA_CRU | K23 | CRURECCLK- | K24 |
| VSSO | L1 | RDAT[24] | L2 | RDAT[25] | L3 |
| VDDI | L4 | | | | |
| CMUFILTER+ | L21 | CMUFILTER- | L22 | CRUFILTER- | L23 |
| VSSOA_CMU | L24 | RDAT[23] | M1 | RDAT[22] | M2 |
| RDAT[20] | M3 | RDAT[21] | M4 | VDDOA_CMU | M21 |
| VSSOA_DATA | M22 | CMUREFCLK+ | M23 | TLOUTSER+ | M24 |
| RDAT[16] | N1 | RDAT[19] | N2 | RAT[18] | N3 |
| RDAT[17] | N4 | VDDOA_DATA | N21 | VSSOA_CLK | N22 |
| CMUREFCLK- | N23 | TLOUTSER- | N24 | VSSI | P1 |
| RDAT[15] | P2 | RDAT[14] | P3 | VDDI | P4 |
| VDDOA_CLK | P21 | VDDOA_MUX | P22 | VSSO | P23 |
| TLCLKSER+ | P24 | RDAT[13] | R1 | RDAT[12] | R2 |
| RDAT[11] | R3 | RDAT[10] | R4 | VSSOA_MUX | R21 |
| VSSOT | R22 | VDDOT | R23 | TLCLKSER- | R24 |
| RDAT[9] | T1 | RDAT[8] | T2 | RDAT[7] | T3 |
| RDAT[6] | T4 | TLSYNCLVDS+ | T21 | TLSYNCLVDS- | T22 |
| VDDI | T23 | TLCLK4- | T24 | VSSI | U1 |
| RDAT[6] | U2 | RDAT[4] | U3 | VDDO | U4 |
| VSSI | U21 | TLPRTY4+ | U22 | TLPRTY4- | U23 |
| TLCLK4+ | U24 | RDAT[3] | V1 | RDAT[2] | V2 |
| RDAT[1] | V3 | VDDI | V4 | VSSOT | V21 |
| TLOUT4[0]+ | V22 | TLOUT4[0]- | V23 | TLOUT4[1]- | V24 |
| RDAT[0] | W1 | RMOD[1] | W2 | RMOD[0] | W3 |
| PERR | W4 | TLOUT4[2]+ | W21 | VDDOT | W22 |
| TLOUT4[1]+ | W23 | TLCLKOUT4+ | W24 | VSSI | Y1 |
| VDDO | Y2 | RPRTY | Y3 | REFCLK | Y4 |
| VSSOT | Y21 | TLOUT4[2]- | Y22 | VSSI | Y23 |

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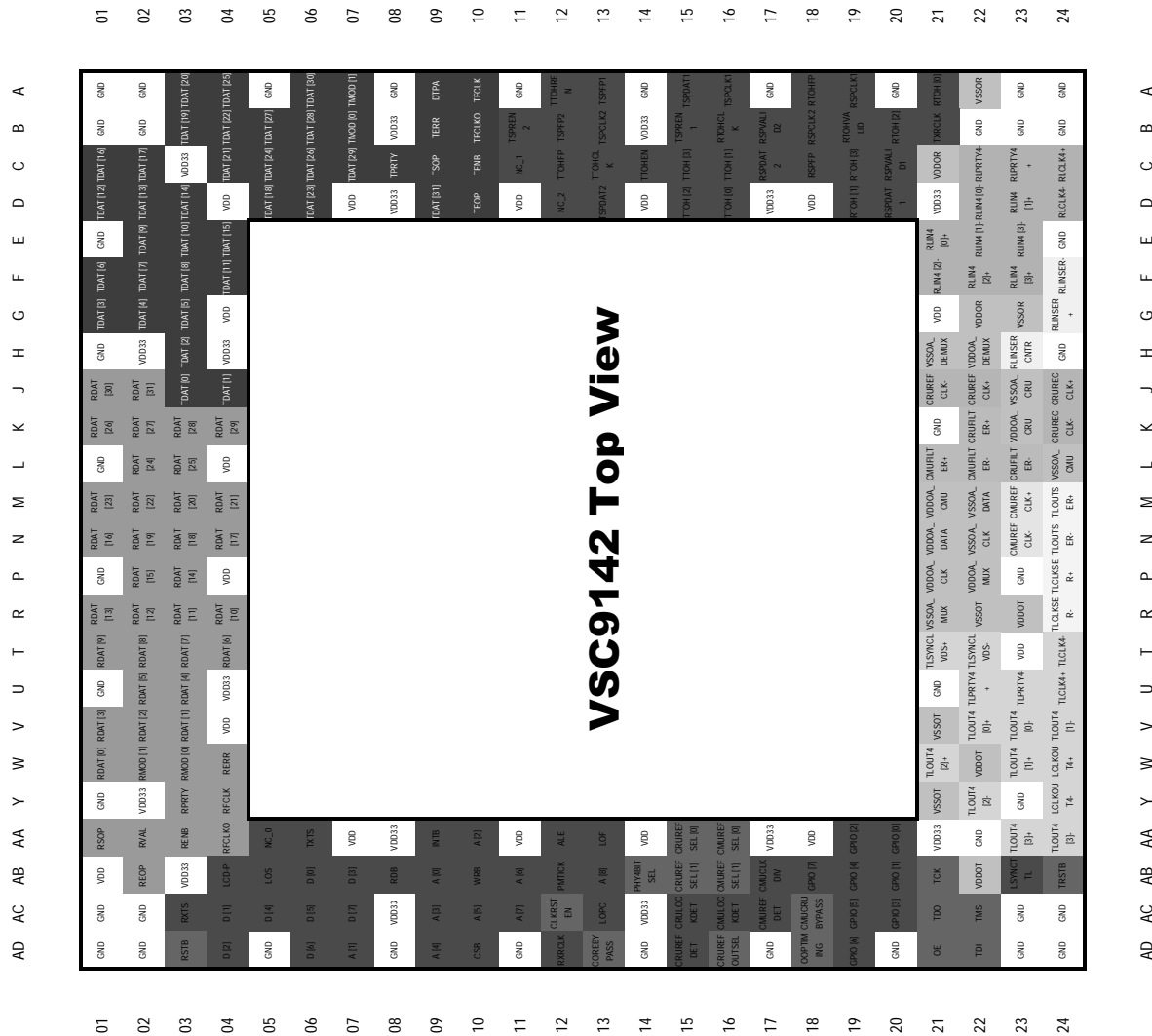
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| Signal | BGA Pin | Signal | BGA Pin | Signal | BGA Pin |
|-----------------|---------|------------|---------|--------------|---------|
| TLCLKOUT4- | Y24 | | | | |
| RSOP | AA1 | RVAL | AA2 | RENB | AA3 |
| RFCLKO | AA4 | NC_0 | AA5 | TXTS | AA6 |
| VDDI | AA7 | VDDO | AA8 | INTB | AA9 |
| A[2] | AA10 | VDDI | AA11 | ALE | AA12 |
| LOF | AA13 | VDDI | AA14 | CRUREFSEL[0] | AA15 |
| CMUREFSEL[0] | AA16 | VDDO | AA17 | VDDI | AA18 |
| GPIO[2] | AA19 | GPIO[0] | AA20 | VDDO | AA21 |
| VSSIT | AA22 | TLOUT4[3]+ | AA23 | TLOUT4[3]- | AA24 |
| VDDI | AB1 | REOP | AB2 | VDDO | AB3 |
| LCD-P | AB4 | LOS | AB5 | D[0] | AB6 |
| D[3] | AB7 | RDB | AB8 | A[0] | AB9 |
| WRB | AB10 | A[6] | AB11 | PMTICK | AB12 |
| A[8] | AB13 | SELLINE4 | AB14 | CRUREFSEL[1] | AB15 |
| CMUREFSEL[1] | AB16 | CMUCLKDIV | AB17 | GPIO[7] | AB18 |
| GPIO[4] | AB19 | GPIO[1] | AB20 | TCK | AB21 |
| VDDOT | AB22 | TLSYNCTTL | AB23 | TRSTB | AB24 |
| VSSI | AC1 | VSSI | AC2 | RXTS | AC3 |
| D[1] | AC4 | D[4] | AC5 | D[5] | AC6 |
| D[7] | AC7 | VDDO | AC8 | A[3] | AC9 |
| A[5] | AC10 | A[7] | AC11 | CLKRSTEN | AC12 |
| LOPC | AC13 | VDDO | AC14 | CRULOCKDET | AC15 |
| CMULOCKDET | AC16 | CMUREFDET | AC17 | CMUCRUBYPASS | AC18 |
| GPIO[5] | AC19 | GPIO[3] | AC20 | TDO | AC21 |
| TMS | AC22 | VSSI | AC23 | VSSI | AC24 |
| VSSI | AD1 | VSSO | AD2 | RSTB | AD3 |
| D[2] | AD4 | VSSO | AD5 | D[6] | AD6 |
| A[1] | AD7 | VSSI | AD8 | A[4] | AD9 |
| CSB | AD10 | VSSI | AD11 | RXRCLK | AD12 |
| COREBYPASS | AD13 | VSSO | AD14 | CRUREFDET | AD15 |
| CRUCLKDIVREFSEL | AD16 | VSSI | AD17 | LOOPIMING | AD18 |
| GPIO[6] | AD19 | VSSO | AD20 | OE | AD21 |
| TDI | AD22 | VSSO | AD23 | VSSI | AD24 |

TS-48c Packet/ATM Over SONET/SDH Device
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Package Pin Layout

Figure 11: Top View Pin Layout

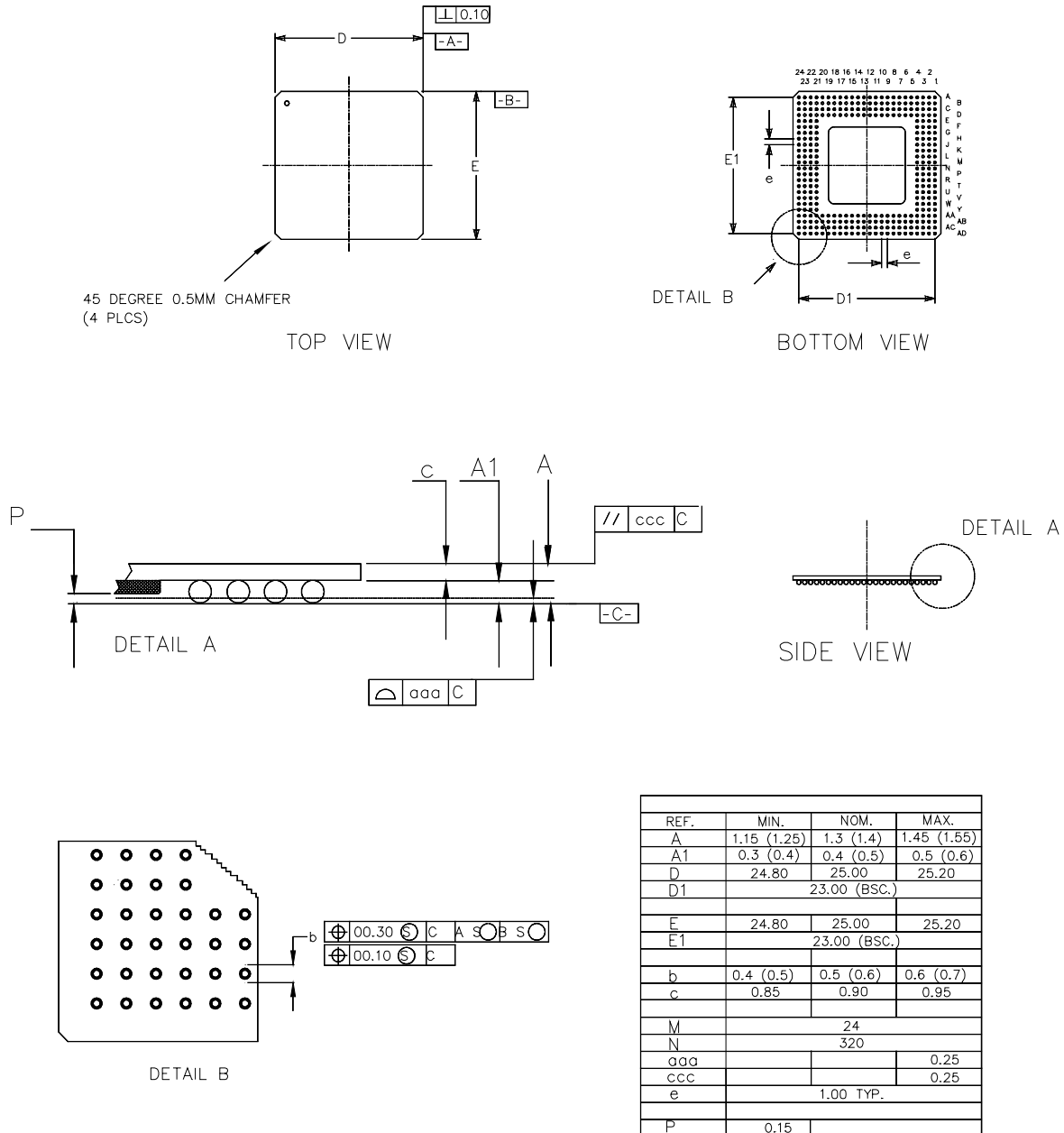


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Package Information

Figure 12: 320-pin TBGA



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Package Thermal Characteristics

| Parameter | Description | (Typ) | Units |
|---------------------|------------------------|-------|-------|
| Th _{JA} | Theta J/A in Still Air | 12.0 | C/W |
| Th _{JA200} | Theta J/A at 200 LFPM | 10.0 | C/W |
| Th _{JC} | Theta J/C | 0.22 | C/W |

Ordering Information

The ordering number for this product is formed by a combination of the device number and package type.

VSC9142 **TBD**

Device Type

VSC9142 - 2.5Gb/s POS/ATM Framer with Integrated Mux/Demux and Clock and Data Recovery

Package Type

TBD - 320-pin TBGA

Notice

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