

SN54279, SN54LS279A, SN74279, SN74LS279A QUADRUPLE S-R LATCHES

SDLS093 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

description

The '279 offers 4 basic \bar{S} - \bar{R} flip-flop latches in one 16-pin, 300-mil package. Under conventional operation, the \bar{S} - \bar{R} inputs are normally held high. When the \bar{S} input is pulsed low, the Q output will be set high. When \bar{R} is pulsed low, the Q output will be reset low. Normally, the \bar{S} - \bar{R} inputs should not be taken low simultaneously. The Q output will be unpredictable in this condition.

FUNCTION TABLE
(each latch)

INPUTS		OUTPUT
\bar{S}^\dagger	\bar{R}	Q
H	H	Q_0
L	H	H
H	L	L
L	L	H^\ddagger

H = high level L = low level

† For latches with double S inputs:

Q_0 = the level of Q before the indicated input conditions were established.

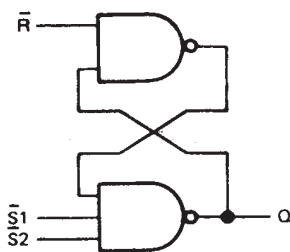
‡ This configuration is nonstable: that is, it may not persist when the \bar{S} and \bar{R} inputs return to their inactive (high) level.

H = both \bar{S} inputs high

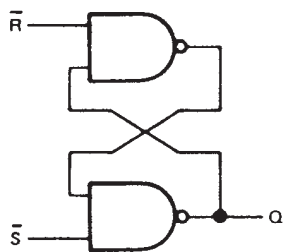
L = one or both \bar{S} inputs low

logic diagram (positive logic)

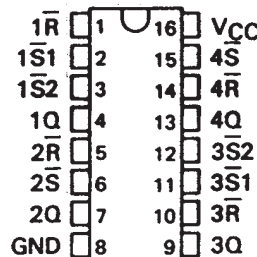
(latches 1 and 3)



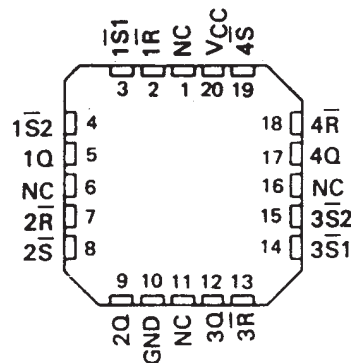
(latches 2 and 4)



SN54279, SN54LS279A . . . J OR W PACKAGE
SN74279 . . . N PACKAGE
SN74LS279A . . . D OR N PACKAGE
(TOP VIEW)

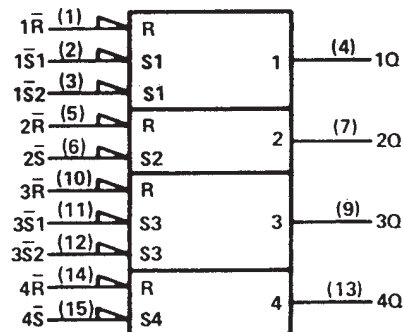


SN54LS279A . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

logic symbol[§]



[§]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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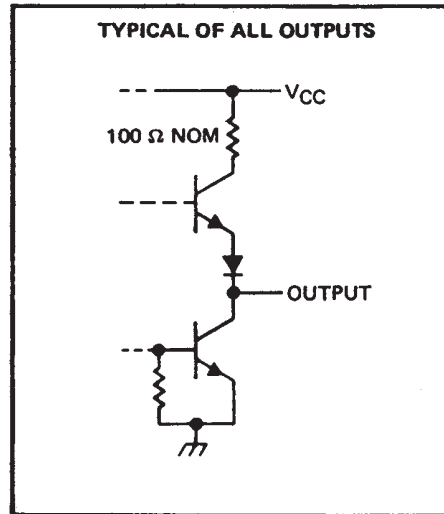
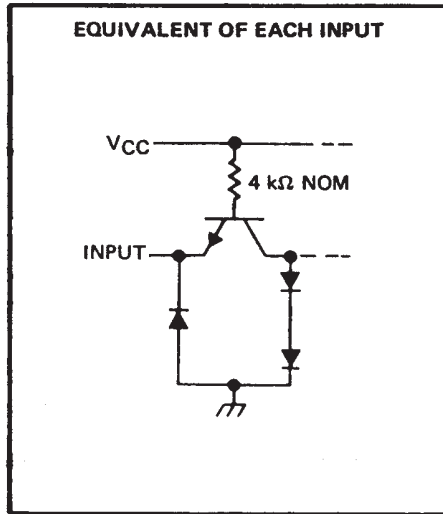
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SN54279, SN54LS279A, SN74279, SN74LS279A QUADRUPLE S-R LATCHES

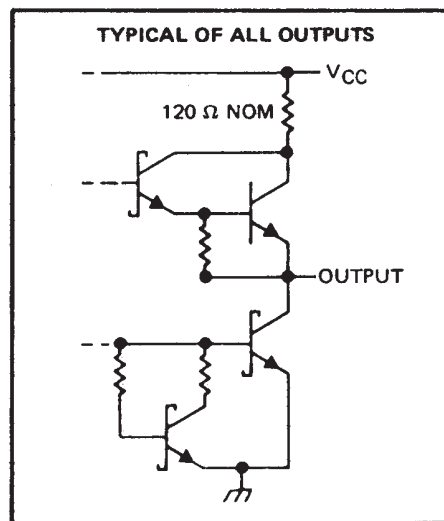
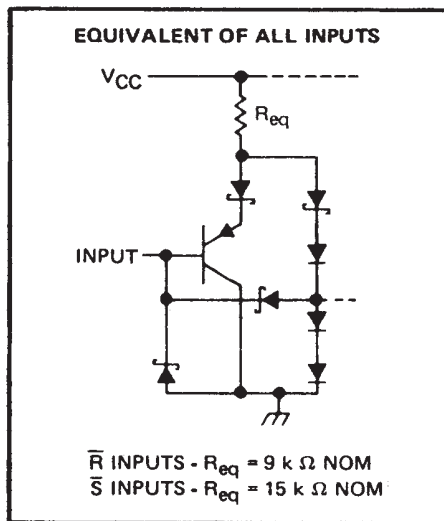
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schematics of inputs and outputs

'279 CIRCUITS



'LS279A CIRCUITS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '279	5.5 V
'LS279A	7 V
Operating free-air temperature range: SN54' TYPES	- 55° C to 125° C
SN74' TYPES	0° C to 70° C
Storage temperature range	- 65° C to 150° C

NOTE 1: Voltage values are with respect to network ground terminal.



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recommended operating conditions

	SN54279			SN74279			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage	0.8			0.8			V
I _{OH} High-level output current	-0.8			-0.8			mA
I _{OL} Low-level output current	16			16			mA
t _w Pulse duration, low	20			20			ns
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54279			SN74279			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -12 mA	-1.5			-1.5			V
V _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -0.8 mA	2.4	3.4		2.4	3.4	V	
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 16 mA	0.2	0.4		0.2	0.4	V	
I _I	V _{CC} = MAX, V _I = 5.5 V	1			1			mA
I _{IH}	V _{CC} = MAX, V _I = 2.4 V	40			40			μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V	-1.6			-1.6			mA
I _{OS} §	V _{CC} = MAX	-18	-55		-18	-57	mA	
I _{CC}	V _{CC} = MAX, See Note 2	18	30		18	30	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all R inputs grounded, all S inputs at 4.5 V, and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	S̄	Q	R _L = 400 Ω, C _L = 15 pF		12	22	ns
t _{PHL}	S	Q			9	15	
t _{PHL}	R̄	Q			15	27	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN54279, SN54LS279A, SN74279, SN74LS279A QUADRUPLE S-R LATCHES

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recommended operating conditions

	SN54LS279A			SN74LS279A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.7			0.8	V
I _{OH} High-level output current			-0.4			-0.4	mA
I _{OL} Low-level output current			4			8	mA
t _w Pulse duration, low	20			20			ns
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS279A			SN74LS279A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = -0.4 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 8 mA					0.25	0.5	
I _I	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			20			20	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			-0.2			-0.2	mA
I _{OS} §	V _{CC} = MAX	-20		-100	-20		-100	mA
I _{CC}	V _{CC} = MAX, See note 2		3.8	7		3.8	7	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should be less than one second.

NOTE 2: I_{CC} is measured with all R inputs grounded, all S inputs at 4.5 V, and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	S	Q	R _L = 2 kΩ, C _L = 15 pF		12	22	ns
t _{PHL}					13	21	
t _{PHL}	R	Q			15	27	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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PRODUCT SUPPORT: [TRAINING](#)

SN54LS279A, Quadruple /S-/R Latches

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54LS279A	SN74LS279A
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-0.4/8
Output	2S	2S
No. of Bits	4	4
tpd max (ns)		22

FEATURES

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- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

DESCRIPTION

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The '279 offers 4 basic S\R flip-flop latches in one 16-pin, 300-mil package. Under conventional operation, the S\R inputs are normally held high. When the S input is pulsed low, the Q output will be set high. When R is pulsed low, the Q output will be reset low. Normally, the S\R inputs should not be taken low simultaneously. The Q output will be unpredictable in this condition.

TECHNICAL DOCUMENTS

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To view the following documents, [Acrobat Reader 4.0](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: [sn54ls279a.pdf](#) (162 KB) (Updated: 03/01/1988)

APPLICATION NOTES

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View Application Notes for [Digital Logic](#)

- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)
- [Designing with the SN54/74LS123 \(Rev. A\)](#) (SDLA006A - Updated: 03/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
- [TI IBIS File Creation, Validation, and Distribution Processes](#) (SZZA034 - Updated: 08/29/2002)
- [Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sheet \(Rev. A\)](#) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

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- [Enhanced Plastic Portfolio Brochure](#) (SGZB004, 387 KB - Updated: 08/19/2002)

- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [Military Brief](#) (SGYN138, 803 KB - Updated: 10/10/2000)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\)](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- [Palladium Lead Finish User's Manual](#) (SDYV001, 2041 KB - Updated: 11/01/1996)
- [QML Class V Space Products Military Brief \(Rev. A\)](#) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

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- [LOGIC Pocket Data Book](#) (SCYD013, 4837 KB - Updated: 12/05/2002)

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION Updated Daily								TI INVENTORY STATUS As Of 09:00 AM GMT, 17 Apr 2003			REPORTED DISTRIBUTOR INVENTORY As Of 09:00 AM GMT, 17 Apr 2003		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY SUS	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
76018012A	ACTIVE	LCCC (FK) 20	-55 TO 125		View Contents	1KU 6.94	1	0*	4066 20 May	6 WKS	None Reported View Distributors		
									> 10k 27 May				
7601801EA	ACTIVE	CDIP (J) 16	-55 TO 125		View Contents	1KU 2.00	1	0*	> 10k 20 May	6 WKS	Avnet Americas	41	BUY NOW
7601801FA	ACTIVE	CFP (W) 16	-55 TO 125		View Contents	1KU 7.29	1	45*	> 10k 20 May	6 WKS	Avnet Americas	149	BUY NOW
SN54LS279AJ	ACTIVE	CDIP (J) 16	-55 TO 125		View Contents	1KU 1.70	1	398*	279 05 May	6 WKS	Avnet-SILICA Europe	28	BUY NOW
									> 10k 20 May		Avnet Americas	12	BUY NOW
SNJ54LS279AFK	ACTIVE	LCCC (FK) 20	-55 TO 125	76018012A	View Contents	1KU 6.94	1	97*	3580 20 May	6 WKS	None Reported View Distributors		
									> 10k 27 May				
SNJ54LS279AJ	ACTIVE	CDIP (J) 16	-55 TO 125	7601801EA	View Contents	1KU 2.00	1	166*	> 10k 20 May	6 WKS	Avnet-SILICA Europe	39	BUY NOW
SNJ54LS279AW	ACTIVE	CFP (W) 16	-55 TO 125	7601801FA	View Contents	1KU 7.29	1	0*	> 10k 20 May	6 WKS	None Reported View Distributors		

Table Data Updated on: 4/17/2003