

TECHNICAL DATA
DATA SHEET 1150, REV. -

Low Capacitance Data I/O Protector for High-Speed Telecommunications Systems

Description:

The SDLP100-7 transient voltage suppressor is designed to protect components which are connected to high speed telecommunication lines from voltage surges caused by lightning, electrostatic discharge (ESD), and electrical fast transients (EFT).

The SDLP100-7 is designed for metallic mode, secondary line side protection in digital line card applications. It features solid-state technology for unmatched transient protection without device degradation.

The SDLP100-7 is suitable for use on T1/E1 and xDSL interfaces in equipment such as base stations, routers, and channel service units.

Features:

- Transient protection for high speed data lines meeting surge requirements 1,2,3 of Bellcore 1089, and surge requirements 1,2,3 of FCC Part 68
- Low capacitance for high speed interfaces
- Low operating and clamping voltage
- Integrated structure saves board space and increases reliability
- Solid-state technology

Mechanical Characteristics:

- Molding compound flammability rating: UL 94V-0
- Marking: Part number, date code, logo

Applications:

- T1/E1 Line Cards
- Base Stations
- WAN Interfaces
- XDSL Interfaces
- CSU/DSU Equipment

Absolute Maximum Rating

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Maximum Surge Current, pulse width <1 msec	I _{Sp}	-	-	150	A (peak)
Operating Temperature	T _{OP}	-55	-	+125	°C
Storage Temperature	T _{STG}	-55	-	+150	°C

Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Input Leakage Specifications					
Leakage Current Between Any Two Pins @ V _{bias} =2.5V	I _L	-	-	200	µA
Leakage Current Between Any Two Pins @ V _{bias} =3.5V	I _L	-	-	300	µA
Clamping Voltage Specifications					
Clamping Voltage Between Any Two Pins @ I _C =0.1A	V _{CL}	-	-	4.5	V
Clamping Voltage Between Any Two Pins @ I _C =10A	V _{CL}	-	-	5.0	V
Clamping Voltage Between Any Two Pins @ I _C =50A	V _{CL}	-	-	5.8	V
Clamping Voltage Between Any Two Pins @ I _C =80A	V _{CL}	-	-	6.4	V
Clamping Voltage Between Any Two Pins @ I _C =100A	V _{CL}	-	-	6.7	V
Clamping Voltage Between Any Two Pins @ I _C =120A	V _{CL}	-	-	7.2	V
Clamping Voltage Between Any Two Pins @ I _C =130A	V _{CL}	-	-	7.3	V
Input Capacitance Specifications					
Input Capacitance Between Any Two Pins @ V _R =2V	C _I	-	-	40	pF

SENSITRON

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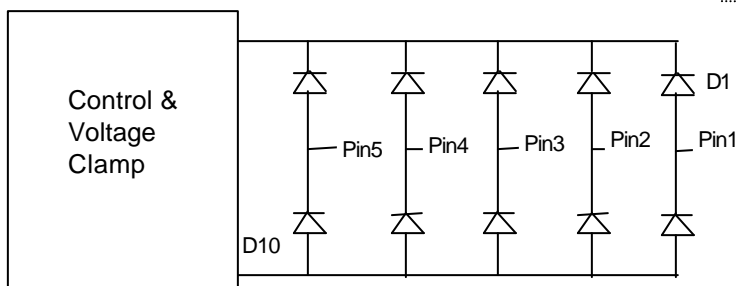
GR-1089 CORE Surges

Surge	Minimum Peak Voltage (Volts)	Minimum Peak Current Per Conductor (Amps)	Maximum Rise Time and Minimum Decay Time (mS)
1	±600	100	10 / 1000
2	±1000	100	10 / 360
3	±1000	100	10 / 1000
4	±1000	25	10 / 360

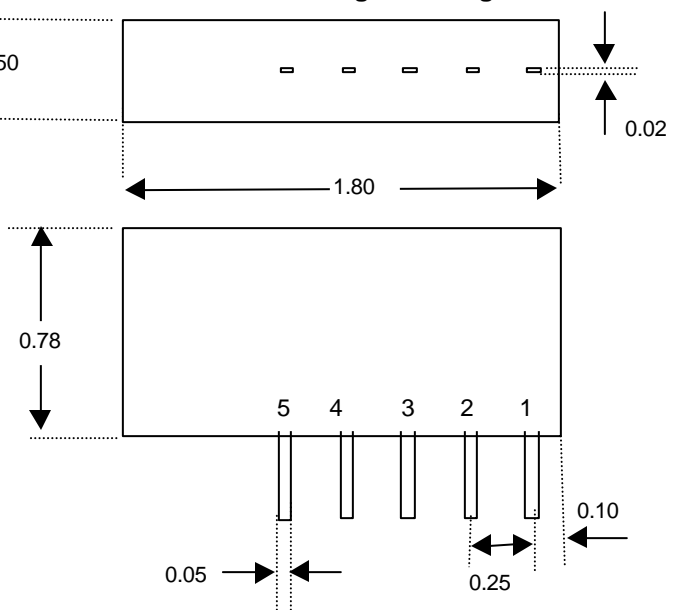
FCC Surges -- FCC Title 47, CFR, Part 68

Surge	Type of Surge	Minimum Peak Voltage (Volts)	Minimum Peak Current per Conductor (Amps)	Maximum Rise Time and Minimum Decay Time (mS)
1	Metallic	±1000	25	10 / 700
2	Longitudinal	±1500	37.5	10 / 700
3	Metallic	±800	100	10 / 560

Schematic Diagram:



Package Drawing:



Typ. Clamping Voltage vs. Surge Current:

