Zilog

PRELIMINARY
Product Specification

October 1988

T-49-17-07

Z320™ CPU

FEATURES

- Full 32-bit architecture and implementation
- 4G (billion) bytes of directly addressable memory in each of four address spaces
- Linear or segmented address space
- Virtual memory management integrated with CPU
- On-chip cache memory
- General-purpose register file with sixteen 32-bit registers
- Nine general addressing modes
- Numerous data types include bit, bit field, logical value, signed integer, and string
- Regular use of operations, addressing modes, and data types in instruction set
- System and normal modes of operation with separate stacks
- Sophisticated interrupt and trap handling
- Software is a binary-compatible extension of Z8000® software, totally compatible with the Z80,000®
- Small, low cost 68-pin plastic leaded chip carrier package for surface mount applications
- Hardware is compatible with other Z-BUS® bus components with multiplexed address and data
- Mainframe performance at a micro price

GENERAL DESCRIPTION

The Z320 CPU is an advanced, high-end 32-bit microprocessor that integrates the architecture of a mainframe computer into a single chip. While maintaining full compatibility with Z8000 family software and hardware, the Z320 CPU offers greater power and flexiblity in both its architecture and interface capability. Operating systems and compilers are easily developed in the Z320 CPU's high-quality environment, and the hardware interface provides for connection to a wide variety of system configurations.

Adddresses in the Z320 CPU are 32 bits. This allows direct addressing of 4G bytes in each of four address spaces: system-mode data, system-mode instruction, normal-mode data, and normal-mode instruction. The CPU supports three modes of address representation. The 16-bit compact addresses are compatible with Z8000 nonsegmented mode. The 32-bit segmented addresses include both 16-bit offset, which is compatible with Z8000 segmented mode, and 24-bit offset. In addition, a full 32-bit linear address space is provided.

The CPU features a general-purpose register file with sixteen 32-bit registers and nine operand addressing choices for compact representation or for full 32-bit addressing. The instruction set can operate on bit, bit field, logical value, signed integer, unsigned interger, address, string, stack, and packed decimal byte data types. Logical and arithmetic instructions operated on bytes (8 bits), words (16 bits) and longwords (32 bits). The Extended Processing Architecture (EPA) supports highly regular in combining operations, data types, and addressing modes. High-level language compilation is supported with instructions for procedure linkage, array index calculation, and bounds checking. Other instructions provide operating system functions such as system call and control of memory management.

There are two main operating modes, system and normal, supported by separate stacks. User programs operate in normal mode, while sensitive operating system functions are performed in system mode. This protects critical parts of the operating system from user access. In addition, some instructions are priveleged, and execute only in system mode. Memory management functions protect both system memory from user programs, and user memory from other users. Vectored, nonvectored, and nonmaskable interrupts support realtime operating systems.

Memory managmement is fully integrated with the CPU; no external support circuitry is necessary. A paging address translation mechanism is implemented. Registers in the CPU point to address translation tables located in memory; the most recently used table entries are kept in a Translation Lookaside Buffer (TLB) in the CPU. The CPU performs logical to physical address translation and access protection for each memory reference. When a logical memory reference causes a translation or protection violation, the state of the CPU is automatically restored to restart the instruction. I/O ports can be referenced either by dedicated instructions or by the memory management mechanism mapping logical memory addresses to I/O port addresses.

Extensive trapping facilities, such as integer overflow, subrange out of bounds, and subscript out of bounds, catch common run-time errors. Software debuggers can use trace and breakpoint traps. Privileged instruction traps and memory protection violation traps secure the operating system from user programming errors or mischief. The overflow stack allows recovery from otherwise fatal errors.

The CPU has full 32-bit internal address and data paths. Externally, 32 pins time-multiplex the address and data. The interface is compatible with the complete line of Z-BUS peripherals. The hardware interface features 16-bit or 32-bit memory data path and programmable wait states. Burst transfers and an on-chip cache for instructions and data help develop high-performance systems. The interface supports multiprocessing configurations with interlocked memory references and two types of bus request protocols. The system designer can tailor the Z320 based system to cost and performance needs.

In summary, the Z320 CPU meets and surpasses the requirements of medium and high-end microprocessor systems for the 1980s. Software program development is easily accomplished with the CPU's sophisticated architecture. The highly pipelined design, on-chip cache, and external interface support systems ranging from dedicated controllers to mainframe computers. While Zilog continues to develop support for the Z320 CPU, Z8000 peripherals and development software are fully compatible with this latest in Zilog's line of high-performance microprocessors.

REGISTERS

The Z320 CPU is a register-oriented processor offering sixteen 32-bit general-purpose registers, a 32-bit Program Counter (PC), a 16-bit Flag and Control Word (FCW), and nine other special-purpose registers.

The general-purpose register file (Figure 1) contains 64 bytes of storage. The first 16 bytes (RL0,RH0,...,RL7,RH7) can be used as accumulators for byte data. The first 16 words (R0,R1,...,R15) can be used as accumulators for word data, as index registers (except R0), or for memory addresses in compact mode (except R0). Any longword register (RR0,RR2,...,RR30) can be used as an accumulator for longword data, an index register in linear or segmented mode (except RR0), or for memory addresses in linear or segmented mode (except RR0). Quadword registers (RQ0,RQ4,...,RQ28) can be used as accumulators for Multiply, Divide, and Extend Sign instructions. This unique register organization allows bytes and words of data to be manipulated conveniently while leaving most of the register file free to hold addresses, counters, and any other data.

Two registers are dedicated to the Stack Pointer (SP) and Frame Pointer (FP) used by Call, Enter, Exit, and Return and R14 the Frame Pointer. In linear or segmented mode, RR14 is the Stack Pointer and RR12 is the Frame Pointer.

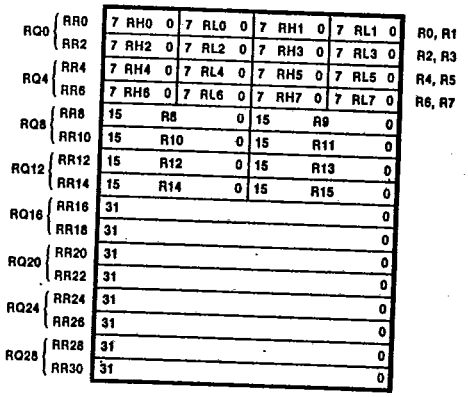

Figure 1. General-Purpose Register File

CACHE

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The CPU implements a cache mechanism to keep on-chip copies of the most recently referenced memory locations (Figure 12). The CPU examines the cache on memory fetches to determine if the addressed data are located in the cache. If the information is in the cache (a hit), then the CPU fetches from the cache, and no transaction is necessary on the external interface. If the information is not in the cache (a miss), then the CPU performs a memory read transaction to fetch the missing information.

The cache stores data in blocks of 16 bytes. Each data word in the cache has an associated validity bit to indicate whether or not the word is a valid copy of the corresponding main memory location. The cache contains 16 blocks, providing 256 bytes of storage.

The cache is fully associative, so that a block currently needed and missing in the cache can replace any block in the cache. Moreover, when a block miss occurs, the least recently used (LRU) block in the cache is replaced. When a cache miss occurs on an instruction fetch, the CPU fetches the missing instruction from memory and prefetches the following words in the block using a burst transaction. When a cache miss occurs on an operand fetch, the CPU fetches the missing data from memory. (The CPU uses burst transactions only for fetching operands when more than one data transfer is necessary: longword operands on a 16-bit bus, unaligned operands, string instructions, Load Multiple instructions, and loading Program Status.)

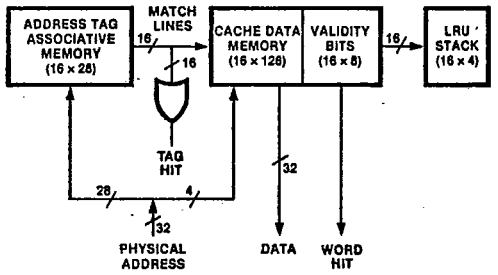

Figure 2. Cache Organization

On store references, the data is written to memory (store through), and if the reference hits in the cache, the data is also written to the cache. If the store reference misses in the cache, the cache is unaffected.

Software has some control over the cache. The cache can be selectively enabled for instruction and data references by bits CI and CD in the SCCL control register. The memory management mechanism allows cacheing to be inhibited for individual pages. The Pcache instruction can be used to invalidate all information in the cache.

The cache has an option, controlled by bit CR in SCCL, to inhibit block replacement on a miss. This option can be used to lock fixed locations into the cache for fast, onchip access. To do this, the cache is first enabled for block replacement of data references only. Selected blocks are read into the cache. The block replacement algorithm is then disabled, while the cache is enabled for instruction and data references.

PIN DESCRIPTIONS

The CPU has 58 signal lines and additional power supply connections. Pin functions are shown in Figure 3a, b, c.

AD_0-AD_{31}. *Address/Data (Bidirectional, active High, 3-state).* These 32 lines are time-multiplexed to transfer address and data. At the beginning of each transaction the lines are driven with the 32-bit address. After the address has been driven, the lines are used to transfer one or more bytes, words, or longwords of data.

$\overline{AS}$. *Address Strobe (Output, active Low, 3-state).* The falling edge of $\overline{AS}$ indicates the beginning of a transaction and shows that the address and ST_0-ST_3, are valid. R/$\overline{W}$, BL/$\overline{W}$, BW/$\overline{L}$, and $\overline{BRST}$ are valid on the rising edge of $\overline{AS}$.

BL/$\overline{W}$; BW/$\overline{L}$. *Byte, Longword/Word; Byte, Word/Longword (Output, 3-state).* These two lines specify the data transfer size.

BL/$\overline{W}$	BW/$\overline{L}$	Size
High	High	Byte
Low	High	Word
High	Low	Longword
Low	Low	Reserved

$\overline{BRST}$. *Burst (Output, active Low, 3-state).* A Low on this line indicates that the CPU is performing a burst transfer; i.e, multiple Data Strobes following a single Address Strobe.

$\overline{BRSTA}$. *Burst Acknowledge (Input, active Low).* A Low on this line indicates that the responding device can support burst transfers.

$\overline{BUSACK}$. *Bus Acknowledge (Output, active Low).* A Low on this line indicates that the CPU has relinquished control of the local bus in response to a bus request.

$\overline{BUSREQ}$. *Bus Request (Input, active Low).* A Low on this line indicates that a bus requestor has obtained or is trying to obtain control of the local bus.

CLK. *Clock (Input).* This is the clock used to generate all CPU timing.

$\overline{DS}$. *Data Strobe (Output, active Low, 3-state).* DS is used for timing data transfers.

EPUABORT. ***EPU Abort (Output, active High).*** **A High on this line indicates that the CPU is aborting execution of an EPA instruction, typically because an Address Translation trap has occurred.**

$\overline{EPUBSY}$. *EPU Busy (Input, active Low).* A Low on this line indicates that an EPU is busy. This line is used to synchronize the operation of the CPU with an EPU during execution of an EPA instruction.

$\overline{GACK}$. *Global Acknowledge (Input, active Low).* A Low on this line indicates the CPU has been granted control of a global bus.

$\overline{GREQ}$. *Global Request (Output, active Low, 3-state).* A Low on this line indicates the CPU has obtained or is trying to obtain control of a global bus.

$\overline{IE}$. *Input Enable (Output, active Low, 3-state).* A Low on this line can be used to enable buffers on the AD lines to drive toward the CPU.

$\overline{NMI}$. *Non-Maskable Interrupt (Input, Edge activated).* A High-to-Low transition on this line requests a nonmaskable interrupt.

$\overline{NVI}$. *Non-Vectored Interrupt (Input, active Low).* A Low on this line requests a non-vectored interrupt.

$\overline{OE}$. *Output Enable (Output, active Low, 3-state).* A Low on this line can be used to enable buffers on the AD lines to drive away from the CPU.

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$\overline{RESET}$. *Reset (Input, active Low).* A Low on this line resets the CPU.

RSP_0-RSP_1. *Response (Input).* These lines encode the response to transactions initiated by the CPU. Note that RSP_0 and RSP_1 can be connected together for Z-BUS $\overline{WAIT}$ timing.

RSP_0	RSP_1	Response
High	High	Ready
Low	High	Bus Error
High	Low	Bus Retry
Low	Low	Wait

R/$\overline{W}$. *Read/Write (Output, Low = Write, 3-state).* This signal indicates the direction of data transfer.

ST_0-ST_3. *Status (Output, active High, 3-state).* These lines specify the kind of transaction occurring on the bus. (See Table 5.)

VBB. *Substrate Bias Generator* (Output, for internal biasing only).

$\overline{VI}$. *Vectored Interrupt (Input, active Low).* A Low on this line requests a vectored interrupt.

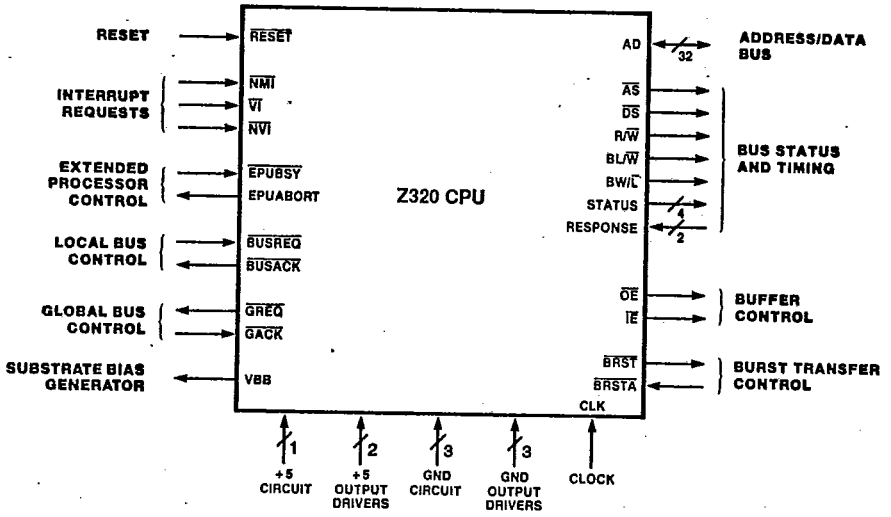

Figure 3a. Pin Functions

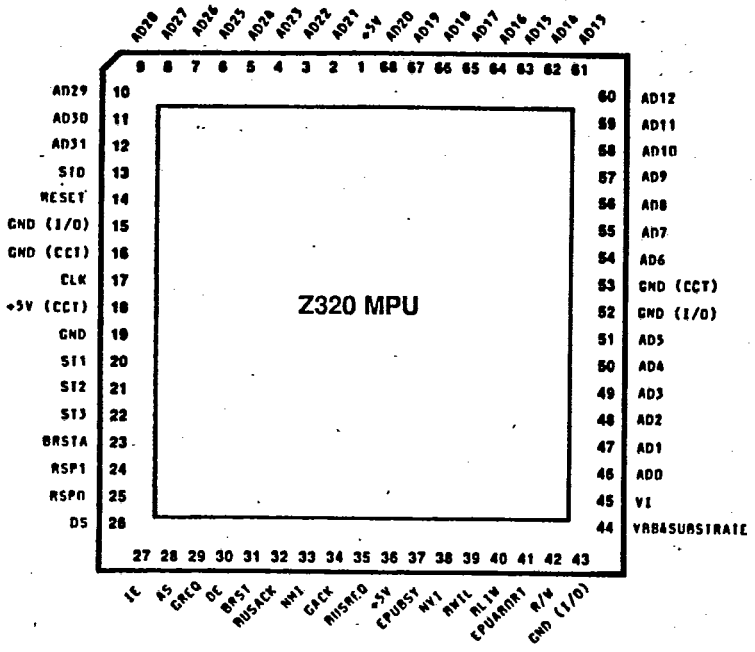

Figure 3b.

PIN ASSIGNMENT FOR Z320 IN 68-PIN PLCC PACKAGE

PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION
10	AD29	27	IE	44	VBBASUBSTRATE	61	AD13
11	AD30	28	AS	45	VI	62	AD14
12	AD31	29	GREQ	46	AD0	63	AD15
13	SIO	30	OE	47	AD1	64	AD16
14	RESET	31	BRST	48	AD2	65	AD17
15	GND (I/O)	32	BUSACK	49	AD3	66	AD18
16	GND (CCT)	33	NMI	50	AD4	67	AD19
17	CLK	34	CACK	51	AD5	68	AD20
18	+5V (CCT)	35	BUSREQ	52	GND (I/O)	1	+5V
19	GND	36	+5V	53	GND (CCT)	2	AD21
20	SI1	37	EPUBSY	54	AD6	3	AD22
21	SI2	38	NVI	55	AD7	4	AD23
22	SI3	39	NVIL	56	AD8	5	AD24
23	BRSTA	40	BLIN	57	AD9	6	AD25
24	RSP1	41	EPUABORT	58	AD10	7	AD26
25	RSP0	42	R/W	59	AD11	8	AD27
26	DS	43	GND (I/O)	60	AD12	9	AD28

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Figure 3c.

ABSOLUTE MAXIMUM RATINGS

Voltages on all inputs and outputs with respect to GND . . . . . −0.3V to +7.0V
Operating Ambient Temperature . . . . . See ordering information
Storage Temperature . . . . . −65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only: operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

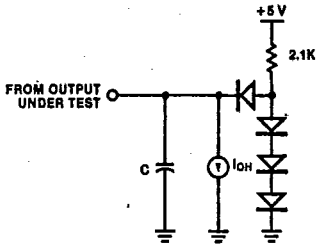
STANDARD TEST CONDITIONS

The DC characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

Available operating temperature ranges are:

■ S = 0°C to +70°C, +4.75V ≤ V_{CC} ≤ +5.25V

All ac parameters assume a total load capacitance (C), including parasitic capacitances, of 100 pf max.



DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{CH}	Clock Input High Voltage	3.0		V_{CC} + 0.3	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	−0.3		0.6	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	
V_{IL}	Input Low Voltage	−0.3		0.8	V	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −500 μA
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = +4.0 mA
I_{IL}	Input Leakage			±10	μA	0.4 ≤ V_{IN} ≤ +2.4V
I_{CC}	V_{CC} Supply Current			700	mA	8 MHz Clock Frequency
	VCC Supply Current			800	mA	10 MHz Clock Frequency

AC CHARACTERISTICS*

Number	Symbol	Parameter	8 MHz Min	8 MHz Max	10 MHz Min	10 MHz Max
1	TcC	PClock Cycle Time	125	500	100	500
2	TwCh	Width (High)	52		40	
3	TwCl	Width (Low)	52		40	
4	TfC	PClock Fall Time		10		10
5	TrC	PClock Rise Time		10		10
6	TdC(Bz)	PClock ↑ to Bus Float		47		47
7	TsA(C)	Address Valid to PClock ↑ Setup Time	0		0	
8	TdC(Az)	PClock ↑ to Address Float		40		40
9	TdA(DR)	Address Valid to Read Data Required Valid (single memory read timing with one wait, without wait is 280)	605†		480†	
10	TsDR(C)	Read Data to PClock ↑ Setup Time	20			
11	TdDS(A)	$\overline{DS}$ ↑ to Address Active	95†		70†	
12	TdC(DW)	PClock ↑ to Write Data Valid		65		65
13	ThDR(C)	Read Data Valid to PClock ↑ Hold Time	5		5	
14	ThDR(DS)	Read Data Valid to $\overline{DS}$ ↑ Hold Time	0		0	
15	TdDW(DS)	Write Data Valid to $\overline{DS}$ ↑ Delay	330†		255†	
16	TdDW(DSW)	Write Data Valid to $\overline{DS}$ ↓ (Write) Delay	80†		55†	
17	TdC(ASf)	PClock ↑ to $\overline{AS}$ ↓ Delay		50		50
18	TsS(C)	Status Valid to PClock ↑ Setup Time	0		0	
19	TdC(ASr)	PClock ↑ to $\overline{AS}$ ↑ Delay		50		50
20	TdAS(DR)	$\overline{AS}$ ↑ to Read Data Required Valid (single memory read timing with one wait; without wait is 120)	420†		320†	
21	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	335†		260†	
22	TwAS	$\overline{AS}$ Width (Low)	110†		85†	
23	TdAS(A)	$\overline{AS}$ ↑ to Address Not Active Delay	95†		70†	
24	TdAz(DSR)	Address Float to $\overline{DS}$ ↓ (Read) Delay	0		0	
25	TdBz(BUS)	Bus Float to $\overline{BUSACK}$ ↓ Delay	9		9	
26	TdAS(DSR)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ (Read) Delay	95†		70†	
27	TdDSR(DR)	$\overline{DS}$ (Read) ↓ to Read Data Required Valid (single memory read timing with one wait, without wait is 20)	295†		220†	
28	TdC(DS)	PClock ↑ to $\overline{DS}$ ↑ Delay		50		50
29	TdDS(DW)	$\overline{DS}$ ↑ to Write Data Not Valid	95†		70†	
31	TdC(DSR)	PClock ↑ to $\overline{DS}$ (Read) ↓ Delay		50		50
32	TwDSR	$\overline{DS}$ (Read) Width (Low) (single memory read timing with one wait, without wait is 85)	360†		285†	
33	TdC(DSW)	PClock ↑ to $\overline{DS}$ (Write) ↓ Delay		50		50
34	TwDSW	$\overline{DS}$ (Write) Width (Low)	235†		185†	
35	TdDSI(DR)	$\overline{DS}$ (I/O) ↓ to Read Data Required Valid	95†		120†	
36	TdC(DSI)	PClock ↑ to $\overline{DS}$ (I/O) ↓ Delay		50		50

*Units in nanoseconds. See Footnotes to AC Characteristics.
†Clock-cycle time-dependent characteristics.

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AC CHARACTERISTICS* (Continued)

Number	Symbol	Parameter	8 MHz Min	8 MHz Max	10 MHz Min	10 MHz Max
37	TwDSI	$\overline{DS}$ (I/O) Width (Low)	235†		185†	
38	TdAS(DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ (Acknowledge) Delay	95†		70†	
39	TdC(DSA)	PClock ↑ to $\overline{DS}$ (Acknowledge) ↓ Delay		50		50
40	TdDSA(DR)	$\overline{DS}$ (Acknowledge) ↓ to Read Data Required Valid	170†		120†	
41	TdC(S)	PClock ↑ to Status Valid Delay		60		60
42	TdS(AS)	Status Valid to $\overline{AS}$ ↑ Delay	85†		60†	
43	TsR(C)	$\overline{RESET}$ to PClock ↓ Setup Time	20		20	
44	ThR(C)	$\overline{RESET}$ to PClock ↓ Hold Time	25		25	
45	TwNMIl	$\overline{NMI}$ Width (Low)	365†		290†	
46	TwNMIh	$\overline{NMI}$ Width (High)	240†		190†	
47	TsNMI(C)	$\overline{NMI}$ ↓ to PClock ↑ Setup Time	40		40	
48	TsVI(C)	$\overline{VI}$, $\overline{NVI}$ to PClock ↑ Setup Time	40		40	
49	ThVI(C)	$\overline{VI}$, $\overline{NVI}$ to PClock ↑ Hold Time	20		20	
50	TwVI	$\overline{VI}$, $\overline{NVI}$ Width (Low)	365†		290†	
51	TsBREQ(C)	$\overline{BUSREQ}$ Change to PClock ↑ Setup Time	40		40	
52	TwBREQ	$\overline{BUSREQ}$ Width (Low)	365†		290†	
53	ThBREQ(C)	$\overline{BUSREQ}$ to PClock ↑ Hold Time	20		20	
54	TdC(BACKr)	PClock ↑ to $\overline{BUSACK}$ ↑ Delay		65		65
55	TdC(BACKf)	PClock ↑ to $\overline{BUSACK}$ ↓ Delay		65		65
57	TdC(IEr)	PClock ↑ to $\overline{IE}$ ↑ Delay		65		65
58	TdC(IEf)	PClock ↑ to $\overline{IE}$ ↓ Delay		65		65
59	TsBRSTA(C)	$\overline{BRSTA}$ to PClock ↑ Setup Time	25		25	
60	TsEPUBSY(C)	$\overline{EPUBSY}$ to PClock ↑ Setup Time	20		20	
61	ThBRSTA(C)	$\overline{BRSTA}$ to PClock ↑ Hold Time	5		5	
62	ThEPUBSY(C)	$\overline{EPUBSY}$ to PClock ↑ Hold Time	5		5	
63	TsRSP(C)	RSP Change to PClock ↑ Setup Time	20		20	
64	ThRSP(C)	RSP to PClock ↑ Hold Time	5		5	
65	TdIE(OE)	$\overline{OE}$ Change to $\overline{IE}$ Change Delay	295†		270†	
66	TwGACK	$\overline{GACK}$ Width (Low)	365†		290†	
67	TsGACK(C)	$\overline{GACK}$ Change to PClock ↑ Setup time	40		40	
68	ThGACK(C)	$\overline{GACK}$ to PClock ↑ Hold Time	20		20	
69	TdC(OEf)	PClock ↑ to $\overline{OE}$ ↓ Delay		50		50
70	TdC(OEr)	PClock ↑ to $\overline{OE}$ ↑ Delay		50		50
71	TdC(BRSTf)	PClock ↑ to $\overline{BRST}$ ↓ Delay		65		65
72	TdC(BRSTr)	PClock ↑ to $\overline{BRST}$ ↑ Delay		65		65
73	TdC(GREQf)	PClock ↑ to $\overline{GREQ}$ ↓ Delay		50		50
74	TdC(GREQr)	PClock ↑ to $\overline{GREQ}$ ↑ Delay		50		50

*Units in nanoseconds. See Footnotes to AC Characteristics.
†Clock-cycle time-dependent characteristics.

FOOTNOTES TO AC CHARACTERISTICS

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No.	Symbol	Equation
9	TdA(DR)	5TcC – TsDR(C)
11	TdDS(A)	TcC – TdC(DS) + TdC(Az) – 20ns
15	TdDW(DS)	3TcC – TdC(DW) + TdC(DS) – 30ns
16	TdDW(DSW)	TcC – TdC(DW) + TdC(DSW) – 30ns
20	TdAS(DR)	4TcC – TdC(ASr) – TsDR(C) – TrC
21	TdDS(AS)	3TcC – TdC(DS) + TdC(ASf) – 40ns
22	TwAS	TcC – 15ns
23	TdAS(A)	TcC – TdC(ASr) + TdC(Az) – 20ns
26	TdAS(DSR)	TcC – TdC(ASr) + TdC(DSR) – 30ns
27	TdDSR(DR)	3TcC – TdC(DSR) – TsDR(C) – TrC
29	TdDS(DW)	TcC – TdC(DS) + TdC(Az) – 20ns
32	TwDSR	3TcC – 15ns
34	TwDSW	2TcC – 15ns
35	TdDSI(DR)	2TcC – TdC(DSI) – TsDR(C) – TrC
37	TwDSI	2TcC – 15ns
38	TdAS(DSA)	TcC – TdC(ASr) + TdC(DSA) – 30ns
40	TdDSA(DR)	2TcC – TdC(DSA) – TsDR(C) – TrC
42	TdS(AS)	TcC – TdC(S) + TdC(ASr) – 30ns
45	TwNMIl	3TcC – 10ns
46	TwNMIh	2TcC – 10ns
50	TwVI	3TcC – 10ns
52	TwBREQ	3TcC – 10ns
65	TdIE(OE)	TcC – TdC(OEr) + TdC(IEf) – 45ns
66	TwGACK	3TcC – 10ns

AC Timing Test Conditions

V_{OL} = 0.8V
V_{OH} = 2.0V
V_{IL} = 0.8V
V_{IH} = 2.4V
V_{ILC} = 0.6V
V_{IHC} = 3.0V

AC TIMING

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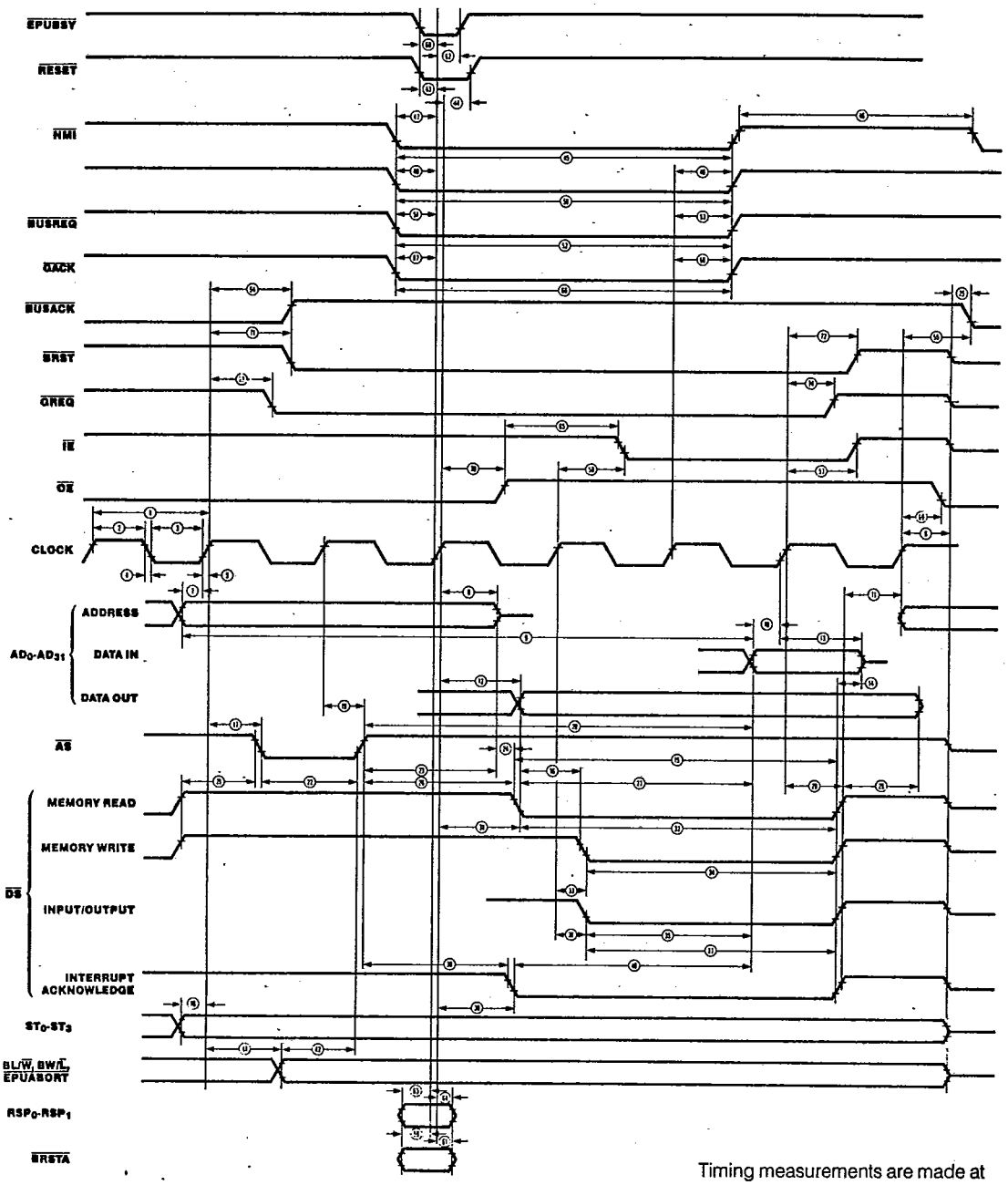

Timing measurements are made at the following voltages.

	High	Low
Clock	3.0V	0.6V
Output	2.0V	0.8V
Input	2.0V	0.8V
Float	ΔV	±0.5V

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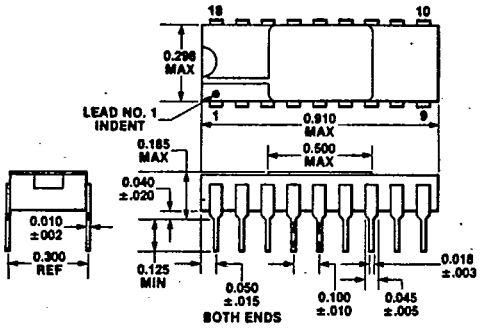
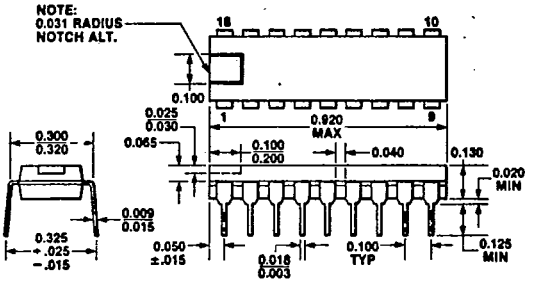
PACKAGE INFORMATION

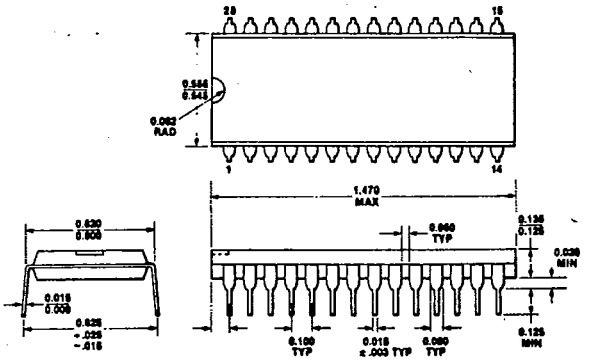


18-Pin Ceramic Package



18-Pin Plastic Package

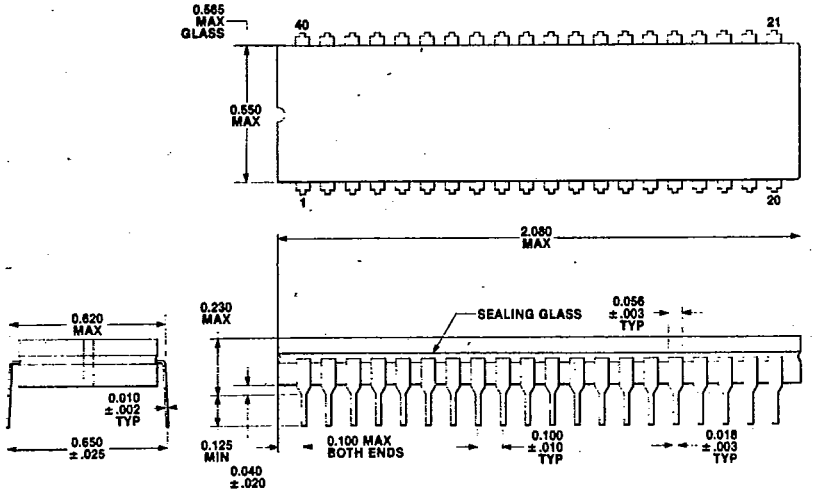
NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4



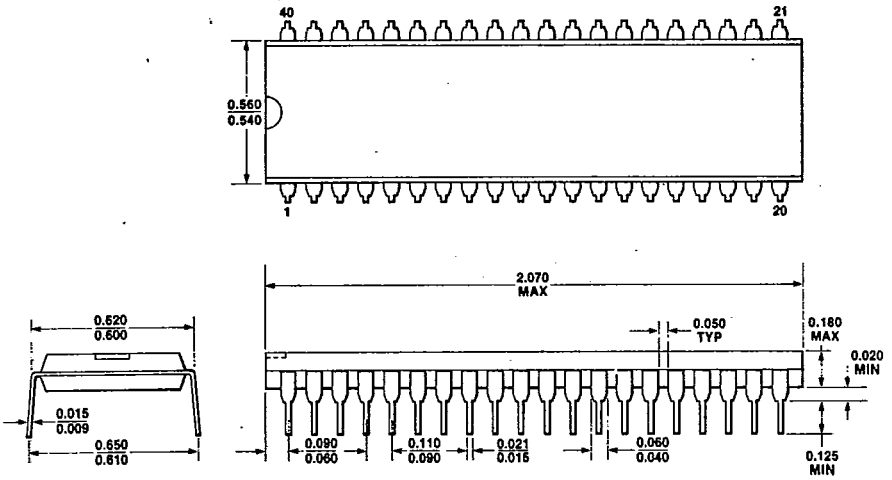
28-Pin Plastic Package

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

PACKAGE INFORMATION (Continued)



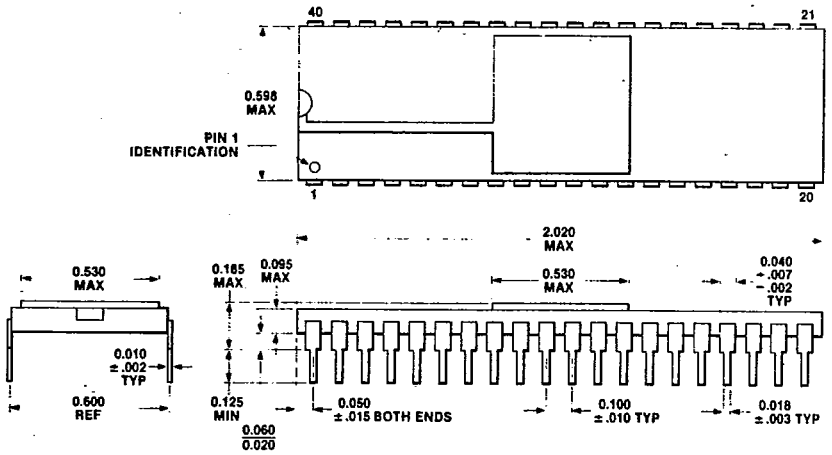
40-Pin Dual-In-Line Package (DIP), Cerdip



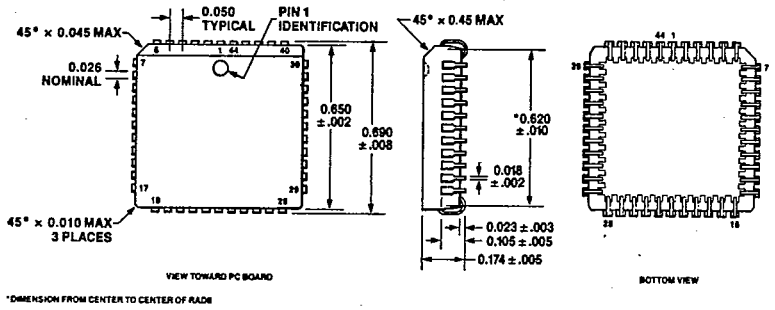
40-Pin Dual-In-Line Package (DIP), Plastic

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

PACKAGE INFORMATION (Continued)

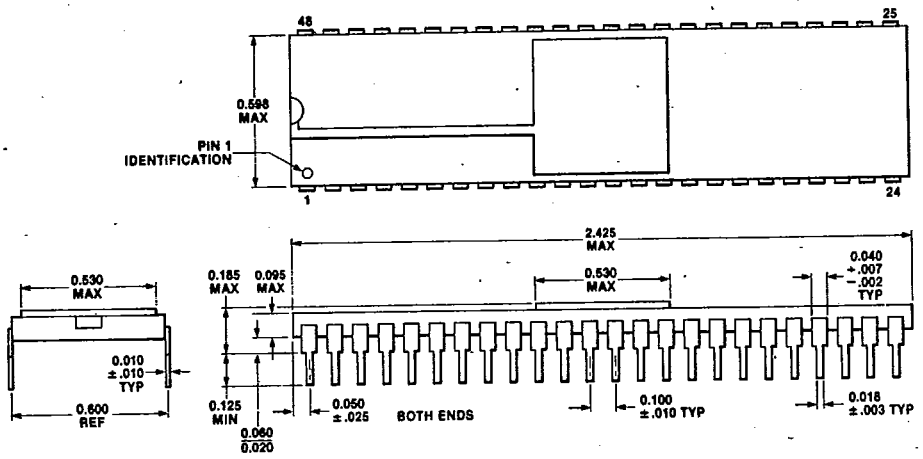


40-Pin Dual-In-Line Package (DIP), Ceramic

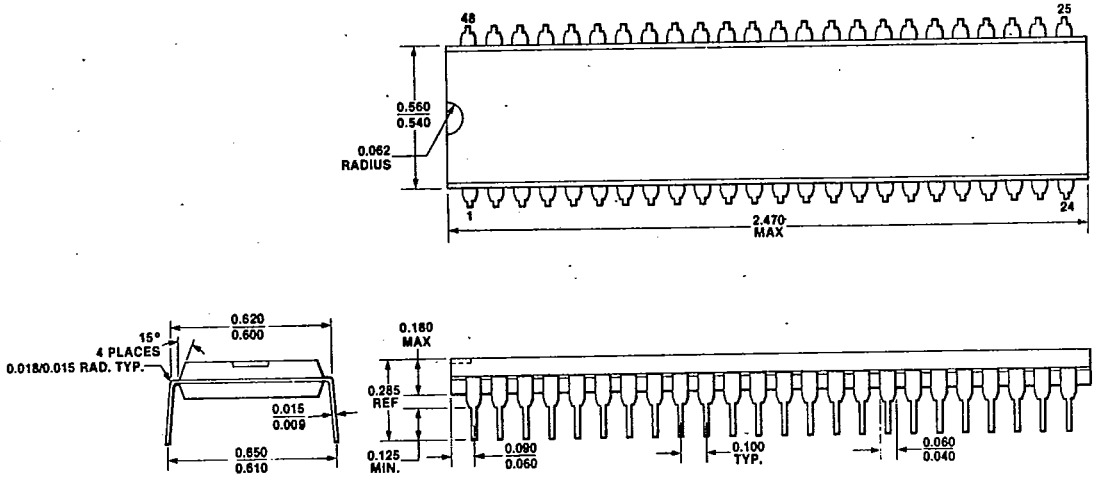


44-Pin Plastic Chip Carrier (PCC)

PACKAGE INFORMATION (Continued)



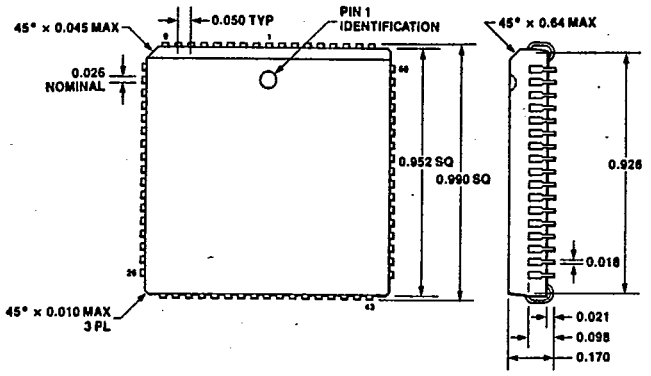
48-Pin Dual-in-Line Package (DIP), Ceramic



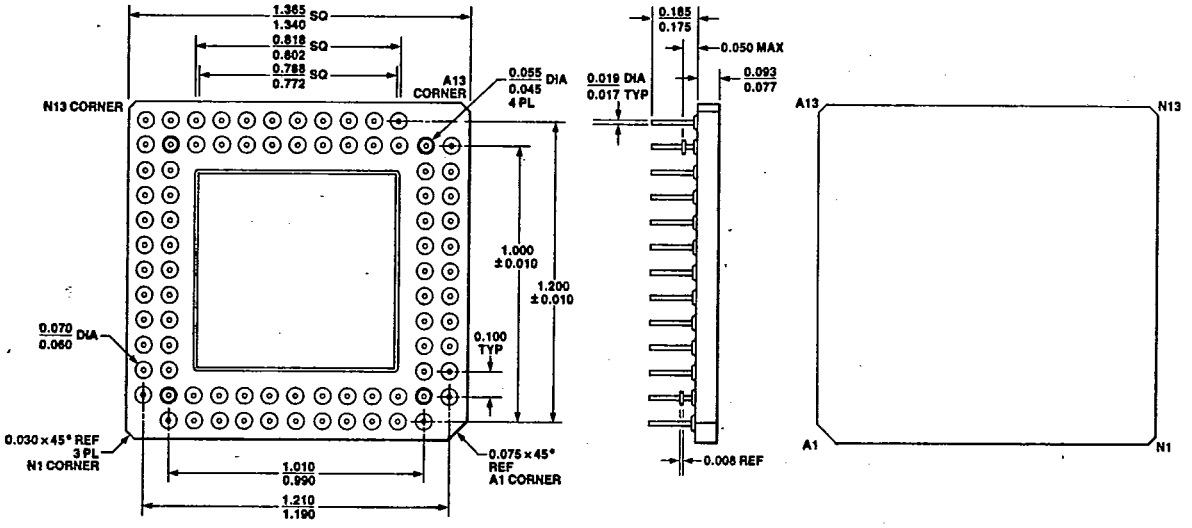
48-Pin Dual-in-Line Package (DIP), Plastic

T-90-20

PACKAGE INFORMATION (Continued)



68-Pin Plastic Chip Carrier (PCC)



84-Pin Grid Array (PGA), Bottom View

View toward PC Board

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.