1. FEATURES

- Monolithic Quad Fast Ethernet Physical Layer Device for Local Area Networks (LANs).
- Combines 10Base-T, 100Base-TX and 100Base-FX in a Quad PHY device to simplify the design and manufacturing of Fast Ethernet products.
- Implements four independent IEEE 802.3u compliant MII interfaces (one per PHY) or four symbol interfaces (one per PHY) or a muxed symbol or MII interface (one for all four PHYs).
- Supports 10Base-T, 100Base-TX and 100Base-FX operation in Half and Full Duplex modes.
- Provides Auto-Negotiation to allow interrogation of a link partner to determine common abilities.
- For 100Base-TX, provides on-chip Clock Recovery, Clock Synthesis, MLT-3 Wave Shaping, Stream Cipher Scrambling, Adaptive Equalization and Baseline Wander Correction.
- For 100Base-FX, provides on-chip Clock Recovery, Clock Synthesis, Signal detect inputs and interfaces directly to multimode or single mode optical modules.
- For 10Base-T, provides on-chip Clock Recovery, Clock Synthesis, Manchester Encoding, Tx and Rx Filters & Drivers.
- Provides interface to set aggregate PHY control functions for; Speed Selection, Duplex Mode, Isolate, Symbol Interface, Repeater support, Auto-negotiation enable and Fiber (100Base-FX) support.
- Provides user programmable serial status outputs on a per PHY basis to indicate; 10/100 speed, Link Status, Collision, Duplex Mode, Tx Activity and Rx Activity
- Provides a MII serial management interface to set control register options and view status registers.
- Low power, +5 Volt CMOS technology.
- 208 pin plastic quad flat pack (PQFP) package.

2. APPLICATIONS

- 10Base-T and 100 Base-TX/FX Switches
- 10Base-T and 100 Base-TX/FX Repeaters
- 10Base-T and 100 Base-TX/FX Bridges
- 100 Base-TX/FX Server NIC cards
- Routers

3. REFERENCES

- ISO/IEC 8802-3:1993 - "Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications"
- IEEE 802.3u-1995 - " Media Access Control (MAC) Parameters, Physical Layer, Medium Attachment Units, and Repeaters for 100 MB/s Operation, Type 100BASE-T"
- ANSI X3.263-1995 - "Fiber Distributed Data Interface (FDDI) - Token Ring Twisted Pair Physical Layer Medium Dependent (TP-PMD)"
- ISO/IEC 9314-3 - "Information processing systems - Fiber distributed Data Interface (FDDI) - Part 3: Physical Layer Medium Dependent (PMD)"

4. APPLICATION EXAMPLES

The ELAN-EPHY is typically used in applications requiring a 100Base-Tx/Fx and/or a 10Base-T interface. The ELAN-EPHY can be utilized in switches, repeater hubs, bridges, routers or Network Interface Cards (NICs) for servers.

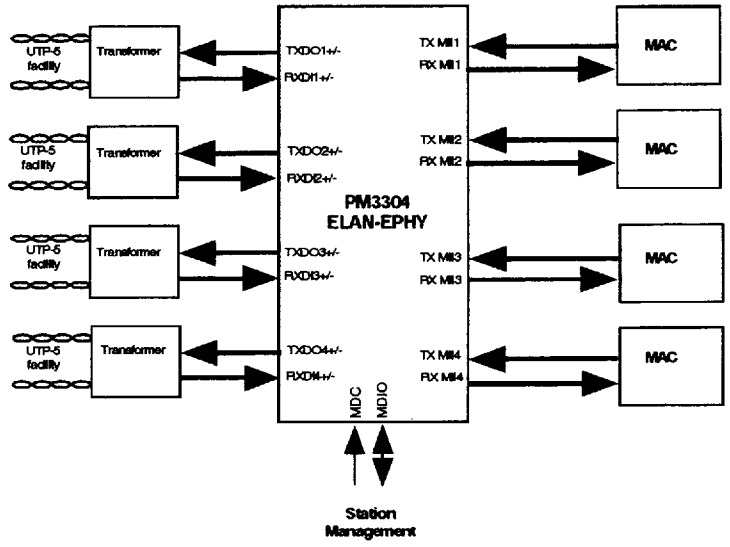
Due to the level of integration utilized in the ELAN-EPHY external components are not required other than line coupling magnetics, a bias setting resistor (per channel) and supply decoupling. The external components that are required are standard components that are readily available in the marketplace.

On the Media Dependent Interface (MDI) side the ELAN-EPHY is interfaced to UTP-5 twisted pair wiring via a transformer. Alternatively, the ELAN-EPHY can be directly connected to an optical datalink. On the Media Independent Interface (MII) side the ELAN-EPHY connects directly to Media Access Controllers (MAC) or Repeater Interface Controllers (RIC). The ELAN-EPHY can be configured at power up via user configurable input pins. Alternatively the ELAN-EPHY can be configured and controlled via the MII Serial Management Interface (SMI).

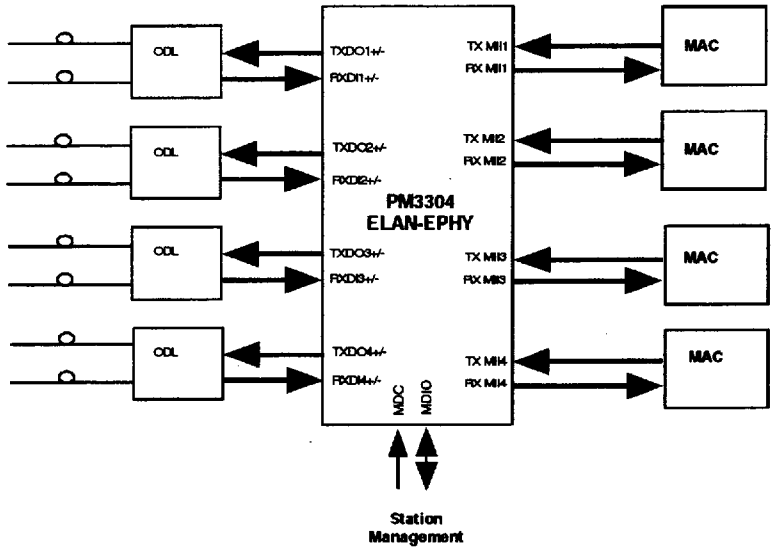
The typical applications that the ELAN-EPHY can be used in are shown below. The ELAN-EPHY can interface each of the four channels directly to a separate MAC layer device by the MII ports. When used in a repeater application the ELAN-EPHY has two modes of operation. For higher functionality repeater hubs (such as segmented hubs) where individual access to each channels symbol (SYMBL) interface is required, the ELAN-EPHY provides full access to each channels transmit and receive ports. For repeater hubs where the cost must be kept as low as possible, the ELAN-EPHY multiplexes all four channel symbol interfaces onto one port. This enables the design of multi-port repeater hubs with minimum external logic.

Fig. 4.1 Typical Applications

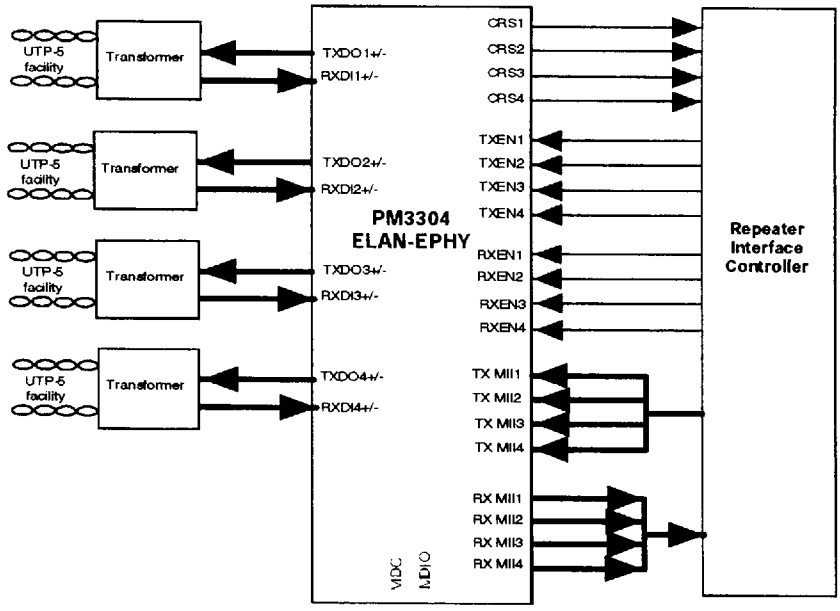
Interfacing to MAC Devices (UTP-5 Interface)



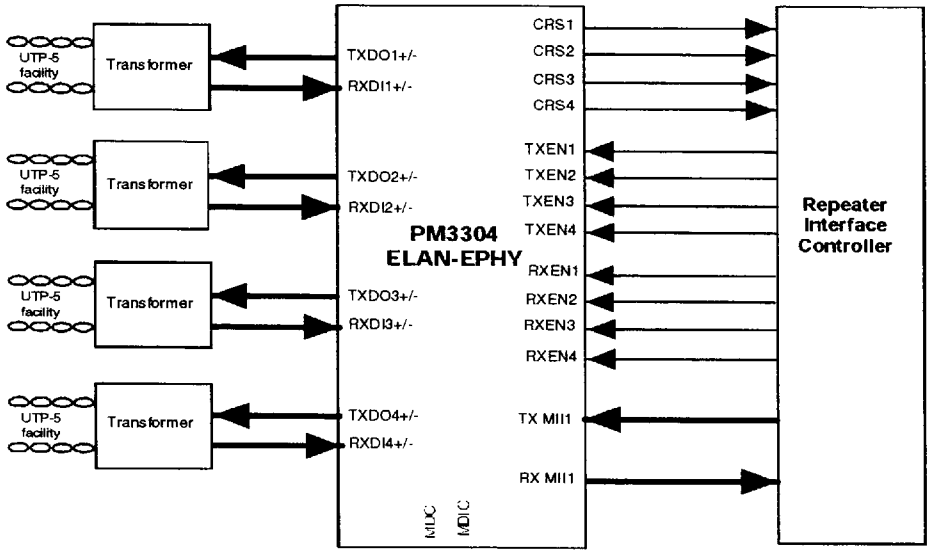
Interfacing to MAC Devices (Fiber Interface)



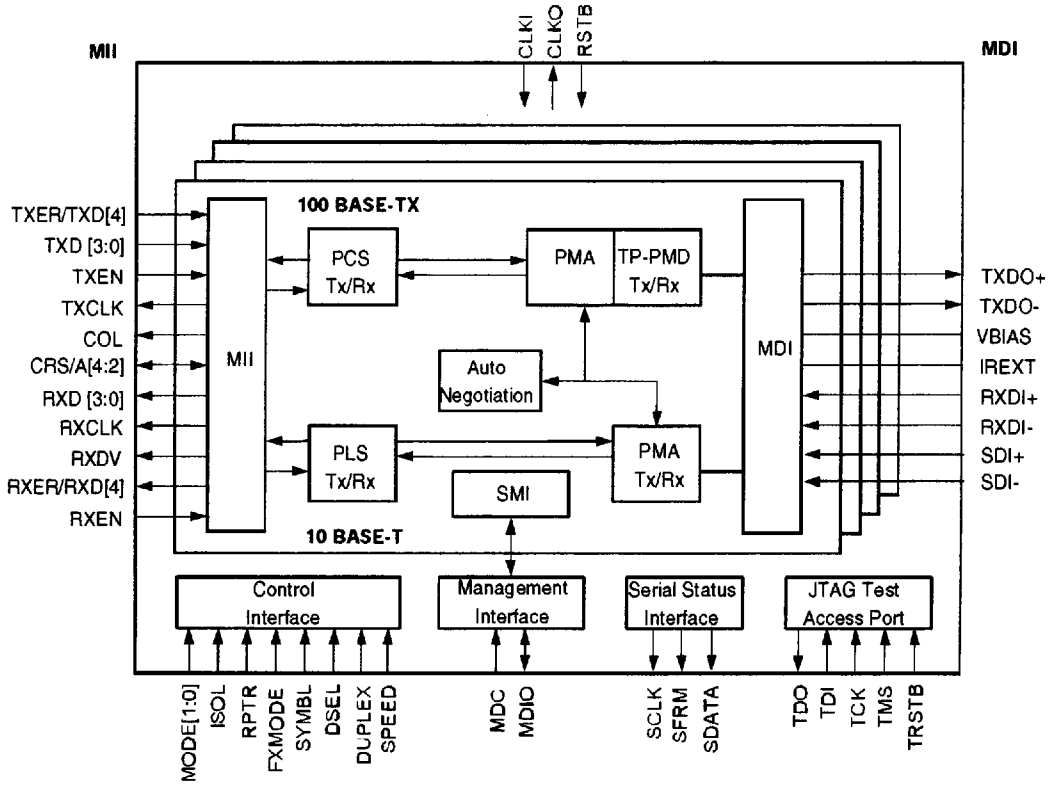
Interfacing to RIC Devices (Symbol Interfaces, UTP-5)



Interfacing to RIC Devices (Multiplexed Symbol or MII Interface, UTP-5)



5. BLOCK DIAGRAM



6. DESCRIPTION

The PM3304 ELAN-EPHY Ethernet Physical Layer interface is a monolithic integrated circuit that implements 10 BASE-T Physical Medium Attachment (PMA) and Physical Layer Signaling (PLS) functions, 100 BASE-TX and 100 BASE-FX Physical Medium Dependent (PMD) functions and 100 BASE-X Physical Medium Attachment (PMA) and Physical Coding Sublayer (PCS) functions.

For 10Base-T PMA layer functions the ELAN-EPHY performs input filtering and squelching on the receive data and output wave shaping on the transmit data. The Jabber detect, Signal Quality Error (SQE) test, collision detection, auto-polarity correction, loopback and Normal Link Pulse generation and detection functions are also provided by the 10Base-T PMA. The PLS layer provides for receive clock recovery and manchester decoding and transmit clock synthesis and manchester encoding. In addition the PLS layer generates the COL and CRS signals and maps the bit wide data to nibbles for transfer across the MII.

For 100Base-TX receive PMD functions the ELAN-EPHY performs adaptive equalization, baseline wander correction, MLT-3 slicing, clock recovery and descrambling. The transmit PMD functions include clock synthesis, scrambling and MLT-3 wave shaping. The PMA layer passes the data to the PCS and also generates the link integrity indications for the Auto-negotiation logic. The PCS layer perform 4B/5B encoding and decoding on the data, framing the data and CRS and COL signal generation.

For 100Base-FX transmit operation the ELAN-EPHY by-passes scrambling and MLT-3 wave shaping and outputs NRZI encoded data. For receive operation the ELAN-EPHY accepts NRZI encoded data on its receive inputs and by-passes adaptive equalization, baseline wander correction and MLT-3 slicing. The 100Base-FX PMA and PCS layer functionality is the same as 100Base-TX.

The ELAN-EPHY supports per channel Auto-negotiation to allow for generation and detection of enhanced modes of operation. The ELAN-EPHY can operate with 10Base-T and 100Base-TX/FX PHYs in half or full duplex mode whether they support Auto-Negotiation or not.

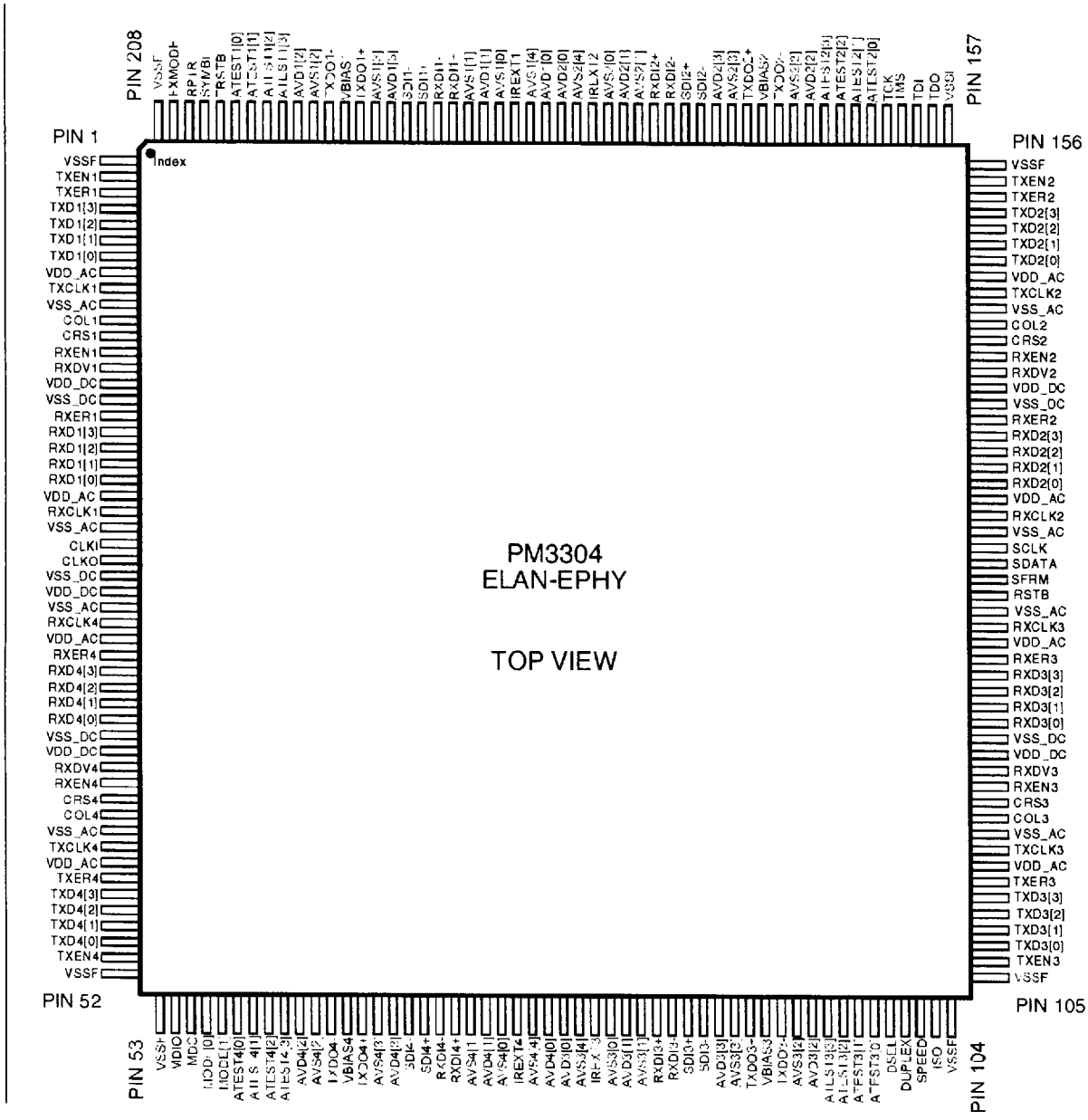
In addition to the above functionality the ELAN-EPHY can be programmed to operate in repeater applications by using the repeater option. For Type 2 repeaters in FAST ETHERNET applications the ELAN-EPHY can reduce latency when configured for symbol data transfer. For low cost hubs all ports can be multiplexed onto a single MII by using the shared port configuration. These features are only available when the ELAN-EPHY is programmed for 100Base-X operation.

The ELAN-EPHY can be configured via external pins at reset or via the Serial Management Interface (SMI). The SMI allows for the ongoing control and monitoring of the ELAN-EPHY. In addition to the SMI the ELAN-EPHY also provides per-PHY status indication on the Serial Status Interface (SSI). The SSI is user programmable to allow for various combinations of status indications.

The ELAN-EPHY provides multiple loopback modes in both 10BASE-T and 100BASE-X modes. A natural auto-loopback and diagnostic loopback is provided in 10BASE-T mode. An at speed diagnostic loopback and low speed diagnostic loopback are provided in 100BASE-X mode. The low speed diagnostic loopback uses the same data path as the at speed diagnostic loopback with the TCK clock pin clocking the line interface logic. For more details on the loopback modes, please refer to the Operations section of this document.

7. PIN DIAGRAM

The ELAN-EPHY is packaged in a 208 pin PQFP package having a body size of 28 mm by 28 mm and a pin pitch of 0.5 mm.



8. PIN DESCRIPTION (TOTAL 208)

8.1. MII Signals (70)

Pin Name	Type	Pin No.	Feature
TXCLK1 TXCLK2 TXCLK3 TXCLK4	Tristate	9 148 113 44	Transmit Clock (TXCLK) signal provides the timing reference for the transmit section of the MII. For 10Base-T operation the TXCLK frequency shall be 2.5 MHz. For 100Base-TX operation the TXCLK frequency shall be 25 MHz. The TXEN, TXER and TXD[3:0] signals are sampled on the rising edge of TXCLK. The TXCLK signal is tri-stated when the PHY is isolated (via the ISOL input or the ISOLATE bit in the Control register) or during reset.
TXEN1 TXEN2 TXEN3 TXEN4	Input	2 155 106 51	The Transmit Enable (TXEN) signal indicates when valid transmit data is present on the MII. When TXEN is sampled high valid data is present on the TXER and TXD[3:0] signals. When TXEN is sampled low the TXER and TXD[3:0] signals are not valid. The TXEN signal is expected to be asserted with the first valid nibble of the preamble and stay asserted through the frame. TXEN should be negated on the first TXCLK following the last nibble of the frame. When configured for a symbol interface (via the SYMBL input or the SYMBL bit in the Extended PHY Control One register) the TXEN is expected to be asserted with the first valid code group of a frame and remain asserted through to the end of the frame. When the PHY is isolated, TXEN is ignored. TXEN is sampled on the rising edge of TXCLK.

TXER1/TXD1[4] TXER2/TXD2[4] TXER3/TXD3[4] TXER4/TXD4[4]	Input	3 154 111 46	When the PHY is configured for a MII interface (via the SYMBL input or the SYMBL bit in the Extended PHY Control One register), the Transmit Coding Error (TXER) signal indicates when the PHY should transmit an invalid symbol in the current frame. When TXER is sampled high the PHY shall transmit an invalid symbol in the current frame. When TXER is sampled low no action is taken. TXER is only valid when TXEN is also sampled high. In addition the TXER signal is ignored for 10Base-T operation. TXER is sampled on the rising edge of TXCLK. When the PHY is configured for a symbol interface, the TXD[4] signal carries the most significant bit of the five bit symbol to the PHY. TXD[4] is only valid when TXEN is sampled high. When the PHY is isolated, TXER/TXD[4] is ignored. TXD[4] is sampled on the rising edge of TXCLK.
TXD1[0] TXD1[1] TXD1[2] TXD1[3] TXD2[0] TXD2[1] TXD2[2] TXD2[3] TXD3[0] TXD3[1] TXD3[2] TXD3[3] TXD4[0] TXD4[1] TXD4[2] TXD4[3]	Input	7 6 5 4 150 151 152 153 107 108 109 110 50 49 48 47	The Transmit Data (TXD[3:0]) bus carries the data nibbles that are to be transmitted by the PHY. TXD[3:0] are only valid when TXEN is sampled high. When the PHY is configured for a symbol interface, TXD[3:0] are only valid when TXEN is sampled high. When the PHY is isolated, TXD[3:0] are ignored. TXD[3:0] are sampled on the rising edge of TXCLK.

RXCLK1 RXCLK2 RXCLK3 RXCLK4	Tristate	23 134 127 30	Receive Clock (RXCLK) signal provides the timing reference for the receive section of the MII. If there is a loss of signal from the medium and RXCLK cannot be recovered, RXCLK transitions to a reference clock, derived from CLKI, in a smooth manner. For 10Base-T operation the RXCLK frequency shall be 2.5 MHz. For 100Base-X operation the RXCLK frequency shall be 25 MHz. The RXDV, RXER and RXD[3:0] signals are updated on the rising edge of RXCLK. The RXCLK signal is tri-stated when the PHY is isolated, RXEN is low or during reset.
RXDV1 RXDV2 RXDV3 RXDV4	Tristate	14 143 118 39	When the PHY is configured for a MII interface, the Receive Data Valid (RXDV) signal indicates when valid receive data is present on the MII. When RXDV is set high valid data is present on the RXER and RXD[3:0] signals. When RXDV is set low the RXER and RXD[3:0] signals are not valid. The RXDV signal is set high sometime after receipt of the Start of Stream Delimiter (SSD), but no later than when the Start of Frame Delimiter (SFD) is provided on RXD[3:0], and stays asserted through the frame. RXDV is set low on the first RXCLK following the last nibble of the frame. When the PHY is configured for a symbol interface, the PHY indicates that it has framed to the incoming data stream through the assertion of RXDV. The RXDV is set high sometime after receipt of the SSD, but no later than when the SFD is provided on RXD[4:0], and stays asserted through the frame. RXDV is set low on the first RXCLK following the last code group of the frame. RXDV is updated on the rising edge of RXCLK. The RXDV signal is tri-stated when the PHY is isolated, RXEN is low or during reset.

RXEN1 RXEN2 RXEN3 RXEN4	Input	13 144 117 40	Receive Output Enable (RXEN) signal controls the tri-stating of the RXCLK, RXDV, RXER and RXD[3:0] signals. When RXEN is high the receive MII port is driven by the PHY. When RXEN is low the receive port is tri-stated. The RXEN can enable the receive MII port asynchronously or synchronously. The method of enabling is set via the RXEN_SYNC bit in the Extended PHY Control One register.
RXER1/RXD1[4] RXER2/RXD2[4] RXER3/RXD3[4] RXER4/RXD4[4]	Tristate	17 140 125 32	When the PHY is configured for a MII interface, the Receive Error (RXER) signal indicates that an error was detected in the current frame by the PHY. When RXER is set high an error was detected in the current receive frame being transferred on the MII. When RXER is set low an error was not detected. RXER is only valid when RXDV is also set high. The RXER signal is tri-stated when the PHY is isolated or when RXEN is low. RXER is updated on the rising edge of RXCLK. When the PHY is configured for a symbol interface, the RXD[4] signal carries the most significant bit of the five bit symbol from the PHY. Since the PHY continuously sources data, RXD[4] will be updated on every RXCLK cycle. When RXDV is asserted, the PHY has framed to the incoming data stream and RXD[4] is aligned to code group boundaries. RXD[4] is updated on the rising edge of RXCLK. The RXD[4] signal are tri-stated when the PHY is isolated, RXEN is low or during reset.

RXD1[0] RXD1[1] RXD1[2] RXD1[3] RXD2[0] RXD2[1] RXD2[2] RXD2[3] RXD3[0] RXD3[1] RXD3[2] RXD3[3] RXD4[0] RXD4[1] RXD4[2] RXD4[3]	Tristate	21 20 19 18 136 137 138 139 121 122 123 124 36 35 34 33	The Receive Data (RXD[3:0]) bus carries the data nibbles that are received by the PHY. When the PHY is configured for a MII interface, RXD[3:0] is only valid when RXDV is also set high. When the PHY is configured for a symbol interface, the PHY continuously sources data and thus RXD[3:0] will be updated on every RXCLK cycle. When RXDV is asserted, the PHY has framed to the incoming data stream and RXD[3:0] is aligned to code group boundaries. RXD[3:0] are updated on the rising edge of RXCLK. The RXD[3:0] signals are tri-stated when the PHY is isolated, RXEN is low or during reset.
COL1 COL2 COL3 COL4	Tristate	11 146 115 42	Collision Detect (COL) signal indicates that a collision was detected on the media. When the PHY is configured for half duplex operation, COL is set high when a collision is detected by the PHY on the media. When COL is set low a collision has not been detected. When the PHY is configured for full duplex operation or repeater operation (via the RPTR bit in the Extended PHY Control One register), COL is not used and is set low. The COL signal is tri-stated when the PHY is isolated or during reset.

CRS1/A[2] CRS2/A[3] CRS3/A[4] CRS4/ANEGAB	I/O	12 145 116 41	When RSTB is low the PHY Address (A[4:2]) specify the most significant three bits of the ELAN-EPHY base address. A[4:2] are sampled at reset to determine the ELAN-EPHY base address. The ELAN-EPHY will occupy four contiguous addresses starting from the base address. The A[4:2] inputs are sampled using the rising edge of RSTB. The Auto-negotiation Ability (ANEGAB) input configures the ELAN-EPHY auto-negotiation capabilities (by setting the ANEG_AB bit in the Status register). When sampled low ANEGAB indicates that the ELAN-EPHY should not auto-negotiate its capabilities with its link partner. The ELAN-EPHY mode of operation will be set via the management interface. When sampled high ANEGAB allows the ELAN-EPHY to determine its mode of operation via auto-negotiation. The ANEGAB input is sampled using the rising edge of RSTB. When RSTB is high the Carrier Sense (CRS) signal is configured as an output. CRS indicates when either the receive or transmit medium is non idle. When the PHY is configured to operate with RICs, the CRS is set high when the receive medium is non idle. When CRS is set low the receive media is idle. When the PHY is configured to operate with MACs in half-duplex mode, the CRS is set high when the transmit or receive mediums are non idle. When CRS is set low both the transmit and receive media are idle. When the PHY is configured to operate with MACs in full-duplex mode, the CRS is set high when the receive medium is non idle. When CRS is set low the receive media is idle. The CRS signal is tri-stated when the PHY is isolated or during reset.

MDC	Input	55	The Management Data Clock (MDC) signal provides the clock source for the MII serial management interface. Data is clocked into and out of the ELAN-EPHY via the MDC. The MDC is an aperiodic signal with a maximum frequency of 25 MHz.
MDIO	I/O	54	The Management Data Input/Output (MDIO) signal carries data to and from the ELAN-EPHY. As an input MDIO is sampled on the rising edge of MDC. As an output MDIO is updated on the rising edge of MDC.

8.2. MDI Signals (32)

Pin Name	Type	Pin No.	Feature
RXDI1+ RXDI1-	Analog	189 190	The Receive differential data inputs (RXDI+ / RXDI-) contain the 100Base-TX, 100Base-FX or 10Base-T receive data streams.
RXDI2+ RXDI2-		176 175	For the TP-PMD the receive data stream encoding is MLT-3 for 100Base-Tx and Manchester for 10Base-T.
RXDI3+ RXDI3-		85 86	For the fiber PMD the receive data stream encoding is NRZI.
RXDI4+ RXDI4-		72 71	
SDI1+ SDI1-	Analog	191 192	The Signal Detect differential inputs (SDI+/SDI-) indicate if the data from the optical module is valid.
SDI2+ SDI2-		174 173	When sampled high, SDI indicates that the data from the optical module is valid. When sampled low, SDI indicates that there is a loss of signal condition at the optical module and the data is invalid.
SDI3+ SDI3-		87 88	
SDI4+ SDI4-		70 69	The SDI inputs are only used for the fiber PMD. For the TP-PMD the SDI inputs should be connected to analog ground.
VBIAS1 VBIAS2 VBIAS3 VBIAS4	Analog	196 169 92 65	The Transmit Bias outputs (VBIAS) are used to bias the centertaps of the transmit magnetics. VBIAS is not used for fiber PMD applications and must be tied to ground through a capacitor.
IREXT1 IREXT2 IREXT3 IREXT4	Analog	185 180 81 76	The Current Reference inputs (IREXT) are used to set analog circuit bias levels using an external precision resistor. The external precision resistor has a nominal value in the range 11.5 to 12.6 Kohms.

TXDO1+ TXDO1- TXDO2+ TXDO2- TXDO3+ TXDO3- TXDO4+ TXDO4-	Analog	195 197 170 168 91 93 66 64	The Transmit differential data inputs (TXDO+ / TXDO-) contain the 100Base-TX, 100Base-FX or 10Base-T transmit data streams. For the TP-PMD the transmit data stream encoding is MLT-3 for 100Base-Tx and Manchester for 10Base-T. For the fiber PMD the transmit data stream encoding is NRZI.

8.3. Configuration / Monitor Signals (12)

Pin Name	Type	Pin No.	Feature
SCLK	Tristate	132	The Status Clock (SCLK) signal provides the clock source for the serial status interface. Data is clocked out of the ELAN-EPHY via SCLK. The SCLK is an aperiodic signal with a maximum frequency of 1 MHz. The SCLK signal is tri-stated during reset.
SFRM	Tristate	130	The Status Frame (SFRM) signal provides an indication of when a complete status frame has been shifted out. SFRM is pulsed once for each status frame the ELAN-EPHY shifts out. The SFRM signal is tri-stated during reset. SFRM is updated on the falling edge of SCLK.
SDATA	Tristate	131	The Status Data (SDATA) signal carries status information from the ELAN-EPHY. The format of the data can be set via the Status Control register. The SDATA signal is tri-stated during reset. SDATA is updated on the falling edge of SCLK.

MODE[0] MODE[1]	Input	56 57	The Mode select (MODE[1:0]) signals are used to configure the operation of the ELAN-EPHY. 00 - All ports enabled. 01 - One port enabled. 10 - Reserved. 11 - Production Test. When MODE=00 each PHY has it's own MII port. When MODE=01 all the MIIs are multiplexed onto a single MII (PHY One's MII). MODE=01 is only valid when the ELAN-EPHY is configured for 100Base-X operation. MODE=11 is reserved for production testing. The MODE[1:0] inputs are assumed stable and should not change after reset.
RPTR	Input	206	The Repeater select (RPTR) input configures the ELAN-EPHY to interface with MACs or RICs. When sampled high, RPTR indicates the ELAN-EPHY should be configured to operate with RICs and will only generate CRS for receive medium activity and will not generate the COL indication. When sampled low, RPTR indicates the ELAN-EPHY should be configured to operate with a MACs and will generate CRS for receive and transmit medium activity and will generate the COL indication. When RPTR is sampled low, control of the per-PHY repeater function is selected by the RPTR bit in the Extended PHY Control One register. The RPTR input is assumed stable and should not change after reset.

FXMODE	Input	207	The Fiber Mode select (FXMODE) input configures the ELAN-EPHY to use the fiber based PMD. When sampled high, FXMODE indicates that the fiber PMD should be used. When sampled low, FXMODE indicates that the TP-PMD should be used. FXMODE is only valid for 100Base-X operation. When the fiber PMD is selected the ELAN-EPHY must bypass its scrambling and MLT-3 encoding/decoding. When FXMODE is sampled low, control of the per-PHY 100Base-FX PMD can be selected by the FXMODE bit in the Extended PHY Control One register. The FXMODE input is assumed stable and should not change after reset.
ISOL	Input	103	The Isolate (ISOL) input controls the tri-stating of the ELAN-EPHY from the MII. When sampled high, ISOL indicates that the ELAN-EPHY should isolate all it's PHYs from their respective MIIs. When sampled low, normal operation is allowed. When ISOL is sampled low, control of the per-PHY isolate function is selected by the ISOLATE bit in the Control register. The ISOL input can be used to configure the ELAN-EPHY in real time.

SYMBL	Input	205	The Symbol (SYMBL) input configures the ELAN-EPHY to use the symbol interface format. SYMBL is only valid for 100Base-X operation. When sampled high, SYMBL indicates that the five bit symbol interface format should be used. The TXER signal is used for TXD[4] and RXER is used for RXD[4]. When sampled low, SYMBL indicates that the standard MII interface format should be used. When SYMBL is sampled low, control of the per-PHY symbol interface function is selected by the SYMBL bit in the Extended PHY Control One register. The SYMBL input is assumed stable and should not change after reset.
DSEL	Input	100	The Default Select (DSEL) signal is used to indicate whether the ELAN-EPHY uses the external default values (set by SPEED and DUPLEX) or its internal default values for the PHY abilities in the Status register. When DSEL is sampled low the ELAN-EPHY will use its internal defaults. When DSEL is sampled high the ELAN-EPHY will use SPEED and DUPLEX to set the default abilities (100XF_AB, 100XH_AB, 10F_AB and 10H_AB in the Status register). The DSEL input must be held low when the Extended PHY Control 1 register bits SMODE[2:0] = "001". The DSEL input is assumed stable and should not change after reset.

SPEED	Input	102	The Speed (SPEED) signal indicates what speed of operation the ELAN-EPHY supports. When SPEED is sampled low and DSEL is sampled high the ELAN-EPHY will default to 10Base-T operation (10F_AB or 10H_AB set high depending on DUPLEX). When SPEED is sampled high and DSEL is sampled high the ELAN-EPHY will default to 100Base-X operation (100XF_AB or 100XH_AB set high depending on DUPLEX). SPEED is ignored when DSEL is sampled low (all four abilities will be enabled). When the Extended PHY Control 1 register bits SMODE[2:0] = "001", the SPEED input affects the output on the Serial Status Interface as indicated in the description of these register bits. The SPEED input is assumed stable and should not change after reset.
DUPLEX	Input	101	The Duplex (DUPLEX) signal indicates whether the ELAN-EPHY supports half or full duplex operation. When DUPLEX is sampled low and DSEL is sampled high, the ELAN-EPHY will default to half-duplex operation (10H_AB or 100XH_AB set high depending on SPEED). When DUPLEX is set high and DSEL is sampled high, the ELAN-EPHY will default to full-duplex operation (10F_AB or 100XF_AB set high depending on SPEED). DUPLEX is ignored when DSEL is sampled low (all four abilities will be enabled). When the Extended PHY Control 1 register bits SMODE[2:0] = "001", the DUPLEX input affects the output on the Serial Status Interface as indicated in the description of these register bits. The DUPLEX input is assumed stable and should not change after reset.

8.4. Miscellaneous Interface Signals (8)

Pin Name	Type	Pin No.	Feature
CLKI	Input	25	25 MHz clock reference input. This input is connected to one terminal of a 25 MHz crystal or a external 25 MHz clock source.
CLKO	Output	26	25 MHz crystal feedback. This output is connected to the other terminal of a 25 MHz crystal. If CLKI is driven with an external clock source, CLKO must be left open.
RSTB	Input	129	The active low reset (RSTB) signal provides an asynchronous ELAN-EPHY reset. RSTB is a Schmitt triggered input with an internal pull up resistor. When RSTB is forced low, all ELAN-EPHY registers are forced to their default states. In addition, all output pins with the exception of TDO are forced tri-state. Outputs remain tri-stated until RSTB is forced high. RSTB is used to sample the ANEGAB and A[4:2] inputs.
TCK	Input	161	The test clock (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port. The TCK signal is used as a clock source in low speed diagnostic loopback mode as indicated in the Operations section of this document.
TMS	Input	160	The test mode select (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an internal pull up resistor.

TDI	Input	159	When the ELAN-EPHY is configured for JTAG operation, the test data input (TDI) signal carries test data into the ELAN-EPHY via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Tristate	158	The test data output (TDO) signal carries test data out of the ELAN-EPHY via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Input	204	The active low test reset (TRSTB) signal provides an asynchronous ELAN-EPHY test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull up resistor. In the event that TRSTB is not used, it must be connected to RSTB.

8.5. Power, Grounds and Test (86)

Pin Name	Type	Pin No.	Feature
ATEST1[3] ATEST1[2] ATEST1[1] ATEST1[0]	Analog	200 201 202 203	The analog test signals (ATEST[3:0]) are pins reserved for providing analog test points. Under normal operation, the ATEST[3:0] pins should be connected to ground.
ATEST2[3] ATEST2[2] ATEST2[1] ATEST2[0]		165 164 163 162	
ATEST3[3] ATEST3[2] ATEST3[1] ATEST3[0]		96 97 98 99	
ATEST4[3] ATEST4[2] ATEST4[1] ATEST4[0]		61 60 59 58	

AVD1[3] AVD1[2] AVD1[1] AVD1[0] AVD2[3] AVD2[2] AVD2[1] AVD2[0] AVD3[3] AVD3[2] AVD3[1] AVD3[0] AVD4[3] AVD4[2] AVD4[1] AVD4[0]	Power	193 199 187 183 172 166 178 182 89 95 83 79 68 62 74 78	The power (AVD) pins for the analog circuitry. AVD should be connected to a clean, well decoupled, +5V supply.
AVS1[4] AVS1[3] AVS1[2] AVS1[1] AVS1[0] AVS2[4] AVS2[3] AVS2[2] AVS2[1] AVS2[0] AVS3[4] AVS3[3] AVS3[2] AVS3[1] AVS3[0] AVS4[4] AVS4[3] AVS4[2] AVS4[1] AVS4[0]	Ground	184 194 198 188 186 181 171 167 177 179 80 90 94 84 82 77 67 63 73 75	The ground (AVS) pins for the analog circuitry. AVS should be connected to a clean ground reference.

VSSF[0] VSSF[1] VSSF[2] VSSF[3] VSSF[4] VSSF[5] VSSF[6] VSSF[7]	Ground	1 52 53 104 105 156 157 208	The pad ring ground pins should be connected to GND in common with VSS_DC.
VDD_AC1 VDD_AC2 VDD_AC3 VDD_AC4 VDD_AC5 VDD_AC6 VDD_AC7 VDD_AC8	Power	8 22 31 45 112 126 135 149	The VDD_AC power pins should be connected to a well decoupled +5 V DC in common with VDD_DC.
VSS_AC1 VSS_AC2 VSS_AC3 VSS_AC4 VSS_AC5 VSS_AC6 VSS_AC7 VSS_AC8	Ground	10 24 29 43 114 128 133 147	The pad ring ground pins should be connected to GND in common with VSS_DC.
VDD_DC1 VDD_DC2 VDD_DC3 VDD_DC4 VDD_DC5	Power	15 28 38 119 142	The VDD_DC power pins should be connected to a well decoupled +5 V DC in common with VDD_AC.
VSS_DC1 VSS_DC2 VSS_DC3 VSS_DC4 VSS_DC5	Ground	16 27 37 120 141	The DC ground pins should be connected to GND in common with VSS_AC.

Notes on Pin Description:

1. All ELAN-EPHY inputs and bi-directionals present minimum capacitive loading and operate at TTL logic levels except for CLKI, which operates at CMOS logic levels.

2. ELAN-EPHY digital outputs and bi-directionals have 4 mA drive capability, except TXCLK and RXCLK, which have 8 mA drive capability.

3. Inputs RSTB, TMS, TDI and TRSTB have internal pull-up resistors.

4. The VDD_DC and VDD_AC power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage to the ELAN-EPHY.

5. The VSS_DC, VSS_AC and VSSF power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage to the ELAN-EPHY.

6. The AVD pins provide power to sensitive analog circuitry in the ELAN-EPHY. These signals should be connected to the PCB VDD power plane at a point where the supply is clean and as free as possible of digitally induced switching noise. In a typical system, AVD should be "starred" back to a clean reference point on the PCB, for example at the card edge connector where the system VDD enters the PCB. In some systems a clean VDD supply cannot be readily obtained, and AVD may require separate regulation.

7. The AVS pins provide the ground return path for sensitive analog circuitry in the ELAN-EPHY. These signals should be connected to the PCB ground plane at a point where the ground is clean and as free as possible of digital return currents. In a typical system, AVS should be "starred" back to a clean reference point on the PCB, for example at the card edge connector where the system ground reference enters the PCB.

8. Before any input activity occurs, ensure that the device power supplies are within their nominal voltage range.

9. Hold the device in the reset condition until the device power supplies are within their nominal voltage range.

10. Ensure that all digital power is applied simultaneously, and it is applied before the analog power is applied.

9. FUNCTIONAL DESCRIPTION

9.1 10BASE-T Physical Layer

Physical Medium Attachment

For receive data, the PMA provides on chip filtering and a squelch function which qualifies the data so that spurious noise events are rejected. A PLL is used to synchronize onto the MAC frame preamble and to recover the embedded clock. For transmitted data the PMA synthesizes a 20 MHz clock and drives the output buffer with the required pre distortion and output filtering.

The CRS, COL, SQE test and 10Base-T loopback behave differently for half and full duplex operation. In half duplex mode the PMA will generate CRS when data is transmitted or received; COL will be generated whenever there is simultaneous transmit and receive activity; SQE test will be generated and data will be copied from the transmit path to the receive path when no data is being received. For full duplex operation CRS is only generated on receive data activity; COL is never asserted; SQE test is not used and the receive data always comes from the MDI.

In order to prevent the PHY from erroneously transmitting for too long the PMA implements the Jabber function. If the PHY exceeds the maximum transmission time the transmitter will become idle and the COL signal will be asserted to indicate the Jabber condition.

Auto polarity correction allows the PHY to determine if the wires in the receive data pair are connected properly. By examining the polarity of the received Link Pulses the PHY can correct for the reversal of the RXDI+/- lines.

Since 10Base-T is not a continuous transmission medium, Normal Link Pulses (NLPs) are sent on the MDI when there is no data to transmit. The NLPs indicate that the link is operational. On the receive side the PMA monitors the NLPs to determine if its link partner is active. If neither data or NLPs are received for a time, the link is considered down.

Physical Layer Signaling

The PLS layer provides for receive clock recovery, receive Manchester decoding, transmit clock synthesis and transmit Manchester encoding. In addition, the PLS layer generates the COL and CRS signals and maps the bit wide data to nibbles for transfer across the MII.

When the PHY is configured to operate with a repeater controller, the PLS layer will generate CRS only for receive data and will suppress the generation of COL.

9.2 100BASE-TX Physical Layer

Physical Media Dependent

For receive data the PMD provides adaptive equalization, baseline wander correction, MLT-3 slicing, clock recovery and descrambling. The adaptive equalization scheme employed uses a master-slave equalizer that monitors the input signal quality and corrects the signal amplitude and phase. Since the scrambled 5B code with MLT-3 encoding is not DC balanced the receiver performs baseline wander correction to reduce low frequency drift of the received signal slicing levels due to AC coupling in the transformer. The slicer converts the analog MLT-3 signal by comparing the analog input with an acquired slicing level. The clock recovery section trains onto the incoming data and extracts a 125 MHz clock. If the input signal is lost the phase lock loop switches to the input reference clock as a source. This provides a continuous RXCLK at the MII. The stream cipher descrambler acquires lock on the incoming data stream by decoding IDLE symbols. Once lock has been achieved the stream cipher descrambler will come out of the lock state if 50 consecutive IDLE line state bits are not detected within 722 us.

For transmit data the PMD provides clock synthesis, scrambling and MLT-3 wave shaping. The 125 MHz transmit clock is synthesized from the reference input clock. The 4B/5B symbols are scrambled to reduce the peak amplitude in the frequency spectrum. The scrambled data is converted to MLT-3 and driven out the TXDO+/- outputs. The transmit stage is a differential current output with wave shaping which significantly reduces external filtering requirements for EMI reduction purposes.

Physical Medium Attachment

The PMA layer passes bit serial data to the PCS and also generates the link integrity indications required by the Auto-negotiation function.

Physical Coding Sublayer

For receive data the PCS provides framing to symbol boundaries, 4B/5B decoding and transmission over the MII. The PCS frames to the "JK" start of stream delimiter and keeps the same symbol boundary till the end of stream delimiter "TR" is received. The aligned symbols are converted to nibbles in the 4B/5B decoder and passed onto the MII. When operating with the symbol interface the PCS bypasses the framing and 4B/5B functions for the data and passes the unaligned symbols onto the repeater controller.

For transmit data the PCS provides the generation of the "JK" and "TR" code groups and 4B/5B encoding. The first byte of preamble from the MAC is replaced by the "JK" code group to indicate start of stream. When TXEN is de-asserted indicating the end of a frame, the PCS inserts the "TR" code group to indicate the end of stream delimiter. The symbols are then serialized and passed to the PMA. When operating in symbol mode the PCS passes the symbols to transmit transparently to the PMA after serialization. A higher layer entity is responsible for providing the "JK" and "TR" code groups to denote the start and end of each frame.

The PCS generates CRS for receive and transmit activity in half duplex mode. The PCS only generates CRS for receive activity in full duplex or when configured to operate with a repeater. For receive activity if a false carrier is detected the PCS will strobe RXER and drive RXD[3:0] with "1110" to indicate the condition.

The PCS generates COL when there is simultaneous receive and transmit activity for half duplex mode. For full duplex or when configured to operate with a repeater COL generation is suppressed.

9.3 100BASE-FX Physical Layer

Physical Media Dependent

For 100Base-FX operation the PHY disables its stream cipher, baseline wander and MLT-3 functions. The PHY outputs NRZI data. The PHY is capable of interfacing to an ODL driver directly from its RXDI+/- and TXDO+/- pins.

The remaining 100Base-FX functionality is the same as 100Base-TX.

9.4 Auto-Negotiation Controller

The Auto-negotiation controller allows the ELAN-EPHY to advertise enhanced modes of operation it possesses to a device at the remote end of a link segment, to detect corresponding enhanced operational modes that the other device maybe advertising and to select an appropriate operational mode. The auto-negotiation process is transparent to the user. The ELAN-EPHY can connect to 10Base-T and 100Base-Tx PHYs that which may or may not posses auto-negotiation capabilities. The ELAN-EPHY negotiates each PHY independently of the other PHYs and thus can operate with a variety of 10Base-T and 100Base-Tx configurations.

9.5 Serial Status Interface

The Serial Status Interface (SSI) enables the ELAN-EPHY to multiplex each PHYs status indication signals onto a common interface. Each PHY by default outputs six status signals. These signals are serialized with the status signals from the other

PHYs and output on the SSI. The SSI can be customized to provide any combination of the default status outputs or to provide vendor specific status outputs. The vendor specific status outputs are selected via the Extended PHY Control One register.

9.6 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The ELAN-EPHY identification code is 033040CD hexadecimal.

9.7 Serial Management Interface

The Serial Management Interface (SMI) provides access to the registers used for control and monitoring of the PHY. The SMI supports the Control, Status, PHY Identifier, Auto-negotiation Advertisement, Link Partner Ability and Expansion registers. In addition, the SMI supports vendor specific registers. The vendor specific registers are used to provide advanced control and status of the PHY. The ELAN-EPHY has a unique base address starting at the value indicated by the A[4:2] pins and incrementing for each PHY sequentially (A+0, A+1, A+2, A+3).

Below is a register map for a PHY. Each PHY has its own set of registers.

Normal Mode Register Memory Map

PHY	Address	Register
One	0x00	Control
	0x01	Status
	0x02	PHY Identifier, Upper Word
	0x03	PHY Identifier, Lower Word
	0x04	Auto-Negotiation Advertisement
	0x05	Auto-Negotiation Link Partner Ability
	0x06	Auto-Negotiation Expansion
	0x07 - 0x0F	Reserved
	0x10	Extended PHY Control One
	0x11	Extended PHY Control Two
	0x12	Reserved
	0x13	Extended PHY Status One
	0x14	Reserved
	0x15 - 0x1E	Reserved
	0x1F	Test Control
Two	0x00	Control
	0x01	Status
	0x02	PHY Identifier, Upper Word
	0x03	PHY Identifier, Lower Word
	0x04	Auto-Negotiation Advertisement
	0x05	Auto-Negotiation Link Partner Ability
	0x06	Auto-Negotiation Expansion
	0x07 - 0x0F	Reserved
	0x10	Extended PHY Control One
	0x11	Extended PHY Control Two
	0x12	Reserved
	0x13	Extended PHY Status One
	0x14	Reserved
	0x15 - 0x1E	Reserved
	0x1F	Test Control

PHY	Address	Register
Three	0x00	Control
	0x01	Status
	0x02	PHY Identifier, Upper Word
	0x03	PHY Identifier, Lower Word
	0x04	Auto-Negotiation Advertisement
	0x05	Auto-Negotiation Link Partner Ability
	0x06	Auto-Negotiation Expansion
	0x07 - 0x0F	Reserved
	0x10	Extended PHY Control One
	0x11	Extended PHY Control Two
	0x12	Reserved
	0x13	Extended PHY Status One
	0x14	Reserved
	0x15 - 0x1E	Reserved
	0x1F	Test Control
Four	0x00	Control
	0x01	Status
	0x02	PHY Identifier, Upper Word
	0x03	PHY Identifier, Lower Word
	0x04	Auto-Negotiation Advertisement
	0x05	Auto-Negotiation Link Partner Ability
	0x06	Auto-Negotiation Expansion
	0x07 - 0x0F	Reserved
	0x10	Extended PHY Control One
	0x11	Extended PHY Control Two
	0x12	Reserved
	0x13	Extended PHY Status One
	0x14	Reserved
	0x15 - 0x1E	Reserved
	0x1F	Test Control

10. NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the ELAN-EPHY. Each PHY within the ELAN-EPHY has its own set of registers. The register numbers are the same for each PHY; only the PHY address is unique.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the ELAN-EPHY to determine the programming state of the block.

3. Writable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect ELAN-EPHY operation unless otherwise noted.

5. Certain register bits are reserved. To ensure that the ELAN-EPHY operates as intended, reserved register bits must only be written with their default values. Similarly, writing to reserved registers should be avoided.

Register 0x0:
Control

Bit	Type	Function	Default
Bit 15	R/W	RESET	0
Bit 14	R/W	LOOPBACK	0
Bit 13	R/W	SPEED	0/1
Bit 12	R/W	ANEG_EN	0/1
Bit 11	R/W	PWR_DN	0
Bit 10	R/W	ISOLATE	0
Bit 9	R/W	ANEG_RES	0
Bit 8	R/W	DUPLEX	0/1
Bit 7	R/W	COL_TST	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

COL_TST:

The Collision Test (COL_TST) bit is used to test the COL signal at the MII. When COL_TST is set to one the PHY will assert the COL signal within 512 bit times in response to the assertion of TXEN and de-assert COL within 4 bit times of TXEN being de-asserted. When COL_TST is set to zero the collision test function is inactive.

DUPLEX:

The DUPLEX bit is used to control the duplex mode of operation for the PHY only when the ANEG_EN bit is set to zero, indicating that the auto-negotiation function is not being used. When ANEG_EN is set to one, this bit has no effect on duplex mode of operation.

Writing a logic one to this bit sets full-duplex mode, while a logic zero sets half-duplex mode. However, if the Status register indicates that only one mode is available, this bit will be read only - writes will not affect it.

The default value of this bit is zero. However, if the Status register indicates that only one mode is available, this bit will default accordingly.

ANEG_RES:

The Auto-Negotiation Restart (ANEG_RES) bit is used to restart the Auto-negotiation process. When set high ANEG_RES will re-initiate the Auto-negotiation process. ANEG_RES will be cleared by the PHY after the Auto-negotiation process has been started.

If ANEG_EN is set to zero (auto-negotiation function disabled), or the Status register indicates that an auto-negotiation function is disabled, this bit will be read only - writes will not affect it.

ISOLATE:

The ISOLATE bit is used to electrical isolate the PHY's data paths from the MII. Setting this bit to one will cause the corresponding PHY to not respond to TXD[3:0], TXEN and TXER inputs and tri-state TXCLK, RXCLK, RXDV, RXER, RXD[3:0], COL and CRS outputs. Setting ISOLATE to zero will enable the MII interface.

Even when the PHY is isolated it shall respond to management transactions.

PWR_DN:

The Power Down (PWR_DN) bit is used to place the PHY in a low power state. Writing a one to PWR_DN will place the PHY into a low power consumption state. Setting PWR_DN to zero will allow normal operation.

Even when the PHY is powered down it shall respond to management transactions.

ANEG_EN:

The Auto-Negotiation Enable (ANEG_EN) bit controls the operation of the auto-negotiation function, as well as determine where some PHY control signals are sourced from.

When ANEG_EN is set to one, then the Auto-negotiation process will determine the link configuration (such as speed of operation and duplex mode). When ANEG_EN is set to zero, the SPEED and DUPLEX register bits in the Control register will determine the link configuration.

If the Status register indicates that the auto-negotiation function is not present, this bit will be read only - writes will not affect it.

The default value for this bit is taken from the Status register bit 3 (ANEG_AB).

SPEED:

The SPEED bit is used to select the link speed of the PHY when the ANEG_EN bit is set to zero (auto-negotiation disabled). When ANEG_EN is set to one, this bit has no effect on the link speed.

Writing a logic one to SPEED sets 100 Mbps mode. Writing a logic zero to this bit sets 10 Mbps mode. However, if the Status register indicates that only one mode is available, this bit will be read only - writes will not affect it.

The default value of this bit is one. However, if the Status register indicates that only one mode is available, this bit will default accordingly.

LOOPBACK:

The LOOPBACK bit is used to control PHY loopback operation. Writing a one to this bit places the PHY into the diagnostic loopback test mode. While in LOOPBACK the PHY will be isolated from the network medium and collision detection will be disabled. Writing a zero to this bit returns the PHY to normal operation. The LOOPBACK mode of operation is valid in both 10Base-T and 100Base-X modes of operation. The PHY will loopback data in less than 512 bit times. For more details on this LOOPBACK mode of operation, please refer to the Operations section of this document.

RESET:

The RESET bit is used to generate an internal "soft" reset. Internally, the soft reset places all registers into their default state. The soft reset does not affect the management interface. After this bit is set, it will automatically clear after 500 ms. Writing a zero to this bit before the reset procedure is complete may lead to unpredictable behavior.

Register 0x1:
Status

Bit	Type	Function	Default
Bit 15	R	100T4_AB	0
Bit 14	R	100XF_AB	0/1
Bit 13	R	100XH_AB	0/1
Bit 12	R	10F_AB	0/1
Bit 11	R	10H_AB	0/1
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	MFPRESUP	0
Bit 5	R	ANEG_COMP	0
Bit 4	R	RF	0
Bit 3	R	ANEG_AB	0/1
Bit 2	R	LS	0
Bit 1	R	JBD	0
Bit 0	R	EXTEND	1

EXTEND:

The EXTEND bit indicates whether the PHY supports the extended register space as defined in IEEE Std 802.3u. Since the PHY does support this register space, this bit is set to one.

JBD:

The Jabber Detected (JBD) bit indicates whether the PHY detected a jabber condition. This bit is set to a logic one when a jabber condition is detected. This bit clears when the register is read and at reset. This bit is disabled in 100BASE-X mode.

LS:

The Link Status (LS) bit indicates whether the link is good.

When the link fails, the LS bit is cleared and stays cleared till the register is read. LS is also cleared at reset. This LS bit is set when the register is read and the link is good.

ANEG_AB:

The Auto-Negotiation Ability (ANEG_AB) bit indicates whether the PHY

supports the auto-negotiation function. The value of ANEG_AB reflects the value of the ANEGAB input.

RF:

The Remote Fault (RF) bit indicates that the PHY has detected a fault in its link partner. This bit is set to a logic one when this condition is determined. This bit clears when the register is read. RF takes its value from the Auto-Negotiation Expansion register bit 13.

ANEG_COMP:

The Auto-Negotiation Complete (ANEG_COMP) bit indicates that the auto-negotiation function has successfully completed.

If the ANEG_EN bit in the Control register is logic zero (auto-negotiation disabled), this bit will be a logic zero.

ANEG_COMP will be set to one when the Auto-negotiation process has been completed and the contents of the Auto-negotiation Advertisement, Auto-negotiation Link Partner Ability and Auto-negotiation Expansion registers are valid. ANEG_COMP will be set to zero while the Auto-negotiation process is in progress and the contents of the above registers are not valid.

MFPRESUP:

The Management Frame Preamble Suppression (MFPRESUP) bit indicates whether the PHY will accept management frames without the preamble or not. Since the PHY requires the preamble, this bit is set to a zero.

10H_AB:

The 10Base-T Half-Duplex Ability (10H_AB) bit indicates that the PHY supports this mode of operation. When 10H_AB is set high the PHY supports 10Base-T half-duplex mode. The default value of 10H_AB depends on the DSEL, FXMODE, SPEED and DUPLEX input pins.

DSEL	SPEED	DUPLEX	FXMODE	10H_AB
1	0	0	X	1
1	0	1	X	0
1	1	0	X	0
1	1	1	X	0
0	X	X	0	1
0	X	X	1	0

10F_AB:

The 10Base-T Full-Duplex Ability (10F_AB) bit indicates that the PHY supports this mode of operation. The default value of 10F_AB depends on the DSEL, FXMODE, SPEED and DUPLEX input pins.

DSEL	SPEED	DUPLEX	FXMODE	10F_AB
1	0	0	X	0
1	0	1	X	1
1	1	0	X	0
1	1	1	X	0
0	X	X	0	1
0	X	X	1	0

100XH_AB:

The 100Base-Tx Half-Duplex Ability (100XH_AB) bit indicates that the PHY supports this mode of operation. The default value of 100XH_AB depends on the DSEL, FXMODE, SPEED and DUPLEX input pins.

DSEL	SPEED	DUPLEX	FXMODE	100XH_AB
1	0	0	X	0
1	0	1	X	0
1	1	0	X	1
1	1	1	X	0
0	X	X	X	1

100XF_AB:

The 100Base-Tx Full-Duplex Ability (100XF_AB) bit indicates that the PHY supports this mode of operation. The default value of 100XH_AB depends on the DSEL, FXMODE, SPEED and DUPLEX input pins.

DSEL	SPEED	DUPLEX	FXMODE	100XF_AB
1	0	0	X	0
1	0	1	X	0
1	1	0	X	0
1	1	1	X	1
0	X	X	X	1

100T4_AB:

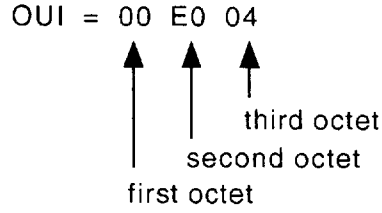
The 100Base-T4 Ability (100T4_AB) bit indicates that the PHY supports this mode of operation. Since the PHY does not support T4 operation, this bit is set to zero.

Register 0x2:
PHY Identifier, Upper Word

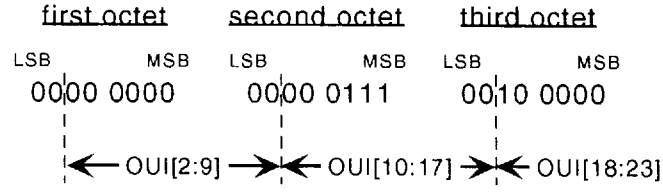
Bit	Type	Function	Default
Bit 15 to Bit 0	R	OUI[2:17]	001CH

OUI[3:18]:

The Organizationally Unique Identifier (OUI) field is a 24-bit field assigned by the IEEE to a PHY manufacturer. Its value is 00E004H. The mapping of the OUI to the PHY Identifier register is described below.



Each octet is represented as a conventional two digit hexadecimal numeral where the first (left-most) digit of the pair is the more significant. The mapping of the OUI to registers 2 and 3 of the ELAN-EPHY is described below.



Register 2 [15:0] = OUI[2:17] = 001C

Register 3 [15:10] = OUI[18:23] = 20

Register 0x3:
PHY Identifier, Lower Word

Bit	Type	Function	Default
Bit 15 to Bit 10	R	OUI[18:23]	20H
Bit 9 to Bit 4	R	MODEL[5:0]	1H
Bit 3 to Bit 0	R	REV[3:0]	0H

OUI[19:24]:

The Organizationally Unique Identifier (OUI) field is a 24-bit field assigned by the IEEE to a PHY manufacturer. Its value is 00E004H.

MODEL[5:0]:

The Manufacturer's Model Number (MODEL) field is a 6-bit field used to differentiate this PHY from others made by PMC-Sierra. Its value is 1H.

REV[3:0]:

The Revision Number (REV) field is a 4-bit field to indicate the revision number of this PHY. Its value is 0H.

Register 0x4:
Auto-Negotiation Advertisement

Bit	Type	Function	Default
Bit 15	R/W	NP	0
Bit 14	R	Reserved	0
Bit 13	R/W	RF	0
Bit 12 to Bit 5	R/W	A[7:0]	00H-1FH
Bit 4 to Bit 0	R/W	S[4:0]	00001

These register bits default as indicated during reset or when autonegotiation is restarted. An update of these register bits should be followed by writing a logic one to the autonegotiation restart (ANEG_RES) bit in the Control register.

S[4:0]:

The Selector Field (S) forms bits D0 to D4 of the Link Code Word sent by the PHY for Auto-negotiation.

A[7:0]:

The Technology Ability Field (A) forms bits D5 to D12 of the Link Code Word sent by the PHY for Auto-negotiation.

The default value for this field is derived from the most significant five bits of the Status register. The upper three bits of this field can be written by the user. The default value of this field is as follows:

A[7:5] = 0
A[4] = Status register, Bit 15
A[3] = Status register, Bit 14
A[2] = Status register, Bit 13
A[1] = Status register, Bit 12
A[0] = Status register, Bit 11

RF:

The Remote Fault (RF) bit forms bit D13 of the Link Code Word sent by the PHY for Auto-negotiation.

NP:

The Next Page (NP) bit forms bit D15 of the Link Code Word sent by the PHY for Auto-negotiation. Since the PHY does not support the Next Page register, this bit should always be set to zero.

Register 0x5:
Auto-Negotiation Link Partner Ability

Bit	Type	Function	Default
Bit 15	R	NP	0
Bit 14	R	ACK	0
Bit 13	R	RF	0
Bit 12 to Bit 5	R	A[7:0]	00H
Bit 4 to Bit 0	R	S[4:0]	00000

This register may not be valid until the Status register indicates that Auto-negotiation has been successfully completed via the ANEG_COMP bit being set to one.

S[4:0]:

The Selector Field (S) represents bits D0 to D4 of the Link Code Word received by the PHY during Auto-negotiation.

A[7:0]:

The Technology Ability Field (A) represents bits D5 to D12 of the Link Code Word received by the PHY during Auto-negotiation.

The bits in the technology ability field are defined in IEEE Std 802.3u as follows:

A[7:5] = Reflect what's received on the line from the link partner
A[4] = 100Base-T4
A[3] = 100Base-TX full duplex
A[2] = 100Base-TX
A[1] = 10Base-T full duplex
A[0] = 10Base-T

RF:

The Remote Fault (RF) bit represents bit D13 of the Link Code Word received by the PHY during Auto-negotiation. This bit is also used to set the RF bit in the Status register.

ACK:

The Acknowledge (ACK) bit represents bit D14 of the Link Code Word received by the PHY during Auto-negotiation.

NP:

The Next Page (NP) bit represents bit D15 of the Link Code Word received by the PHY during Auto-negotiation.

Register 0x6:
Auto-Negotiation Expansion

Bit	Type	Function	Default
Bit 15 to Bit 5	R	Reserved	0
Bit 4	R	PD_FAULT	0
Bit 3	R	LPNPAB	0
Bit 2	R	NP_AB	0
Bit 1	R	PG_RX	0
Bit 0	R	LPANAB	0

This register may not be valid until the Status register indicates that auto-negotiation has been successfully completed via the ANEG_COMP bit being set to one.

LPANAB:

The Link Partner Auto-Negotiation Able (LPANAB) bit indicates that the Auto-negotiation function determined that the PHY at the other end of the link supports Auto-negotiation. LPANAB is set to logic one to indicate that the link partner supports Auto-Negotiation.

PG_RX:

The Page Received (PG_RX) bit indicates that the Auto-negotiation function has received a new page (3 consecutive identical link code words). PG_RX is set to logic one to indicate that a new page has been received. PG_RX is cleared when the register is read or upon reset.

NP_AB:

The Next Page Able (NP_AB) bit indicates whether the local PHY's Auto-negotiation function supports the next page feature. Since the PHY does not implement the Next Page register, this bit is set to logic zero.

LPNPAB:

The Link Partner Next Page Able (LPNPAB) bit indicates that the Auto-negotiation function determined that the PHY at the far end of the link supports the next page feature. LPNPAB is set to logic one to indicate that the link partner is next page able.

PD_FAULT:

The Parallel Detection Fault (PD_FAULT) bit indicates that a fault has been detected in the parallel detection function of the Auto-negotiation function. This bit is set to a logic one when a fault has been detected via parallel detection function (more than one technology present and indicating ready). PD_FAULT is cleared when the register is read or upon reset.

Register 0x10:
Extended PHY Control One

Bit	Type	Function	Default
Bit 15 to Bit 13	R/W	Reserved[2:0]	0H
Bit 12	R/W	DLCS	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	ISOL_SWPR	0
Bit 9	R/W	RXEN_SYNC	0
Bit 8	R/W	BYPSCR	0
Bit 7	R/W	FXMODE	0
Bit 6	R/W	SYMBL	0
Bit 5	R/W	RPTR	0
Bit 4	R/W	SMODE[2]	0
Bit 3	R/W	SMODE[1]	0
Bit 2	R/W	SMODE[0]	0
Bit 1	R/W	SQEC	0
Bit 0	R/W	JFE	1

JFE:

The Jabber Function Enable (JFE) bit enables the jabber function in the PHY (10Base-T only). When JFE is set to logic one, the PHY will perform Jabber detection on the transmit data.

SQEC:

The SQE control (SQEC) bit is used to control the signal quality error test in the 10 Mbps PHY (half-duplex only). When SQEC is set to logic one, the PHY will perform the SQE test function by strobing the COL signal, after the transmission of a packet, to indicate that the collision detect circuitry is functioning. When SQEC is set to logic zero the SQE test is not performed by the PHY.

SMODE[2:0]:

The Status Mode (SMODE[2:0]) bits define the operational mode of the serial status interface. For more details on this mode of operation, please refer to the Functional Timing and Operations sections of this document.

SMODE[2:0]	Mapping
000	PMC
001	VSP_ONE
010-111	Reserved

RPTR:

The Repeater (RPTR) bit configures the PHY for operation with a MAC or RIC. When set to logic one, RPTR indicates the PHY should be configured to operate with RICs and will only generate CRS for receive medium activity and will not generate the COL indication.

When set to logic zero, RPTR indicates the PHY should be configured to operate with a MACs and will generate CRS for receive and transmit medium activity and will generate the COL indication.

SYMBL:

The Symbol (SYMBL) bit configures the PHY for MII or symbol interface operation. When set to logic zero, SYMBL indicates the PHY should be configured to operate with a MII interface. When set to logic one, SYMBL indicates the PHY should be configured to operate with a symbol interface.

FXMODE:

The Fiber Mode select (FXMODE) bit configures the PHY to use the fiber based PMD. When set to logic one, FXMODE indicates the PHY should be configured for 100Base-FX operation. When set to logic zero, FXMODE indicates the PHY should be configured for 100Base-TX operation.

BYPSCR:

The Bypass Scrambler select (BYPSCR) bit configures the PHY to bypass its 100Base-X stream cipher scrambling function.

If FXMODE is high the stream cipher scrambler will automatically be bypassed. If FXMODE is low, then BYPSCR can be used to bypass the scrambler.

When set to logic one, BYPSCR indicates the PHY should bypass its stream cipher scrambling function. When set to logic zero, FXMODE indicates the PHY should utilize it's scrambler.

RXEN_SYNC:

The RXEN synchronization (RXEN_SYNC) bit indicates if the PHY should synchronize RXEN to RXCLK before enabling the receive MII port. When set to logic zero, RXEN_SYNC indicates the PHY should not synchronize RXEN. When set to logic one, RXEN_SYNC indicates the PHY should synchronize RXEN.

When RXEN is synchronized, the PHY will enable the tri-state Rx MII drivers on the falling edge of RXCLK. The PHY updates the Rx MII output signals on the rising edge of RXCLK. This ensures that there are no spurious transitions on the Rx MII output signals.

ISOL_SWPR:

The ISOL_SWPR bit indicates whether PHY to MII isolation is based on the value of the ISOL pin or the value of the ISOLATE Control register bit. When set to logic one, PHY to MII isolation is determined by the logic value of the ISOLATE Control register bit. When set to logic zero, PHY to MII isolation for all PHY's is determined by the logic value of the ISOL pin.

FEFD_EN:

The Far End Fault Detect Enable (FEFD_EN) bit enables the far end fault generation and detection circuitry. When set to logic one, the far end fault generation and detection circuitry are enabled. When set to logic zero, the far end fault generation and detection circuitry are disabled.

DLCS:

The Diagnostic Loopback Clock Select (DLCS) bit is used to select the clock source for diagnostic loopback. The DLCS bit is only valid in 100Base-X mode. When set to logic one, the TCK pin is used as a clock source in place of the Tx and Rx PLL clocks. When set to logic zero, the clock source is taken from the Tx and Rx PLLs. For more details on this mode of operation, please refer to the Operations section of this document.

Reserved[2:0]:

The Reserved bits should be written with a logic zero to ensure proper operation of the PHY.

Register 0x11:
Extended PHY Control Two (SMODE=000)

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	DPL_POL	1
Bit 12	R/W	SPD_POL	1
Bit 11	R/W	LNK_POL	1
Bit 10	R/W	COL_POL	1
Bit 9	R/W	TXA_POL	1
Bit 8	R/W	RXA_POL	1
Bit 7	R/W	Reserved	1
Bit 6	R/W	Reserved	1
Bit 5	R/W	DPL_EN	1
Bit 4	R/W	SPD_EN	1
Bit 3	R/W	LNK_EN	1
Bit 2	R/W	COL_EN	1
Bit 1	R/W	TXA_EN	1
Bit 0	R/W	RXA_EN	1

The bit definitions for the Extended PHY Control Two register are dependent on the SMODE[2:0] bits. The above mapping is the default PMC mode. Vendor specific mappings are possible by selecting the appropriate SMODE.

RXA_EN, TXA_EN, COL_EN, LNK_EN, SPD_EN, DPL_EN:

The Enable (EN) bits indicate if the corresponding bit should be shifted out of the serial status interface. If the *_EN bit is set to one the status will be shifted out. If the *_EN bit is set to zero the bit will be dropped and the status information word concatenated.

RXA_POL, TXA_POL, COL_POL, LNK_POL, SPD_POL, DPL_POL:

The Polarity (POL) bits indicate if the polarity of the corresponding status bit. If the *_POL bit is set to one the status bit will be active high. If the *_POL bit is set to zero the status bit will be active low.

Register 0x11:
Extended PHY Control Two (SMODE=001)

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	Reserved	1
Bit 12	R/W	Reserved	1
Bit 11	R/W	TX_RED_POL	1
Bit 10	R/W	TX_GRN_POL	1
Bit 9	R/W	RX_RED_POL	1
Bit 8	R/W	RX_GRN_POL	1
Bit 7	R/W	Reserved	1
Bit 6	R/W	Reserved	1
Bit 5	R/W	Reserved	1
Bit 4	R/W	ONLINE	1
Bit 3	R/W	LINK_EN	1
Bit 2	R/W	RX_EN	1
Bit 1	R/W	TX_EN	1
Bit 0	R/W	LED_MODE	1

The bit definitions for the Extended PHY Control Two register are dependent on the SMODE[2:0] bits. The above mapping is the VSP_ONE mode. The Extended PHY Control Two register should be configured to the desired default values before SMODE selects the VSP_ONE status mode. The enables for VSP_ONE status mode default to 0FH.

LED_MODE, TX_EN, RX_EN, LINK_EN, ONLINE:

These register bits are set by VSP_ONE and are used in the generation of the RX_GRN, RX_RED, TX_GRN and TX_RED status signals.

RX_GRN_POL, RX_RED_POL, TX_GRN_POL, TX_RED_POL:

The Polarity (POL) bits indicate if the polarity of the corresponding status bit. If the *_POL bit is set to one the status bit will be active high. If the *_POL bit is set to zero the status bit will be active low.

Register 0x13:
Extended PHY Status One

Bit	Type	Function	Default
Bit 15	R	PHY_100EN	0
Bit 14	R	PHY_10EN	0
Bit 13	R	ANEG_FAIL	X
Bit 12	R	DPLV	X
Bit 11	R	LNKV	X
Bit 10	R	COLV	X
Bit 9	R	TXAV	X
Bit 8	R	RXAV	X
Bit 7	R	SCRLV	X
Bit 6	R	LOSV	X
Bit 5	R	FLP_LINK_GOOD_CHECK	X
Bit 4	R	ACK_DETECT	X
Bit 3	R	ABILITY_DETECT	X
Bit 2	R	LOSI	X
Bit 1	R	SCRLI	X
Bit 0	R	JBDI	X

JBDI:

The Jabber Detect Indicator (JBDI) bit is used to indicate that a Jabber condition was detected by the PHY (10Base-T only). When set to a logic one, JBDI indicates that a Jabber condition has been detected. JBDI is cleared when the register is read.

SCRLI:

The Stream Cipher Scrambler Lock Indicator (SCRLI) bit is used to indicate the receive stream cipher scrambler has locked onto the incoming data (100Base-X only). SCRLI is cleared when the register is read.

LOSI:

The Loss of Signal Indicator (LOSI) bit is used to indicate insufficient signal levels on the receive MDI pins (100Base-X only). When LOSI is high, the PHY has insufficient signal levels on the receive MDI pins. When LOSI is low, the PHY signal levels on the receive MDI pins are sufficient. This bit is cleared when the register is read.

When the FX PMD is being utilized, insufficient signal levels are indicated via the SDI pins.

ABILITY_DETECT:

The Ability Detect (ABILITY_DETECT) bit indicates how far autonegotiation has progressed. When ABILITY_DETECT is high, the ELAN-EPHY has entered the state where it is trying to determine the link partners abilities. When ABILITY_DETECT is low, the ELAN-EPHY has not entered this state. This bit is cleared when the register is read. Please refer to clause 28 of the IEEE 802.3u specification for further details.

ACK_DETECT:

The Acknowledge Detect (ACK_DETECT) bit indicates how far autonegotiation has progressed. When ACK_DETECT is high, the ELAN-EPHY has entered the state where it is waiting for acknowledgment that the link partner has recognized the ELAN-EPHYs autonegotiation capabilities. When ACK_DETECT is low, the ELAN-EPHY has not entered this state. This bit is cleared when the register is read. Please refer to clause 28 of the IEEE 802.3u specification for further details.

FLP_LINK_GOOD_CHECK:

The Fast Link Pulse Link Good Check (FLP_LINK_GOOD_CHECK) bit indicates how far autonegotiation has progressed. When FLP_LINK_GOOD_CHECK is high, the ELAN-EPHY has entered the state where it is waiting sufficient time to allow the link partner to complete autonegotiation. The ELAN-EPHY has completed its portion of the autonegotiation algorithm at this point. When FLP_LINK_GOOD_CHECK is low, the ELAN-EPHY has not entered this state. This bit is cleared when the register is read. Please refer to clause 28 of the IEEE 802.3u specification for further details.

LOSV:

The Loss of Signal Value (LOSV) bit is read to determine the current loss of signal state of the PHY (100Base-X only).

SCRLV:

The Stream Cipher Scrambler Lock Value (SCRLI) bit is read to determine the current state of the stream cipher scrambler in the PHY (100Base-X only).

RXAV:

The Receive Activity Value (RXAV) bit indicates if the PHY is currently receiving data. When RXAV is high the PHY is receiving data. When RXAV is low there is no receive activity.

The RXAV bit reflects the value of RXA status indication outputted on the SSI when the SMODE[2:0] bits from the Extended PHY Control 1 register are "000".

TXAV:

The Transmit Activity Value (TXAV) bit indicates if the PHY is currently transmitting data. When TXAV is high the PHY is transmitting data. When TXAV is low there is no transmit activity.

The TXAV bit reflects the value of TXA status indication outputted on the SSI when the SMODE[2:0] bits from the Extended PHY Control 1 register are "000".

COLV:

The Collision Value (COLV) bit indicates if the PHY is experiencing a collision. When COLV is high the PHY is experiencing a collision. When COLV is low the PHY is not experiencing a collision on its medium.

The COLV bit reflects the value of COL status indication outputted on the SSI when the SMODE[2:0] bits from the Extended PHY Control 1 register are "000".

LNKV:

The Link Value (LNKV) bit indicates if the PHY's links are valid. When LNKV is high the PHY's links are valid and operational. When LNKV is low the PHY's links are down.

The LNKV bit reflects the value of LNK status indication outputted on the SSI when the SMODE[2:0] bits from the Extended PHY Control 1 register are "000".

DPLV:

The Duplex Value (DPLV) bit indicates the selected duplex mode of the PHY. When DPLV is high full-duplex mode of operation has been selected. When DPLV is low half-duplex mode of operation has been selected.

The DPLV bit reflects the value of DPL status indication outputted on the SSI when the SMODE[2:0] bits from the Extended PHY Control 1 register are "000".

ANEG_FAIL:

The Auto-Negotiation Failure (ANEG_FAIL) bit indicates that the Auto-negotiation function was not able to successfully communicate with its link partner. ANEG_FAIL is not valid when Auto-negotiation has been disabled.

ANEG_FAIL is set to a logic one after a failure condition is detected. ANEG_FAIL is cleared when Auto-negotiation is completed or upon reset.

PHY_10EN:

The 10Base-T PHY Enable (PHY_10EN) bit is used to indicate that this speed of PHY was chosen and is enabled.

PHY_100EN:

The 100Base-TX/FX PHY Enable (PHY_100EN) bit is used to indicate that this speed of PHY was chosen and is enabled.

11. TEST FEATURES DESCRIPTION

Test mode registers are used to apply test vectors during production testing of the ELAN-EPHY.

In addition, the ELAN-EPHY also supports a standard IEEE 1149.1 five signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port. Analog pins cannot be accessed via the JTAG port.

11.1. Test Mode Register Memory Map

PHY #	Address	Register
One	0x00-0x1E 0x1F	Normal Mode Registers Test Control
Two	0x00-0x1E 0x1F	Normal Mode Registers Test Control
Three	0x00-0x1E 0x1F	Normal Mode Registers Test Control
Four	0x00-0x1E 0x1F	Normal Mode Registers Test Control

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 0x1F:
Test Control

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	TOUT[15:0]	0

The TOUT[15:0] field is used to control production test functions in the ELAN-EPHY.

11.2. JTAG Test Port

The ELAN-EPHY JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Identification Register

Length - 32 bits
Version number - 0H
Part Number - 3304H
Manufacturer's identification code - 0CDH
Device identification - 033040CDH

Boundary Scan Register

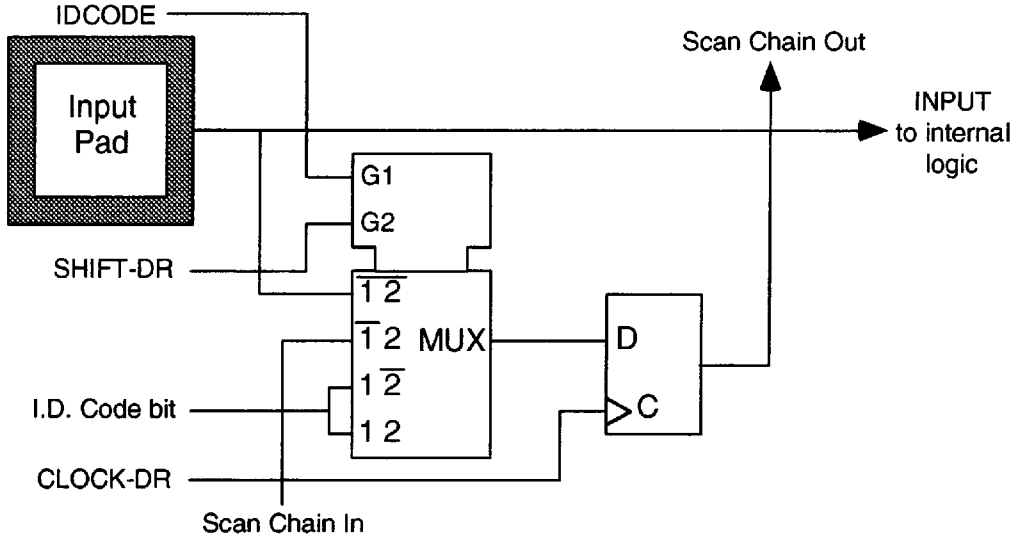
The boundary scan register is made up of 98 boundary scan cells, divided into input observation (in_cell), output (out_cell), and bi-directional (io_cell) cells. These cells are detailed in the pages which follow. The first 32 cells form the ID code register, and carry the code 033040CDH. The cells are arranged as follows:

Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
DUPLEX	97	IN_CELL	0 (16)	CRS1	53	IO_CELL	
SPEED	96	IN_CELL	0 (16)	COL1	52	OUT_CELL	
DSEL	95	IN_CELL	0 (16)	TXCLK1	51	OUT_CELL	
ISOL	94	IN_CELL	0 (16)	TXER3	50	IN_CELL	
SYMBL	93	IN_CELL	0	TXEN3	49	IN_CELL	
FXMODE	92	IN_CELL	0	TXD3[3:0]	48:45	IN_CELL	
RPTR	91	IN_CELL	1	RXEN3	44	IN_CELL	
MODE[0:1]	90:89	IN_CELL	10	RXCLK3	43	OUT_CELL	
RSTB	88	IN_CELL	0	RXDV3	42	OUT_CELL	
SYSCLK (1)	87	IN_CELL	1	RXER3	41	OUT_CELL	
MDC	86	IN_CELL	1	RXD3[3:0]	40:37	OUT_CELL	
MDIO	85	IO_CELL	0	CRS3	36	IO_CELL	
MDO_EN (2)	84	OUT_CELL	0	COL3	35	OUT_CELL	
CRS_EN1 (3)	83	OUT_CELL	0	TXCLK3	34	OUT_CELL	
CRS_EN2 (4)	82	OUT_CELL	0	TXER4	33	IN_CELL	
CRS_EN3 (5)	81	OUT_CELL	0	TXEN4	32	IN_CELL	
CRS_EN4 (6)	80	OUT_CELL	1	TXD4[3:0]	31:28	IN_CELL	
RXMII_EN1 (7)	79	OUT_CELL	0	RXEN4	27	IN_CELL	
RXMII_EN2 (8)	78	OUT_CELL	0	RXCLK4	26	OUT_CELL	
RXMII_EN3 (9)	77	OUT_CELL	0	RXDV4	25	OUT_CELL	
RXMII_EN4 (10)	76	OUT_CELL	0	RXER4	24	OUT_CELL	
ISOL1 (11)	75	OUT_CELL	0	RXD4[3:0]	23:20	OUT_CELL	
ISOL2 (12)	74	OUT_CELL	0	CRS4	19	IO_CELL	
ISOL3 (13)	73	OUT_CELL	1	COL4	18	OUT_CELL	
ISOL4 (14)	72	OUT_CELL	1	TXCLK4	17	OUT_CELL	
SDATA	71	OUT_CELL	0	TXER2	16	IN_CELL	
SCLK	70	OUT_CELL	0	TXEN2	15	IN_CELL	
SFRM	69	OUT_CELL	1	TXD2[3:0]	14:11	IN_CELL	
SENB (15)	68	OUT_CELL	1	RXEN2	10	IN_CELL	
TXER1	67	IN_CELL	0	RXCLK2	9	OUT_CELL	
TXEN1	66	IN_CELL	1	RXDV2	8	OUT_CELL	
TXD1[3:0]	65:62	IN_CELL		RXER2	7	OUT_CELL	
RXEN1	61	IN_CELL		RXD2[3:0]	6:3	OUT_CELL	
RXCLK1	60	OUT_CELL		CRS2	2	IO_CELL	
RXDV1	59	OUT_CELL		COL2	1	OUT_CELL	
RXER1	58	OUT_CELL		TXCLK2	0	OUT_CELL	
RXD1[3:0]	57:54	OUT_CELL					

NOTES:
1. SYSCLK is assumed to be connected to CLKI.
2. MDO_EN selects the direction of MDIO.
3. CRS_EN1 selects the direction of CRS1.

4. CRS_EN2 selects the direction of CRS2.
5. CRS_EN3 selects the direction of CRS3.
6. CRS_EN4 selects the direction of CRS4.
7. RXMII_EN1 is the active low output enable for RXCLK1, RXDV1, RXER1 and RXD1[3:0].
8. RXMII_EN2 is the active low output enable for RXCLK2, RXDV2, RXER2 and RXD2[3:0].
9. RXMII_EN3 is the active low output enable for RXCLK3, RXDV3, RXER3 and RXD3[3:0].
10. RXMII_EN4 is the active low output enable for RXCLK4, RXDV4, RXER4 and RXD4[3:0].
11. ISOL1 is the active low output enable for COL1 and TXCLK1.
12. ISOL2 is the active low output enable for COL2 and TXCLK2.
13. ISOL3 is the active low output enable for COL3 and TXCLK3.
14. ISOL4 is the active low output enable for COL4 and TXCLK4.
15. SENB is the active low output enable for SDATA, SCLK and SFRM.
16. This version bit can be reconfigured with a metal layer modification.

Fig. 11.1 Input Observation Cell (IN_CELL)



In this diagram and those that follow, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the table above.

Fig. 11.2 Output Cell (OUT_CELL)

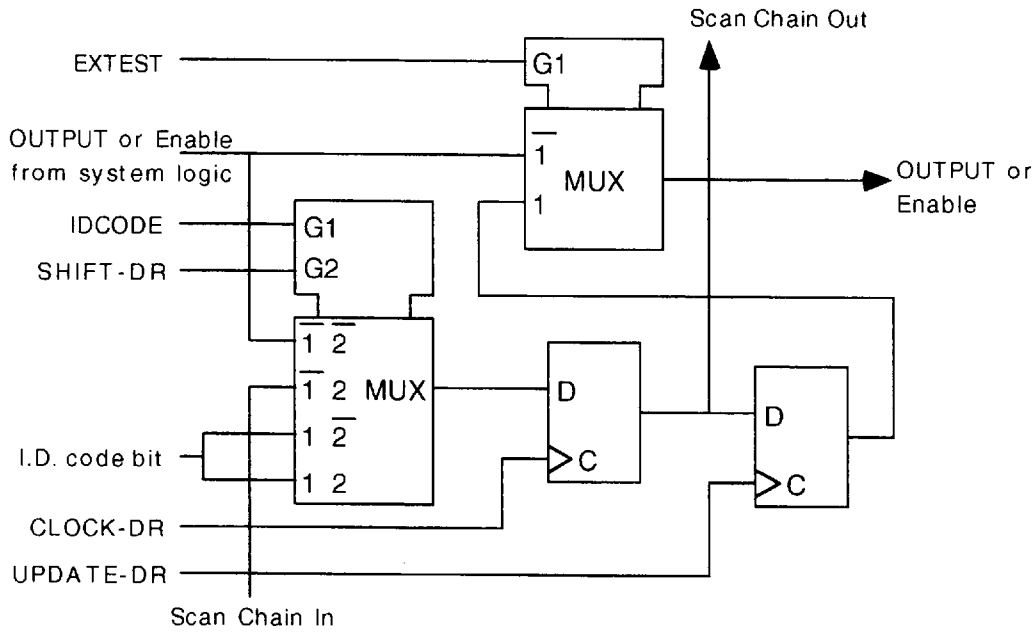


Fig. 11.3 Bidirectional Cell (IO_CELL)

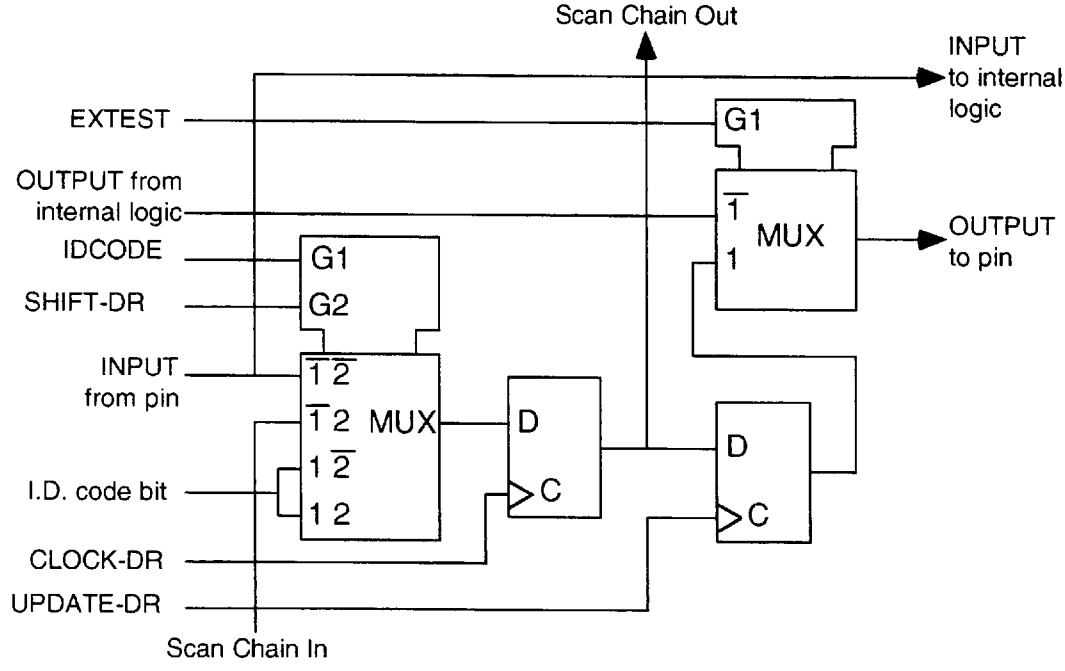
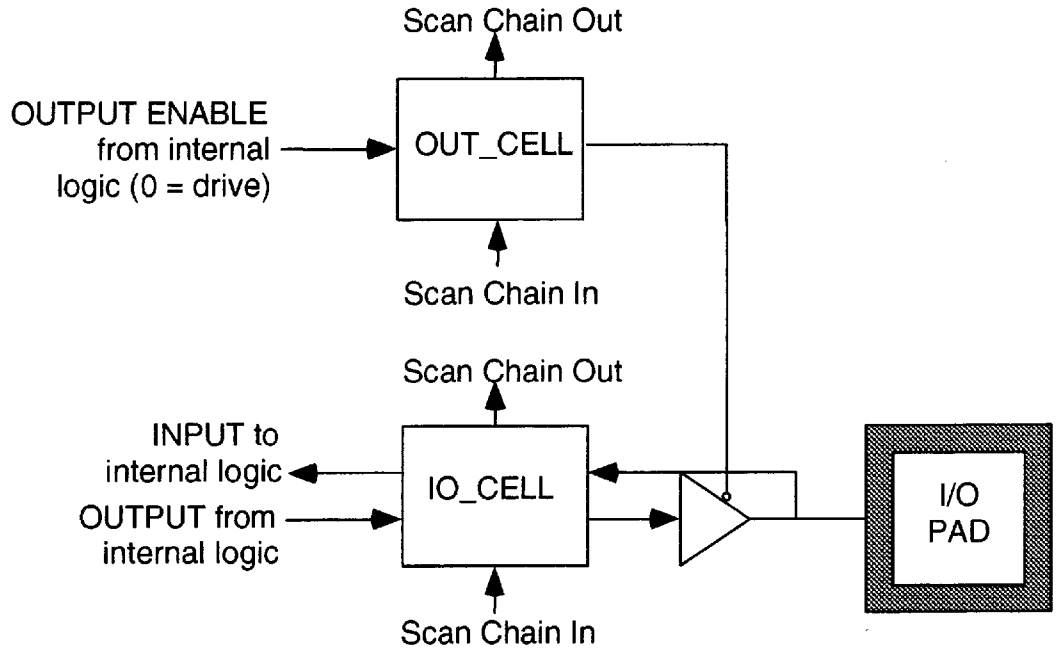


Fig. 11.4 Layout of Output Enable and Bidirectional Cells



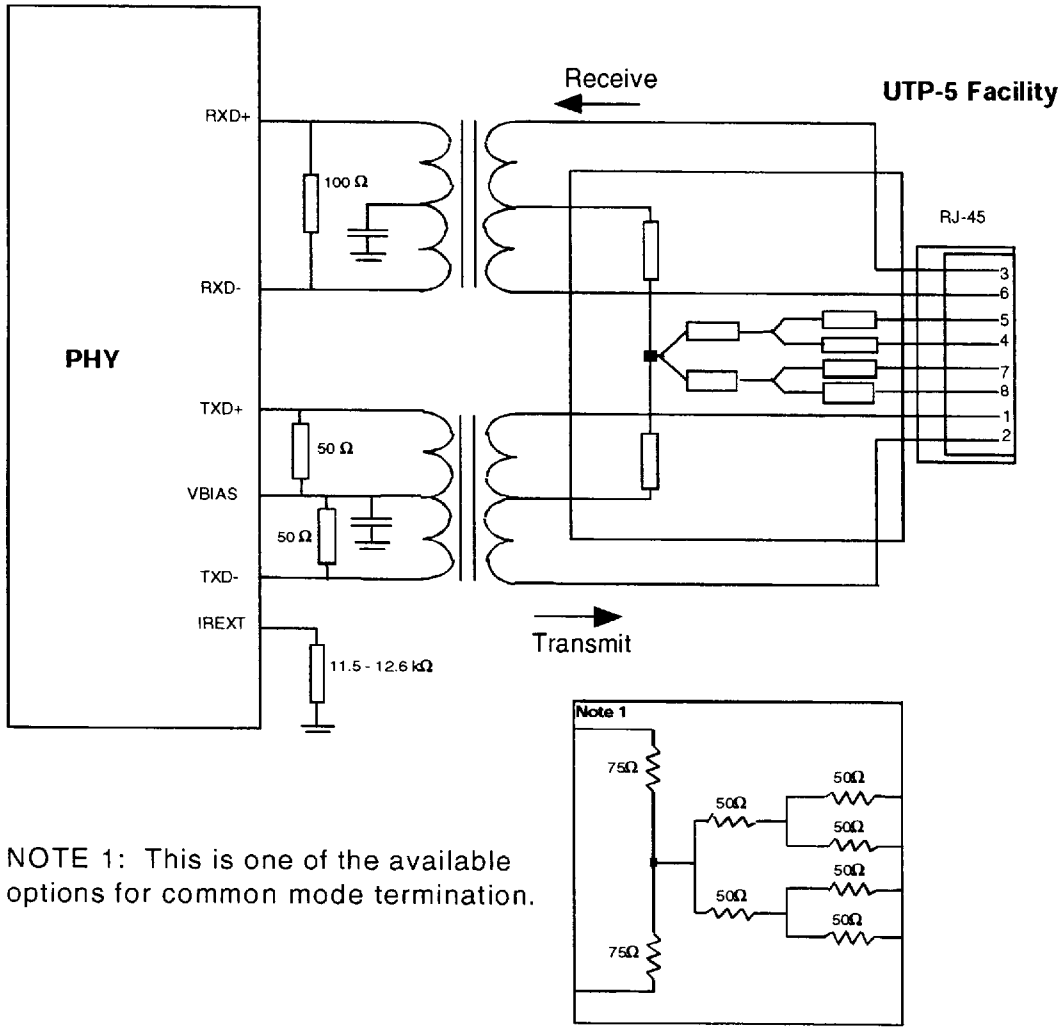
12. OPERATION

This section presents interface connection details for the ELAN-EPHY and operating details for the JTAG boundary scan feature. Bit delay constraints through the ELAN-EPHY are also included.

12.1. UTP-5 Magnetics Passives

Figure 12.1 is an example of using the ELAN-EPHY for UTP-5 applications.

Fig. 12.1 UTP-5 Magnetics



NOTE 1: This is one of the available options for common mode termination.

12.2. PECL Termination Passives

Below is an example of using the ELAN-EPHY for fiber applications. Figure 12.2 demonstrates the PECL Transmit termination and figure 12.3 demonstrates the PECL Receive termination.

Fig. 12.2 PECL Transmit Termination

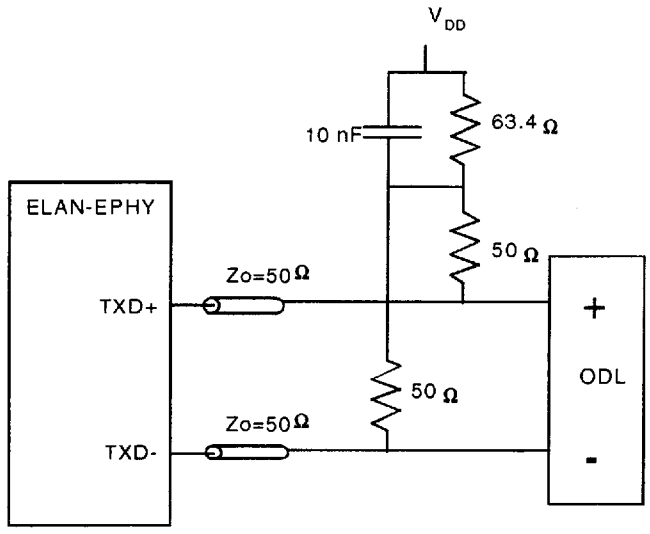
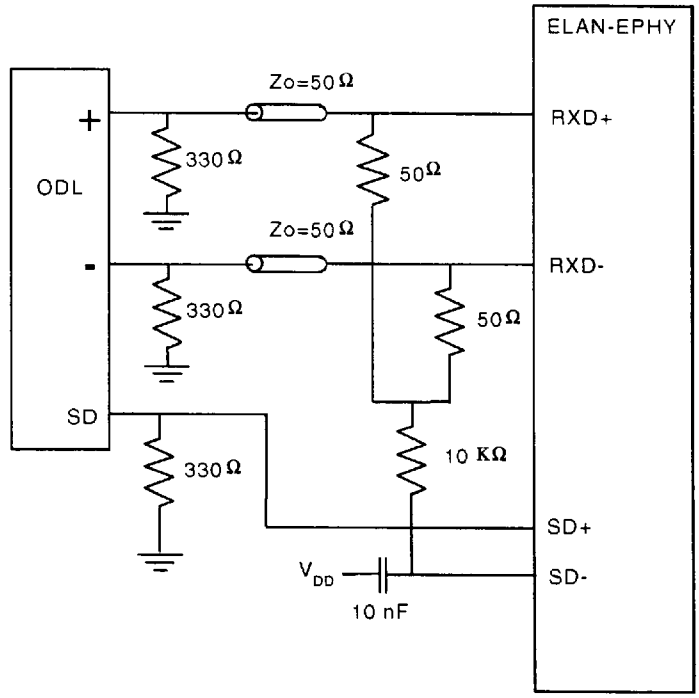


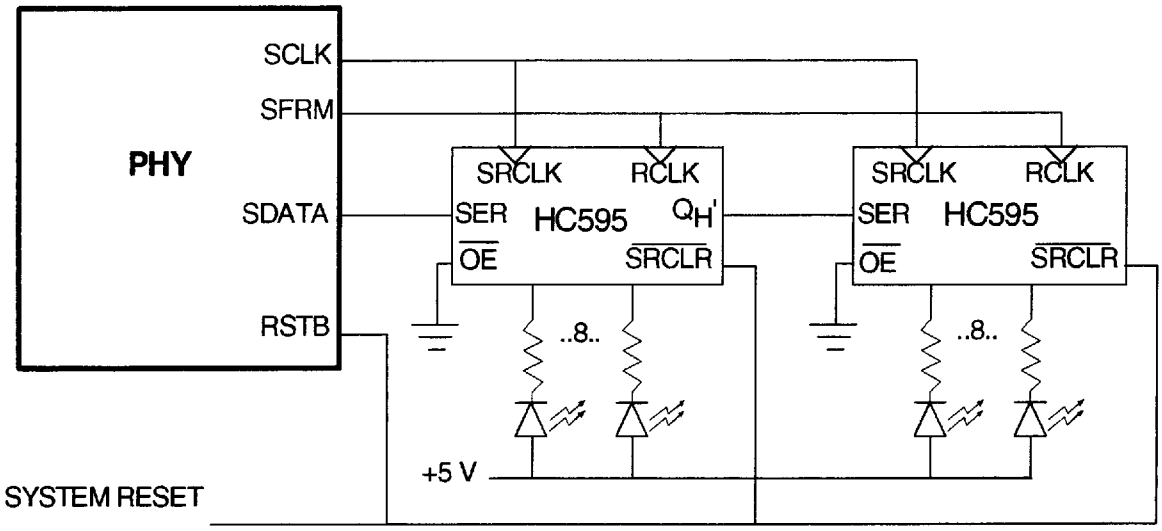
Fig. 12.3 PECL Receive Termination



12.3. Serial Status LED Output Decoder

Figure 12.4 is an example of using the ELAN-EPHY serial status output for controlling Status LED's using shift registers. In this example, the polarity of the output status signals is active low.

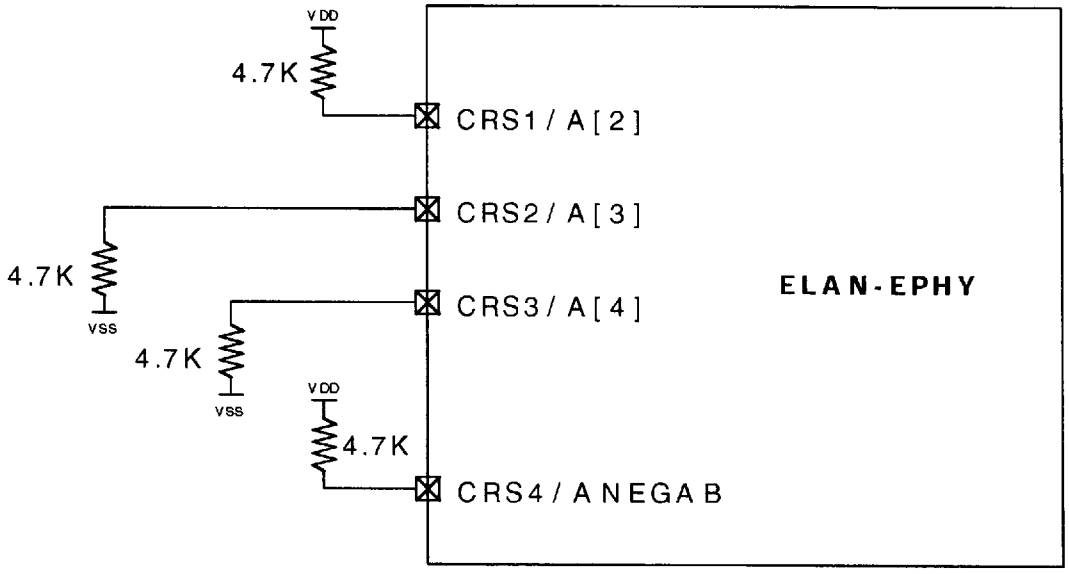
Fig. 12.4 Shift Register Status LED for Serial Status Interface



12.4. Pull-ups and Pull-downs on CRS / ANEGAB pins

Figure 12.5 is an example of how to pull-up / pull-down the CRS and ANEGAB pins to set the ELAN-EPHY base address. These pins are sampled on reset to establish the base address for serial management cycles. In this example, the ELAN-EPHY base address is 0x04 and the ELAN-EPHY is autonegotiation capable. Serial management transactions with PHY address 0x04 denotes PHY1, address 0x05 denotes PHY2, address 0x06 denotes PHY3 and 0x07 denotes PHY4.

Fig. 12.5 Pull-up / Pull-down example for CRS / ANEGAB pins



12.5. Loopback Modes

Below are examples of using the ELAN-EPHY in one of its 5 loopback modes. The path taken by data through the device is highlighted in bold. The blocks through which data passes is shaded. The path taken by the Tx and Rx clocks is also highlighted in bold. Figure 12.6 illustrates the at speed 100Base-X diagnostic loopback mode. Figure 12.7 illustrates the low speed 100Base-X diagnostic loopback mode. Figure 12.8 illustrates the timing relationship between TCK and CLKI for the low speed 100Base-X diagnostic loopback mode to function correctly. Figure 12.9 illustrates the 10Base-T diagnostic loopback mode. Figure 12.10 illustrates the 10Base-T natural auto-loopback mode.

Fig. 12.6 At Speed Diagnostic Loopback (100Base-X)

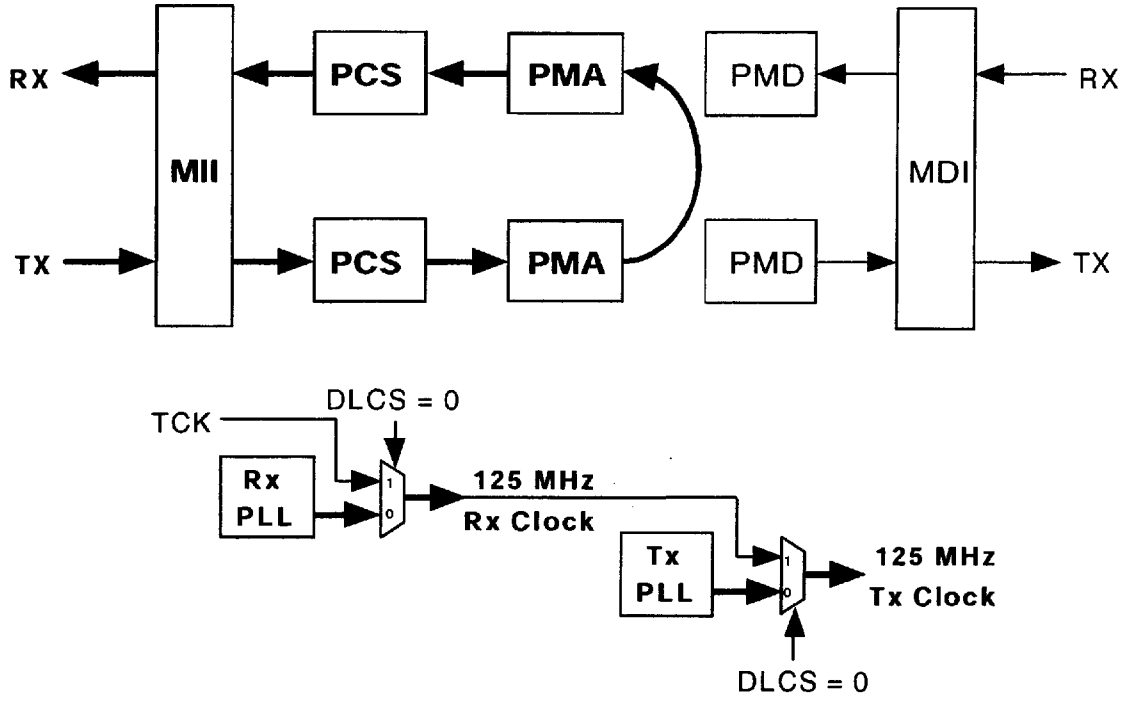
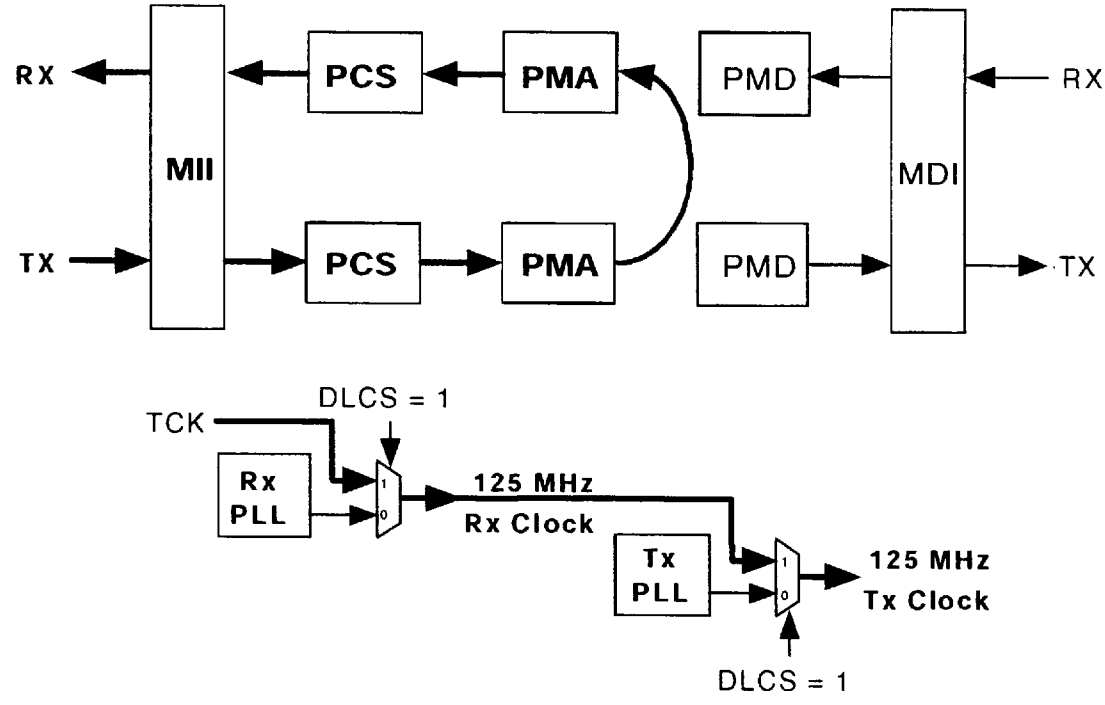


Fig. 12.7 Low Speed Diagnostic Loopback (100Base-X)



The falling edge of TCK should be aligned with the rising edge of CLKI to ensure correct operation of the Low Speed Diagnostic Loopback mode. Figure 12.8 below illustrates the timing relationship between TCK and CLKI.

Fig. 12.8 Timing Relationship between TCK and CLKI for Fig. 12.7

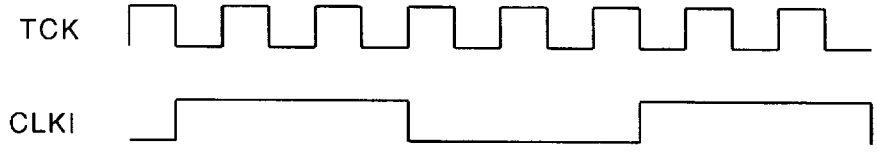


Fig. 12.9 Diagnostic Loopback (10Base-T)

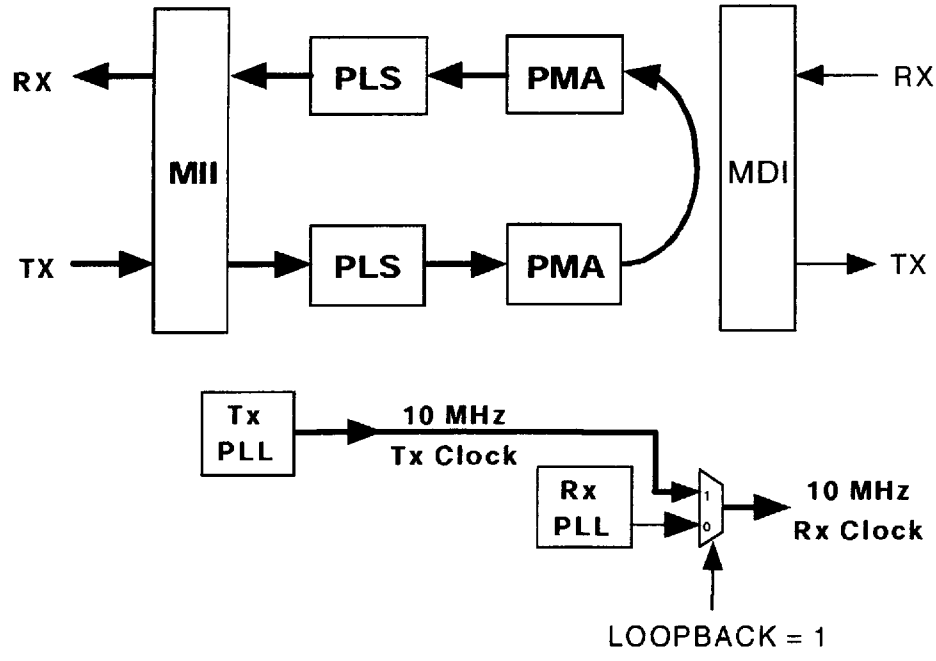
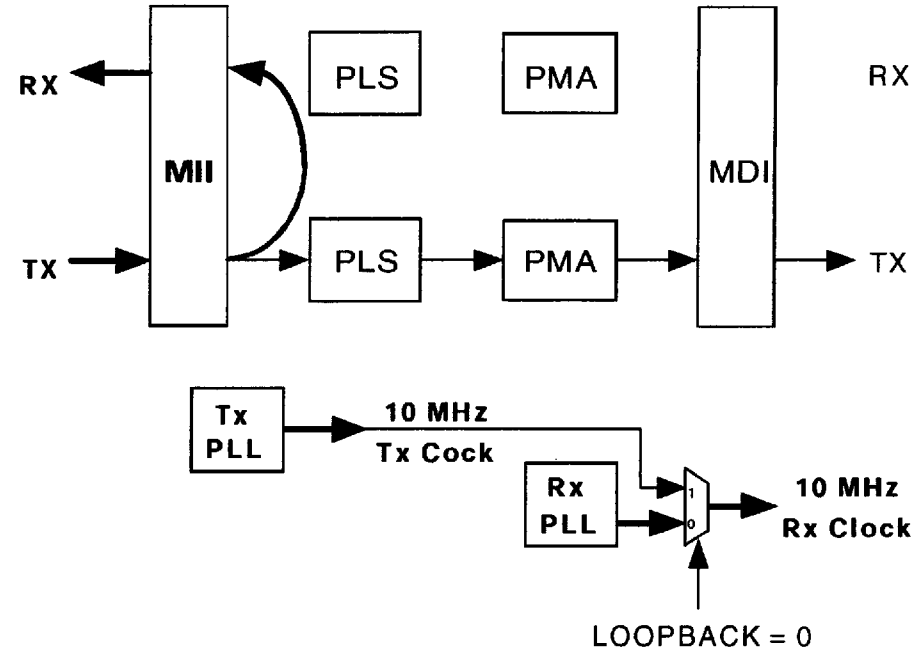


Fig. 12.10 Natural Auto-Loopback (10Base-T)



12.6. Bit Delay Constraints (100Base-X)

Below are tables describing the delay budget through the ELAN-EPHY for the receive and transmit data streams and the CRS and COL control signals when operating in 100Base-X mode. The first table contains delays for when the ELAN-EPHY is configured to interface to MAC devices via the MII. The second table contains delays for when ELAN-EPHY interfaces to RICs via the symbol interface.

MDI to MII Interface Delay Constraints (100Base-X)

Timing Event	Min (bits)	Max (bits)	Input Timing Reference	Output Reference
TXEN sampled to MDI output	6	14	TXCLK rising	1st bit of /J/
MDI input to RXD		21	1st bit of /J/	/J/ on RXD
MDI input to CRS assert		20	1st bit of /J/	
MDI input to CRS de-assert (aligned)	13	24	1st bit of /T/	
MDI input to CRS de-assert (unaligned)	13	24	1st ONE	
MDI input to COL assert		20	1st bit of /J/	
MDI input to COL de-assert (aligned)	13	24	1st bit of /T/	
MDI input to COL de-assert (unaligned)	13	24	1st ONE	
TXEN sampled to CRS assert	0	4	TXCLK rising	
TXEN sampled to CRS de-assert	0	16	TXCLK rising	

MDI to Symbol Interface Delay Constraints (100Base-X)

Timing Event	Min (bits)	Max (bits)	Input Timing Reference	Output Reference
TXEN sampled to MDI output		5	TXCLK rising	1st bit of /J/
MDI input to RXD		12.5	1st bit of /J/	/J/ on RXD
MDI input to CRS assert		20	1st bit of /J/	
MDI input to CRS de-assert (aligned)	13	24	1st bit of /T/	
MDI input to CRS de-assert (unaligned)	13	24	1st ONE	
MDI input to COL assert		20	1st bit of /J/	
MDI input to COL de-assert (aligned)	13	24	1st bit of /T/	
MDI input to COL de-assert (unaligned)	13	24	1st ONE	
TXEN sampled to CRS assert	0	4	TXCLK rising	
TXEN sampled to CRS de-assert	0	16	TXCLK rising	

12.7. Bit Delay Constraints (10Base-T)

Below is a table describing the delay budget through the ELAN-EPHY for the receive and transmit data streams and the CRS and COL control signals when operating in 10Base-T mode. The table contains delays for when the ELAN-EPHY is configured to interface to MAC devices via the MII.

MDI to MII Interface Delay Constraints (10Base-T)

Timing Event	Min (bits)	Max (bits)	Input Timing Reference	Output Reference
TXEN sampled to MDI output		4	TXCLK rising	1st bit of preamble
MDI input to RXD (steady-state)		12	1st bit if first data nibble	1st data nibble
MDI input to CRS assert		6	1st bit of preamble	
MDI input to CRS de-assert	16	22	Last data transition	
MDI input to COL assert		6	1st bit of preamble	
MDI input to COL de-assert	16	22	Last data transition	
TXEN sampled to CRS assert	0	4	TXCLK rising	
TXEN sampled to CRS de-assert	0	4	TXCLK rising	

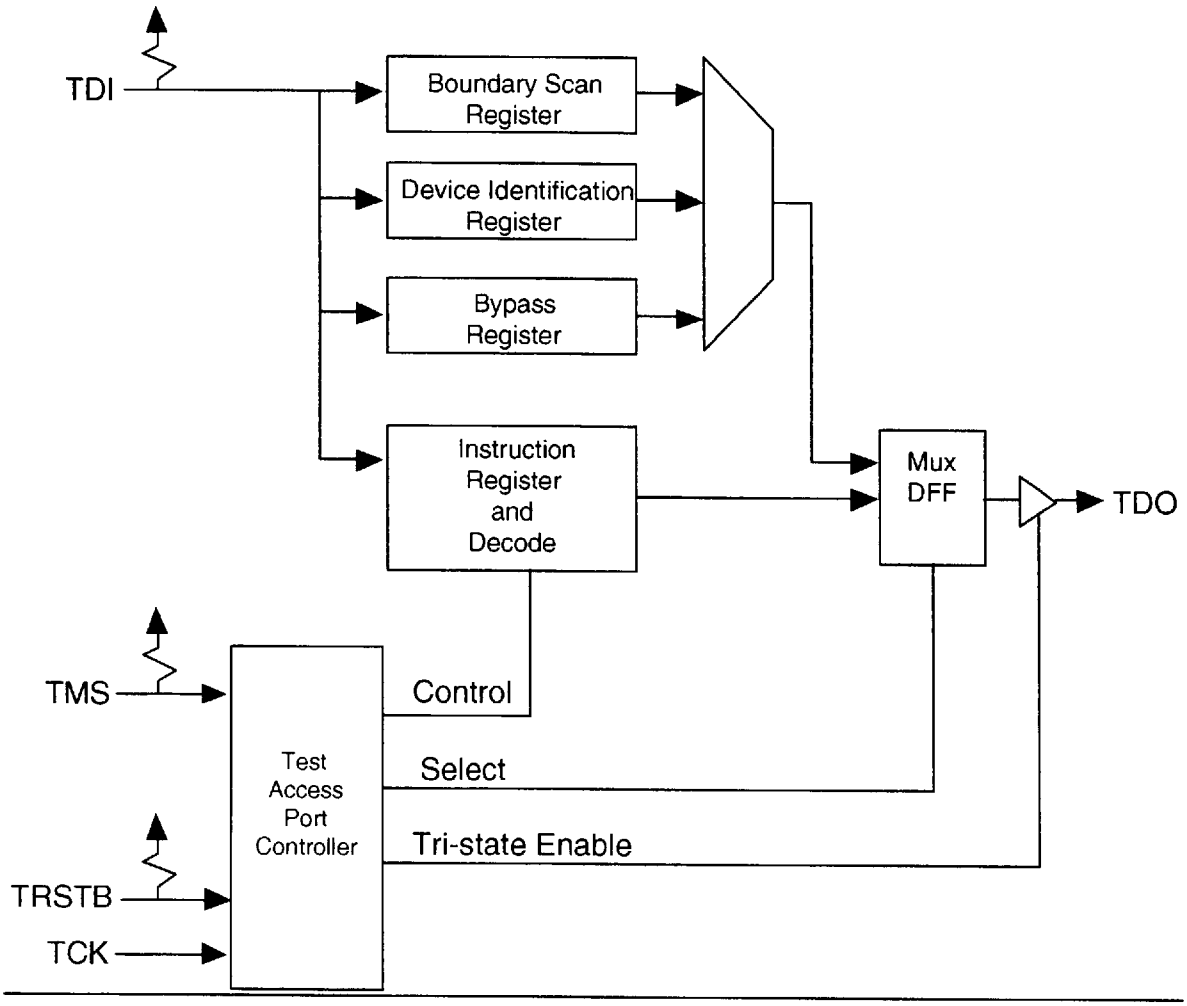
12.8. VSP_ONE Status Interface

When SMODE is set to select the VSP_ONE Status Interface (SMODE=001) the SPEED pin performs the function of the YELLOW control signal and the DUPLEX pin performs the function of the BLINK control signal. Before enabling the VSP_ONE mode the Extended PHY Control Two register should be set to the appropriate default values.

12.9. JTAG Support

The ELAN-EPHY supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Fig. 12.11 Boundary Scan Architecture



The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single bit delay from primary input, TDI to primary output , TDO. The device identification register contains the device identification code.

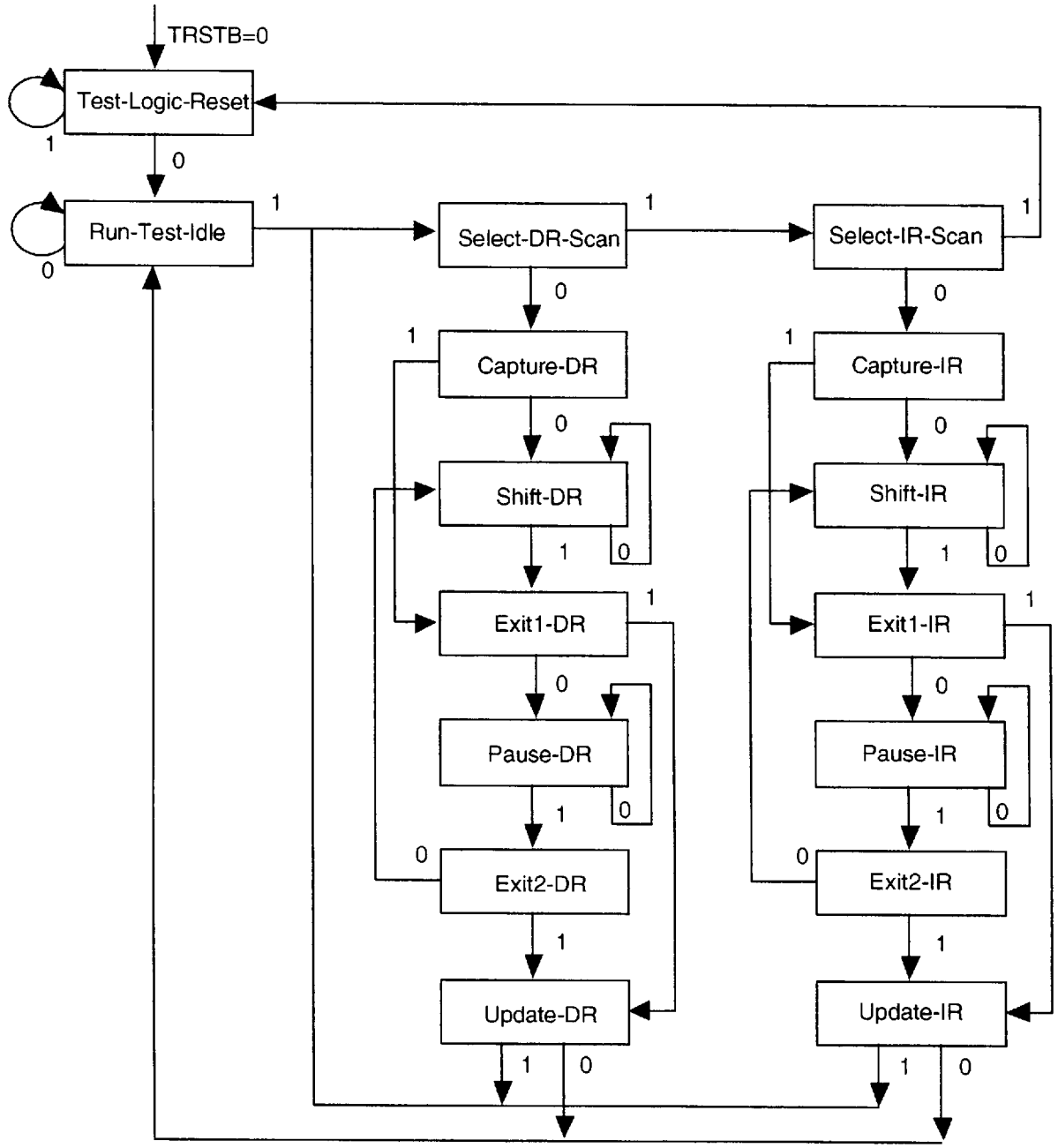
The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register placed in series with device inputs and

outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Fig. 12.12 TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

INTEST

The internal test instruction is used to exercise the device's internal core logic. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Update-DR state, patterns shifted in on input, TDI are used to drive primary inputs. During the

Capture-DR state, primary outputs are sampled and loaded into the boundary scan register.

12.10. Board Design Recommendations

The noise environment and signal integrity are often the limiting factors in system performance. Therefore, the following board design guidelines *must* be followed in order to ensure proper operation.

1.) Connect digital and analog grounds together at a point where the ground reference is clean and as free as possible of digital return currents. Typically, this means as close as possible to the PCB connector where ground is brought into the card.

2.) Provide separate +5 volt analog and +5 volt digital supplies, but otherwise connect the supply voltages together at a point where the supply is clean and as free as possible of digitally induced switching noise. Typically, this means as close as possible to the PCB connector where +5 volts is brought into the card.

3.) Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is probably the best approach provided care is taken to ensure the IR drop in the resistor does not lower the supply voltage below the recommended operating voltage.

4.) Ferrite beads are recommended for AVD1-4.

5.) Separate high-frequency decoupling capacitors are recommended for each analog power (AVD1-4) pin as close to the package pin as possible. Separate decoupling is required to prevent the transmitter from coupling noise into the receiver and to prevent transients from coupling into the reference circuitry.

6.) The high speed serial streams (TXDO1-4+/- and RXDI1-4+/-) must be routed with controlled impedance circuit board traces and must be terminated with a matched load. Further, the length of the traces on each differential pair should match to ensure the differential signals maintain their phase relationship. Normal TTL-type design rules are not recommended and will reduce the performance of the device.

13. FUNCTIONAL TIMING

13.1. MII Interface

Fig. 13.1 Transmit Medium Independent Interface - no collisions

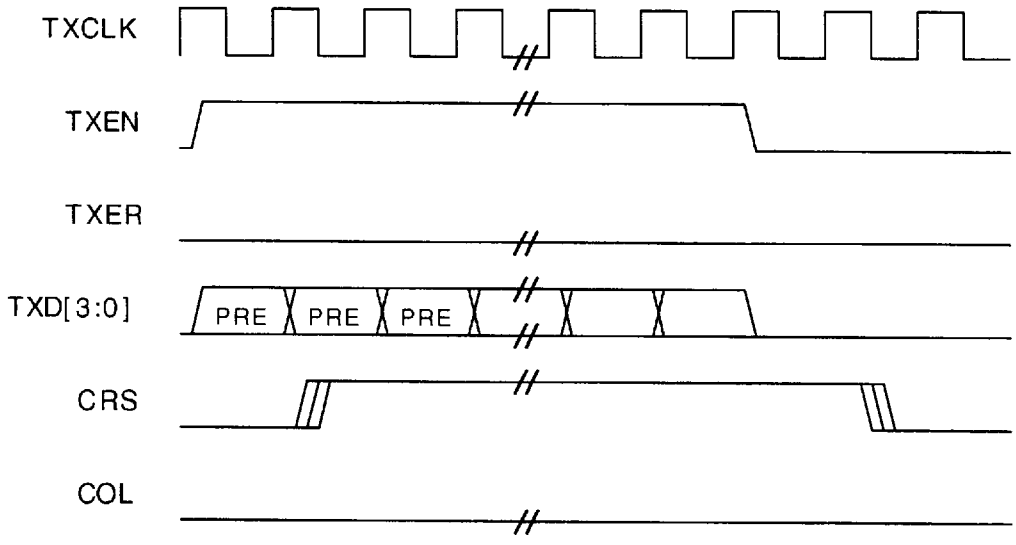


Figure 13.1 illustrates data transfer on the Transmit (Tx) Medium Independent Interface (MII) of the ELAN-EPHY device assuming no collisions. The ELAN-EPHY device recognizes the data on TXD[3:0] as valid on every rising edge of TXCLK that TXEN is sampled high and TXER is sampled low. TXEN is asserted with the first nibble of the preamble and shall remain asserted while all nibbles to be transmitted are presented to the ELAN-EPHY device. TXEN is negated prior to the first rising edge of TXCLK following the final nibble of a frame.

When operating in half duplex mode, the ELAN-EPHY device asserts CRS in response to sampling TXEN high to indicate the detection of a carrier. The ELAN-EPHY device negates CRS in response to sampling TXEN low to indicate loss of carrier. When operating in full duplex mode, CRS is unaffected by data transfer on the Tx MII.

When operating in half duplex mode, COL remains low to indicate no collisions have been detected. When operating in full duplex mode, collisions cannot occur and COL always remains low.

Fig. 13.2 Transmit Medium Independent Interface - collisions

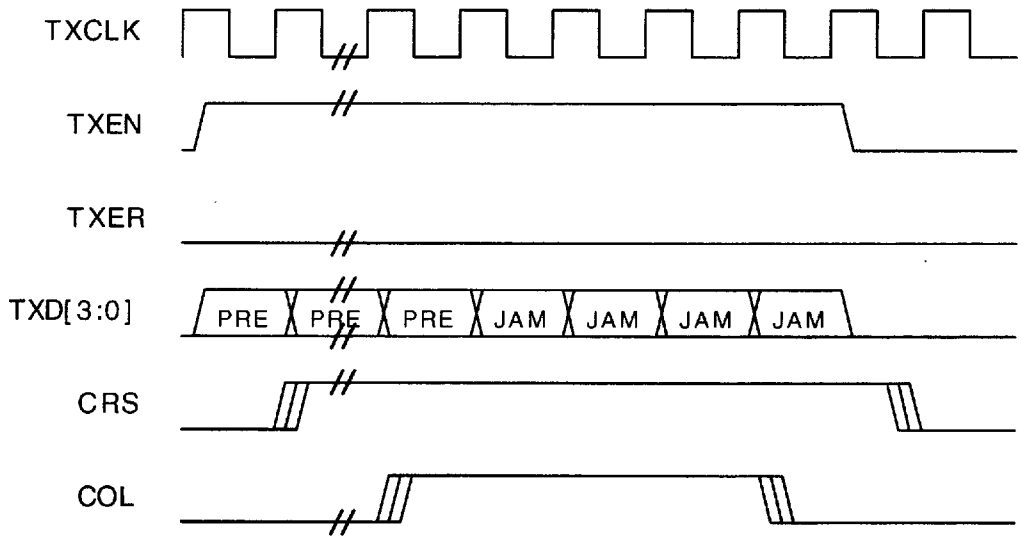


Figure 13.2 illustrates data transfer on the Transmit (Tx) Medium Independent Interface (MII) of the ELAN-EPHY device with collisions. The ELAN-EPHY device recognizes the data on TXD[3:0] as valid on every rising edge of TXCLK that TXEN is sampled high and TXER is sampled low. TXEN is asserted with the first nibble of the preamble and shall remain asserted while all nibbles to be transmitted are presented to the ELAN-EPHY device. TXEN is negated prior to the first rising edge of TXCLK following the final nibble of a frame.

When operating in half duplex mode, the ELAN-EPHY device asserts COL upon detection of a collision on the medium. The ELAN-EPHY device ensures COL remains asserted while the collision condition persists. The ELAN-EPHY device is not responsible for transmitting JAM signals during a collision condition, but continues to transmit the data provided on TXD[3:0]. It is the responsibility of the MAC layer to provide JAM signals on TXD[3:0]. The ELAN-EPHY device negates COL when the collision condition no longer exists. When operating in full duplex mode, collisions cannot occur and COL always remains low.

The ELAN-EPHY device ensures that CRS remains asserted throughout the duration of a collision condition. Otherwise, CRS behaves as indicated in figure 13.1 (previous figure).

Fig. 13.3 Transmission of an Error on Medium Independent Interface

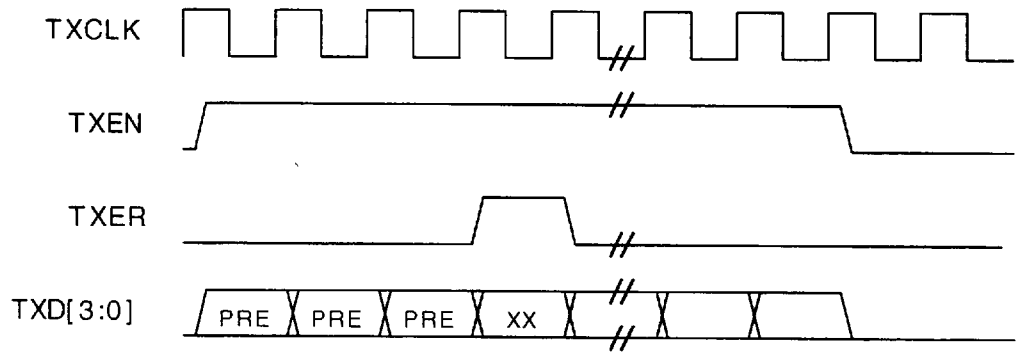


Figure 13.3 illustrates transmission of an error on the Transmit (Tx) Medium Independent Interface (MII) of the ELAN-EPHY device. The ELAN-EPHY device recognizes the data on TXD[3:0] as valid on every rising edge of TXCLK that TXEN is sampled high and TXER is sampled low. TXEN is asserted with the first nibble of the preamble and shall remain asserted while all nibbles to be transmitted are presented to the ELAN-EPHY device. TXEN is negated prior to the first rising edge of TXCLK following the final nibble of a frame.

The ELAN-EPHY device ignores the data on TXD[3:0] on every rising edge of TXCLK that TXEN and TXER are sampled high. In this case, the ELAN-EPHY device transmits the H invalid code word on the medium. TXER may be asserted at any time during data transfer on the Tx MII. The assertion of TXER does not affect data transmission when the ELAN-EPHY device is operating at 10 Mbps, or when TXEN is negated.

Fig. 13.4 Reception on Medium Independent Interface without errors

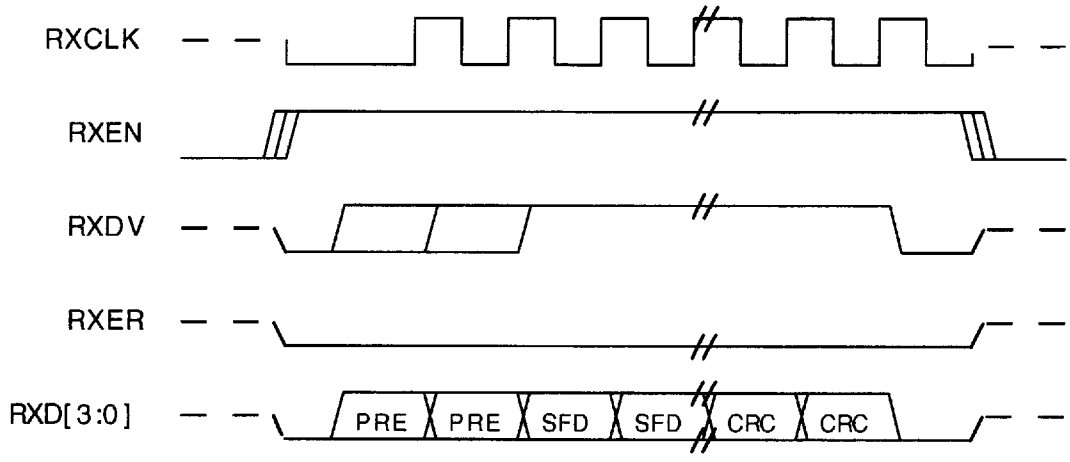


Figure 13.4 illustrates data transfer on the Receive (Rx) Medium Independent Interface (MII) of the ELAN-EPHY device. The RXEN synchronization option is selected in this example. RXDV is asserted by the ELAN-EPHY device to indicate that recovered and decoded nibbles are being presented on RXD[3:0]. RXDV is asserted no later than the Start of Frame Delimiter (SFD). RXDV remains asserted continuously from the first recovered nibble of a frame to the final recovered nibble, and is negated following the final recovered nibble excluding any End of Frame Delimiter (EFD).

RXEN must remain high during data reception to allow the ELAN-EPHY device to drive the RXDV, RXER and RXD[3:0] signals. Setting RXEN low tri-states these signals. RXCLK can be driven low for one cycle before it is allowed to transition.

The ELAN-EPHY device drives RXER low to indicate that no errors are detected in the frame presently being received.

Fig. 13.5 Reception on Medium Independent Interface with errors

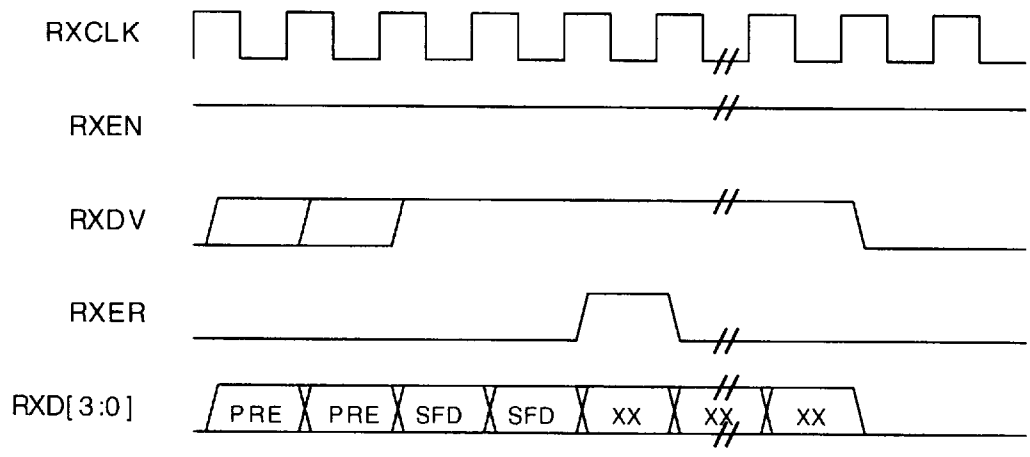


Figure 13.5 illustrates data transfer with errors on the Receive (Rx) Medium Independent Interface (MII) of the ELAN-EPHY device. RXDV is asserted by the ELAN-EPHY device to indicate that recovered and decoded nibbles are being presented on RXD[3:0]. RXDV is asserted no later than the Start of Frame Delimiter (SFD) and remains asserted continuously until the final recovered nibble. RXDV is negated following the final recovered nibble excluding any End of Frame Delimiter (EFD).

RXEN must remain high during data reception to allow the ELAN-EPHY device to drive the RXCLK, RXDV, RXER and RXD[3:0] signals. Setting RXEN low tri-states these signals.

The ELAN-EPHY device drives RXER and RXDV high to indicate that the nibble present on RXD[3:0] is in error.

Fig. 13.6 False Carrier Indication

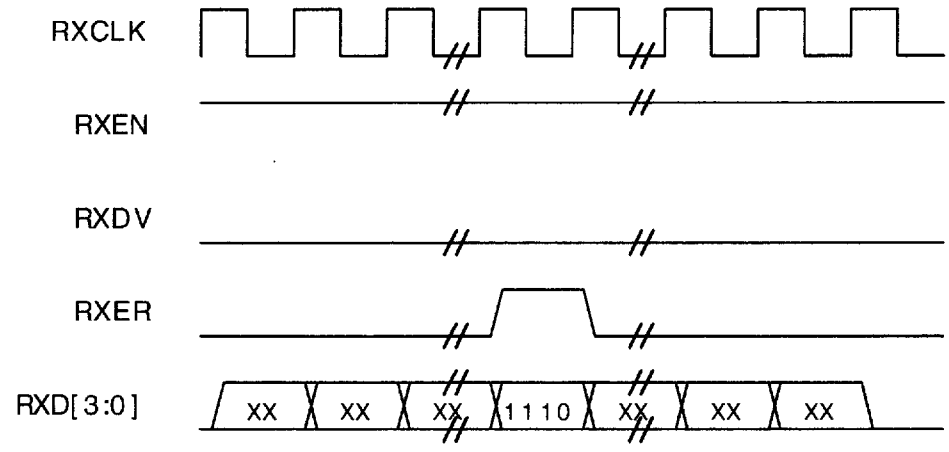


Figure 13.6 illustrates a false carrier indication on the Receive (Rx) Medium Independent Interface (MII) of the ELAN-EPHY device. The ELAN-EPHY device indicates a false carrier condition by asserting RXER while driving RXD[3:0] with "1110". The ELAN-EPHY device holds RXDV low during a false carrier indication condition.

RXEN must remain high during a false carrier indication to allow the ELAN-EPHY device to drive the RXDV, RXER and RXD[3:0] signals. Setting RXEN low tri-states these signals.

Fig. 13.7 Collision Test in Loopback Mode

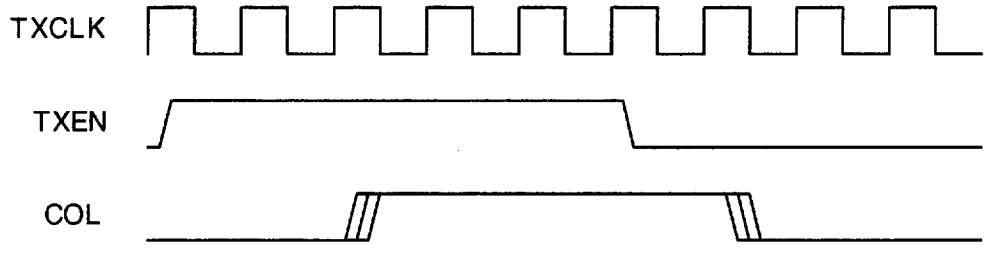


Figure 13.7 illustrates the behavior of COL when collision testing in loopback mode. The ELAN-EPHY device asserts COL in response to the assertion of TXEN. The ELAN-EPHY device negates COL in response to the negation of TXEN. COL has no timing relationship to TXCLK.

COL remains low in loopback mode if collision testing is disabled. It is recommended that collision testing only be enabled when in loopback mode.

Fig. 13.8 Transmit Symbol Interface (Repeater Mode)

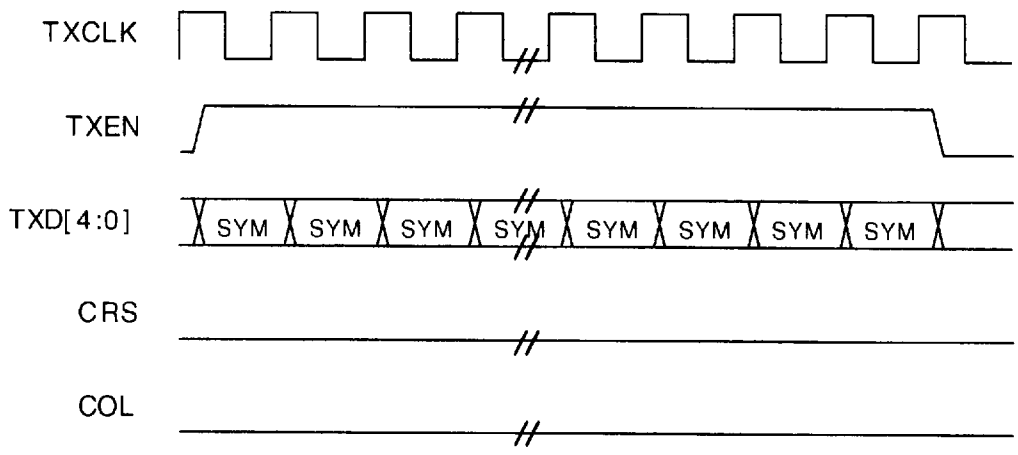


Figure 13.8 illustrates data transfer on the Transmit (Tx) Symbol Interface of the PHY. Since the ELAN-EPHY continuously sinks data it samples TXD[4:0] on every rising edge of TXCLK. TXEN is high during the transmission of valid code groups on the symbol interface. When TXEN is low, the ELAN-EPHY forces the transmission of IDLE code groups.

When operating with the symbol interface in repeater mode, the ELAN-EPHY will not assert CRS for data transmission. CRS will only be asserted for the reception of data. In addition the COL signal will remain low and it will be the responsibility of the repeater controller to detect collisions.

Fig. 13.9 Receive Symbol Interface (Repeater Mode)

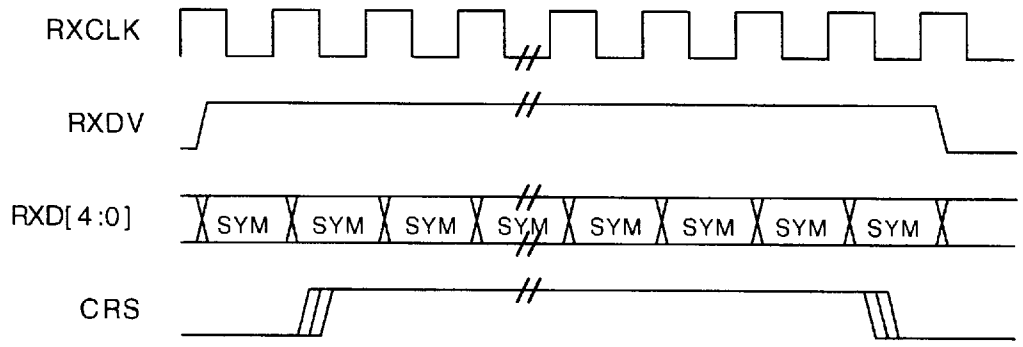


Figure 13.9 illustrates data transfer on the Receive (Rx) Symbol Interface of the PHY. Since the ELAN-EPHY will continuously source data, RXD[4:0] will be updated on every RXCLK cycle. RXDV is high to indicate the receipt of a valid frame on the symbol interface.

When operating with the symbol interface in repeater mode, the CRS signal will be asserted by the ELAN-EPHY on the reception of data to indicate activity on the receive medium.

Fig. 13.10 FLP Bursts and NLPs

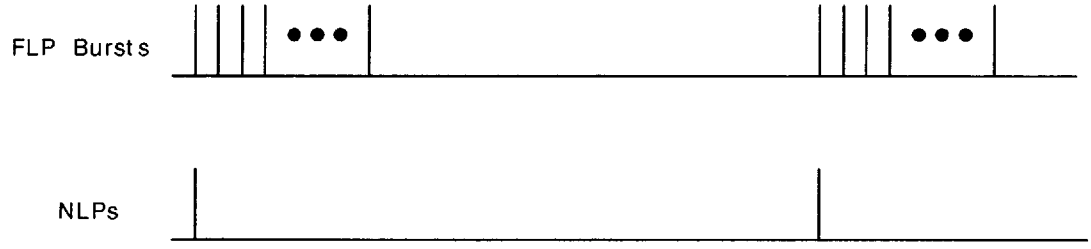


Figure 13.10 illustrates FLP bursts and NLPs. FLP burst builds upon the link pulse mechanism (NLPs) employed by 10Base-T to detect the status of the link. FLP bursts are substituted the in place of the single 10Base-T link integrity test pulse within the Normal Link Pulse sequence.

Fig. 13.11 FLP clock pulses and data pulses

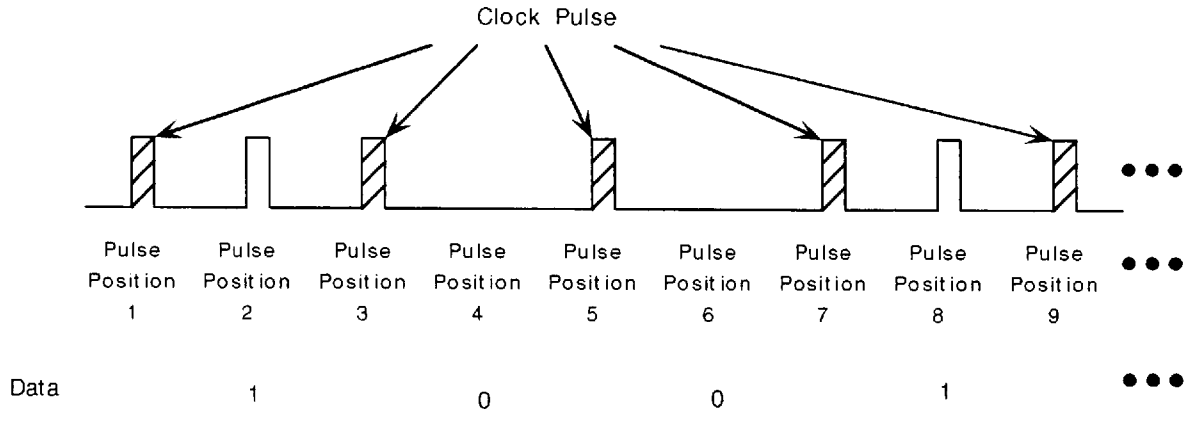


Figure 13.11 illustrates clock and data pulses within a FLP burst. The FLP Burst encodes the data that is used to control the Auto-Negotiation function in following way. A FLP burst consists of 33 pulse positions. The 17 odd-numbered pulse positions contain a link pulse and represent clock information. The 16 even-numbered pulse positions contain data and represent 1 if a pulse presents and 0 if a pulse is absent at the position.

13.2. SMI Interface

Fig. 13.12 Serial Management Interface Write Cycle

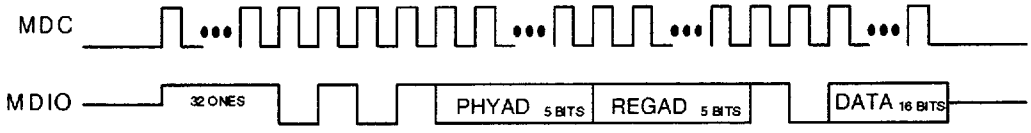


Figure 13.12 illustrates a write cycle on the serial management interface of the ELAN-EPHY device. The ELAN-EPHY device observes a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC before it responds to any transaction. Once the ELAN-EPHY device has established synchronization using the 32 logic one bit pattern, a 2 bit "01" start of frame pattern assures transition from the default logic one line state to zero and back to one. The following "01" pattern is interpreted by the ELAN-EPHY device as a write transaction. If the 5 bit PHYAD field matches that of the ELAN-EPHY device, the ELAN-EPHY device responds to the write transaction by writing the 16 bit data field into the register addressed by the 5 bit REGAD field. A single pulse MDC turn-around cycle is required at the end of each transaction.

Fig. 13.13 Serial Management Interface Read Cycle

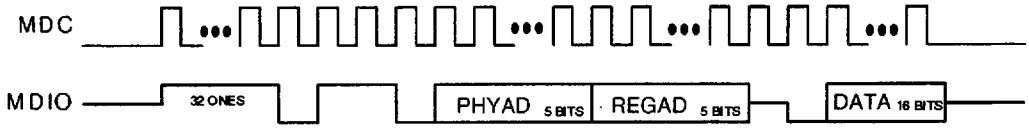
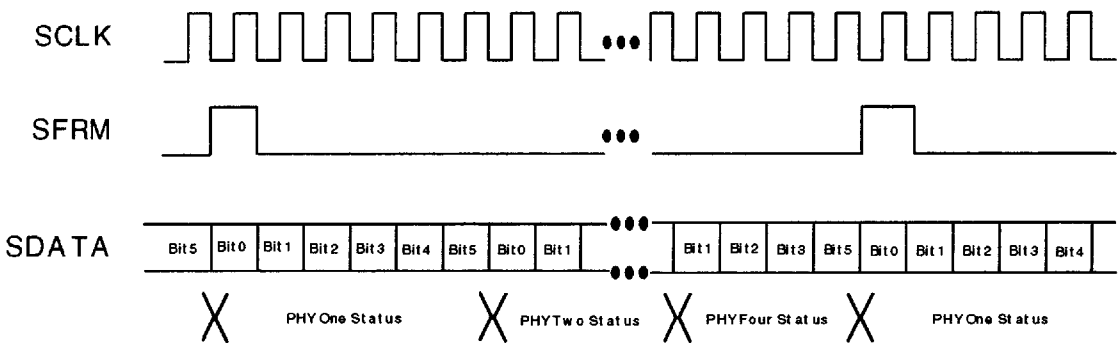


Figure 13.13 illustrates a read cycle on the serial management interface of the ELAN-EPHY device. The ELAN-EPHY device observes a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC before it responds to any transaction. Once the ELAN-EPHY device has established synchronization using the 32 logic one bit pattern, a 2 bit "01" start of frame pattern assures transition from the default logic one line state to zero and back to one. The following "10" pattern is interpreted by the ELAN-EPHY device as a read transaction. If the 5 bit PHYAD field matches that of the ELAN-EPHY device, the ELAN-EPHY device responds to the read transaction by providing the 16 bit register data addressed by the 5 bit REGAD field onto MDIO. A turn-around cycle is required following the REGAD field where the station management entity does not drive MDIO, after which the ELAN-EPHY device drives a logic zero and the 16 bit read

data onto MDIO. A single pulse MDC turn-around cycle is required at the end of each transaction.

13.3. SSI Interface

Fig. 13.14 Serial Status Interface (SMODE = 000)

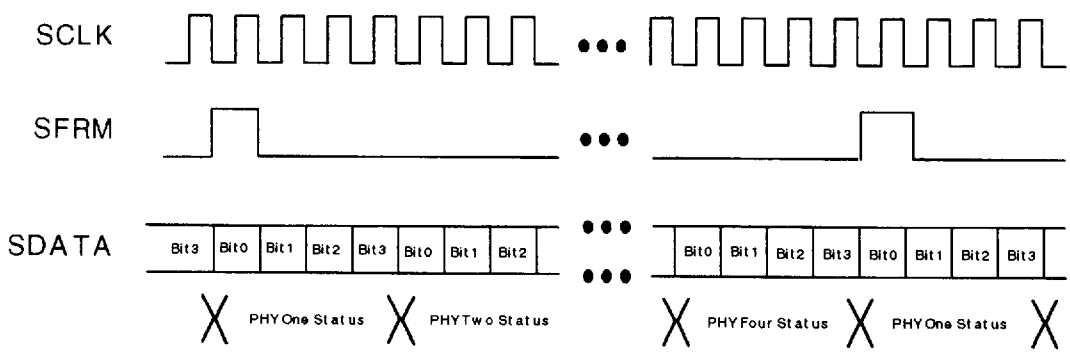


The Serial Status Interface (SSI) serializes each PHYs status information and shifts it out for use by external controllers or LED drivers. The SSI shifts out a frame of data consisting of each PHYs enabled status bits. Status bit 0 of PHY 1 is shifted out first and status bit 5 of PHY 4 is shifted out last. After the frame has been shifted out the SFRM signal is pulsed to indicate the end of the current frame. As defined in the Extended PHY Control Two register, each status bit can be disabled and thus not shifted out by the SSI. In addition, the polarity for each status bit can also be programmed.

In the example above for PMC status mode (SMODE=000) Bit0 corresponds to the RXA status and Bit5 corresponds to the DPL status in the Extended PHY Control Two register. For PHY four the RXA_EN and SPD_EN bits are set low. Thus, those status bits are dropped and the status word for that PHY is only four bits. The RXA, TXA, COL and LNK status indications have been stretched to give a minimum pulse of 100 ms. This ensures that the LEDs are visible when driven via these indications. SPD and DPL are not stretched since they do not change after the PHY is configured.

The first frame shifted out on the SSI after power up or reset will be invalid and should be ignored. In addition, if the status enable register bits are changed, the current frame and the following frame shifted out on the SSI may be invalid and should be ignored.

Fig. 13.15 Serial Status Interface (SMODE = 001)



In the example above for Vendor Specific status mode (SMODE=001), there are four status bits in each status word for each PHY. The four status bits are always enabled and depend on the 5 control signals in the extended PHY control 2 register as well as the PHYs status. Bit0 corresponds to the RX_GRN status and Bit3 corresponds to the TX_RED status in Extended PHY Control Two register. Again, status bit 0 of PHY 1 is shifted out first and status bit 3 of PHY 4 is shifted out last. The RX_GRN, RX_RED, TX_GRN and TX_RED status indications have been stretched to give a minimum pulse of 100 ms. This ensures that when LEDs are driven via these indications that they will be visible. In addition, the polarity for each status bit can be programmed.

The status indications shifted out on the SSI are invalid until SMODE[2:0] = 001 in all four PHYs.

14. ABSOLUTE MAXIMUM RATINGS

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal operating conditions.

Ambient Temperature under Bias	0°C to +70°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to V_{DD}+0.5V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+300°C
Absolute Maximum Junction Temperature	+150°C

15. D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{DD} = 5 V ±5%

(Typical Conditions: T_A = +25°C, V_{DD} = 5 V)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power Supply	4.75	5	5.25	Volts	Note 5.
V_{IL} (TTL)	Input Low Voltage	-0.5		0.8	Volts	Guaranteed Input LOW Voltage for TTL inputs.
V_{IL} (CMOS)	Input Low Voltage	-0.5		0.3* V_{DD}	Volts	Guaranteed Input LOW Voltage for CMOS inputs.
V_{IH} (TTL)	Input High Voltage	2.0		V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage for TTL inputs.
V_{IH} (CMOS)	Input High Voltage	0.7* V_{DD}		V_{DD}	Volts	Guaranteed Input HIGH Voltage for CMOS inputs.
V_{OL}	Output or Bidirectional Low Voltage		0.1	0.4	Volts	I_{OL} = -4 mA for all outputs. Notes 3, 5.
V_{OH}	Output or Bidirectional High Voltage	V_{DD} - 1.0	4.7		Volts	I_{OH} = 4 mA for all outputs. Notes 3, 5.
V_{T+}	Reset Input High Voltage	3.5			Volts	
V_{T-}	Reset Input Low Voltage			0.6	Volts	
V_{TH}	Reset Input Hysteresis Voltage		0.6		Volts	Note 5.
I_{ILPU}	Input Low Current	175	250	525	uA	V_{IL} = GND, Notes 1, 3, 5.
I_{IHPU}	Input High Current	-10	0	+10	uA	V_{IH} = V_{DD}, Notes 1, 3

I_{IL}	Input Low Current	-10	0	+10	uA	V_{IL} = GND, Notes 2, 3
I_{IH}	Input High Current	-10	0	+10	uA	$V_{IH} = V_{DD}$, Notes 2, 3
C_{IN}	Input Capacitance		5		pF	Excludes package. Package Typically 2 pF. Note 5.
C_{OUT}	Output Capacitance		5		pF	All pins. Excludes package. Package Typically 2 pF. Note 5.
C_{IO}	Bidirectional Capacitance		5		pF	All pins. Excludes package. Package Typically 2 pF. Note 5.
I_{DDOP}	Operating Current.			345	mA	MDI Interface Loaded Passing Data, Digital Outputs Unloaded.

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistor.
2. Input pin or bidirectional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. Typical values are given as a design aid. The product is not tested to the typical values given in the data sheet.
5. Typical values are not production tested.

16. A.C. TIMING CHARACTERISTICS

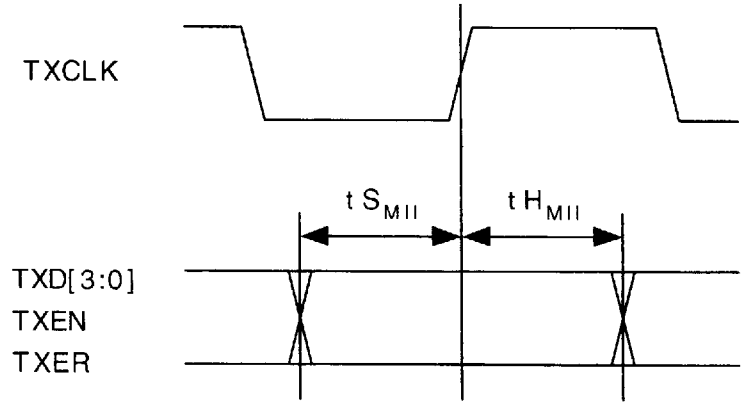
Medium Independent Interface

(T_A = -0°C to +70°C, V_{DD} = 5 V ±5%)

Transmit MII (Fig. 16.1)

Symbol	Description	Min	Max	Units
	TXCLK Frequency (100 MHz)		25	MHz
	TXCLK Frequency (10 MHz)		2.5	MHz
	TXCLK Duty Cycle	40	60	%
tS_{MII}	Setup time to TXCLK; TXD[3:0], TXEN, TXER	10		ns
tH_{MII}	Hold time to TXCLK; TXD[3:0], TXEN, TXER	0		ns

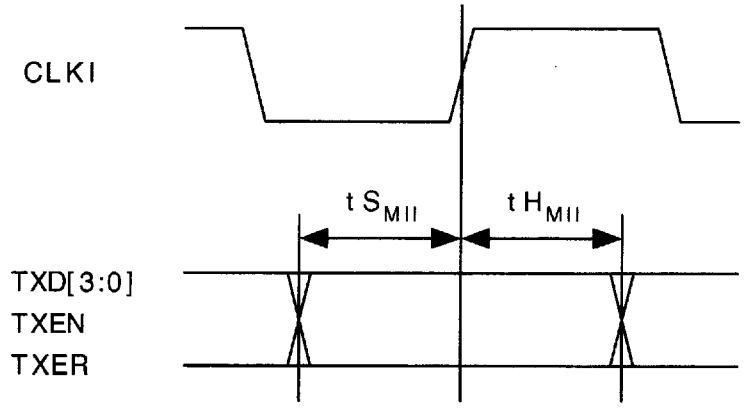
Fig. 16.1 Transmit MII Timing



Transmit MII (Repeater Applications, 100 Mbps only) (Fig. 16.2)

Symbol	Description	Min	Max	Units
	CLKI Frequency (100 MHz)		25	MHz
	CLKI Duty Cycle	40	60	%
tS_{MII}	Setup time to CLKI; TXD[3:0], TXEN, TXER	10		ns
tH_{MII}	Hold time to CLKI; TXD[3:0], TXEN, TXER	0		ns

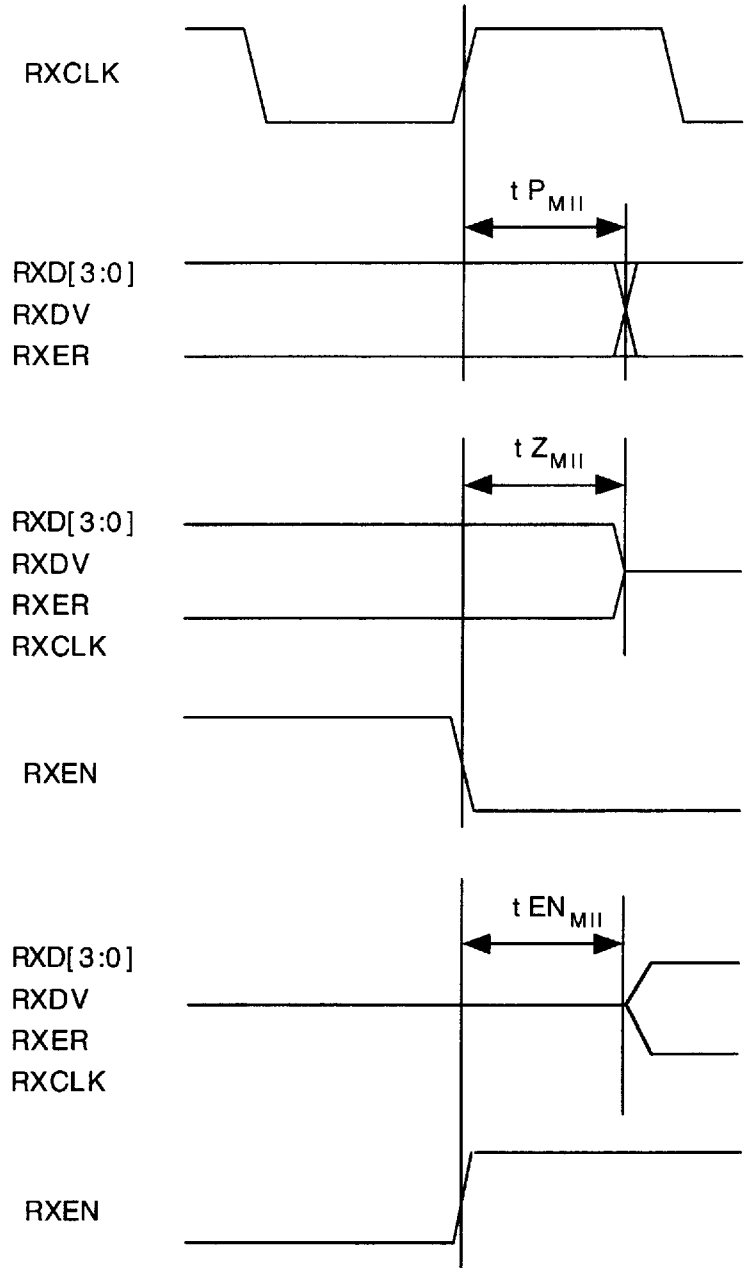
Fig. 16.2 Transmit MII Timing (Repeater Applications, 100 Mbps only)



Receive MII (Fig. 16.3)

Symbol	Description	Min	Max	Units
	RXCLK Frequency (100 MHz)		25	MHz
	RXCLK Frequency (10 MHz)		2.5	MHz
	RXCLK Duty Cycle	40	60	%
tP_{MII}	RXCLK to Output Valid; RXD[3:0], RXDV, RXER	1	25	ns
tZ_{MII}	RXEN Falling Edge to Output Tristate (RXEN_SYNC=0); RXD[3:0], RXDV, RXER, RXCLK	1	15	ns
tZ_{MII}	RXEN Falling Edge to Output Tristate (RXEN_SYNC=1); RXD[3:0], RXDV, RXER, RXCLK	0.5	1.5	RXCLK Cycle
tEN_{MII}	RXEN Rising Edge to Output Enabled (RXEN_SYNC=0); RXD[3:0], RXDV, RXER, RXCLK	0	15	ns
tEN_{MII}	RXEN Rising Edge to Output Enabled (RXEN_SYNC=1); RXD[3:0], RXDV, RXER, RXCLK	0.5	1.5	RXCLK Cycle

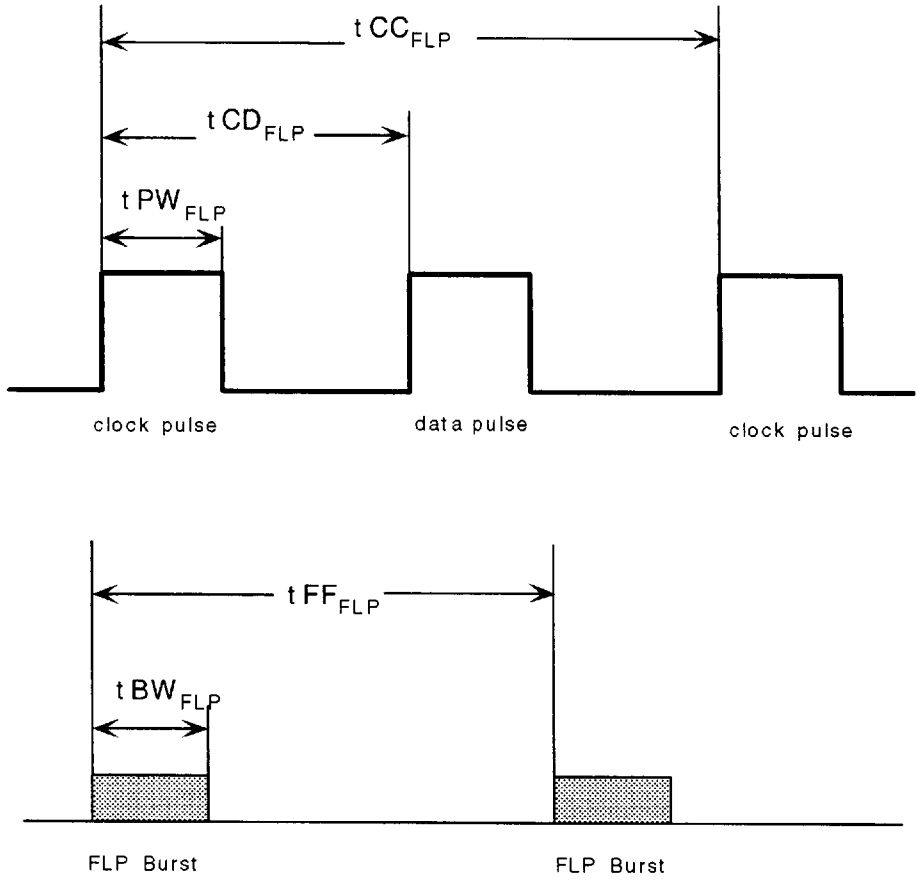
Fig. 16.3 Receive MII Timing



Auto-negotiation Timing (Fig. 16.4)

Symbol	Description	Min	Max	Units
tPW_{FLP}	FLP Pulse width	100		ns
tCD_{FLP}	FLP clock pulse to FLP data pulse	55.5	69.5	us
tCC_{FLP}	FLP clock pulse to FLP clock pulse	111	139	us
tBW_{FLP}	FLP Burst width		2	ms
tFF_{FLP}	FLP burst to FLP burst	8	24	ms

Fig. 16.4 Auto-negotiation Timing

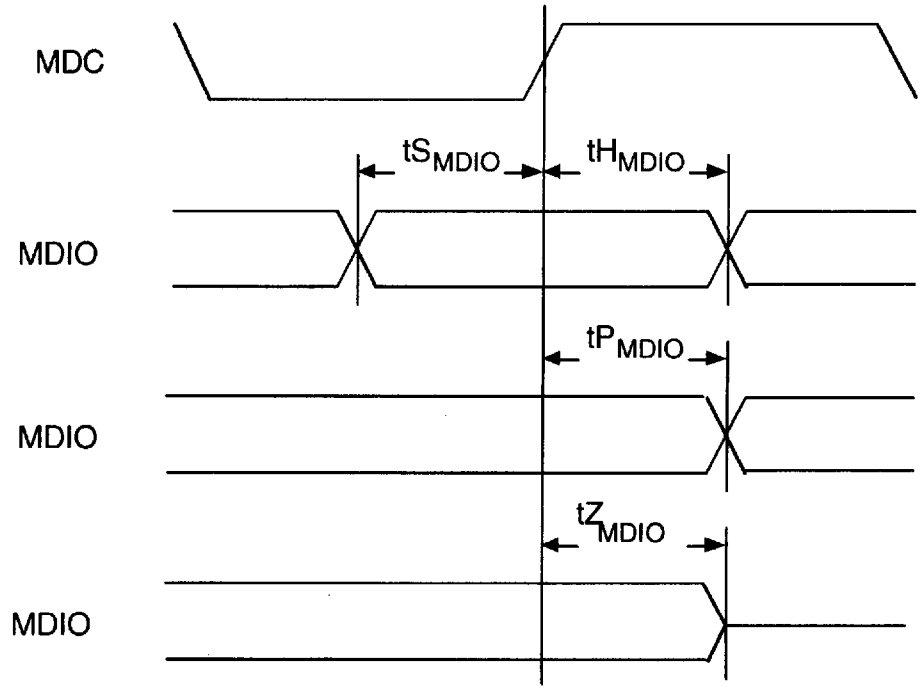


Configuration / Monitor Signals

Serial Management Interface Timing (Fig. 16.5)

Symbol	Description	Min	Max	Units
	MDC Frequency		25	MHz
	MDC High/Low Time	16		ns
tS_{MDIO}	MDIO Set-up to MDC Rising	10		ns
tH_{MDIO}	MDIO Hold to MDC Rising	1		ns
tP_{MDIO}	MDC Rising to MDIO Valid	1	25	ns
tZ_{MDIO}	MDC Rising to MDIO tri-stated	1	25	ns

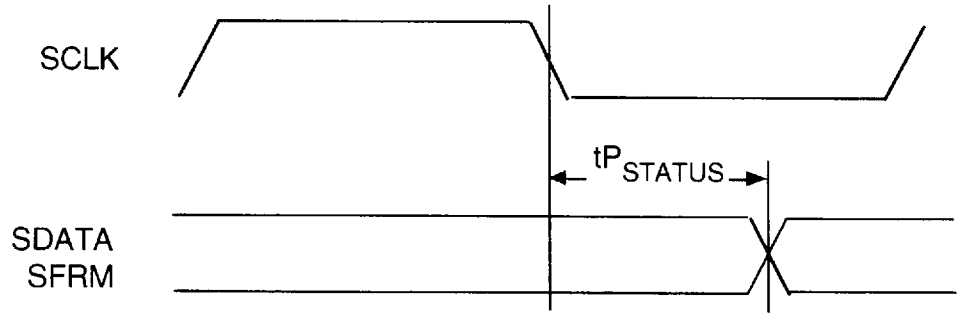
Fig. 16.5 Serial Management Interface Timing



Serial Status Interface Timing (Fig. 16.6)

Symbol	Description	Min	Max	Units
	SCLK Frequency		1	MHz
	SCLK Duty Cycle	40	60	%
tP_{STATUS}	SCLK to Output Valid; SDATA, SFRM	-5	+5	ns

Fig. 16.6 Serial Status Interface Timing

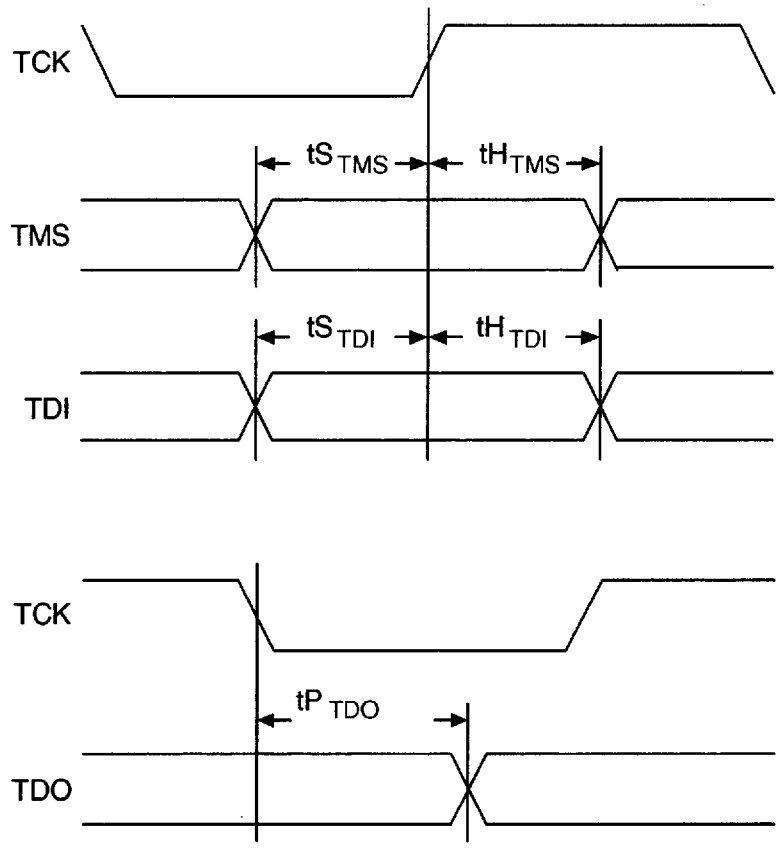


Miscellaneous Interface Signals

JTAG Port Interface (Fig. 16.7)

Symbol	Description	Min	Max	Units
	TCK Frequency		1	MHz
	TCK Duty Cycle	40	60	%
tS_{TMS}	TMS Set-up time to TCK	50		ns
tH_{TMS}	TMS Hold time to TCK	50		ns
tS_{TDI}	TDI Set-up time to TCK	50		ns
tH_{TDI}	TDI Hold time to TCK	50		ns
tP_{TDO}	TCK Low to TDO Valid	2	50	ns

Fig. 16.7 JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum and minimum output propagation delays are measured with a 30 pF load on all the outputs, except for the MDIO output. The MDIO output propagation delay is measured with a 50 pF load on the output.

3. Output tri-state delay is the time in nanoseconds from the 1.4 Volt point of the reference signal to ±300 mV of the termination voltage on the output. The test load is 50Ω to 1.4V in parallel with 10 pF to GND.

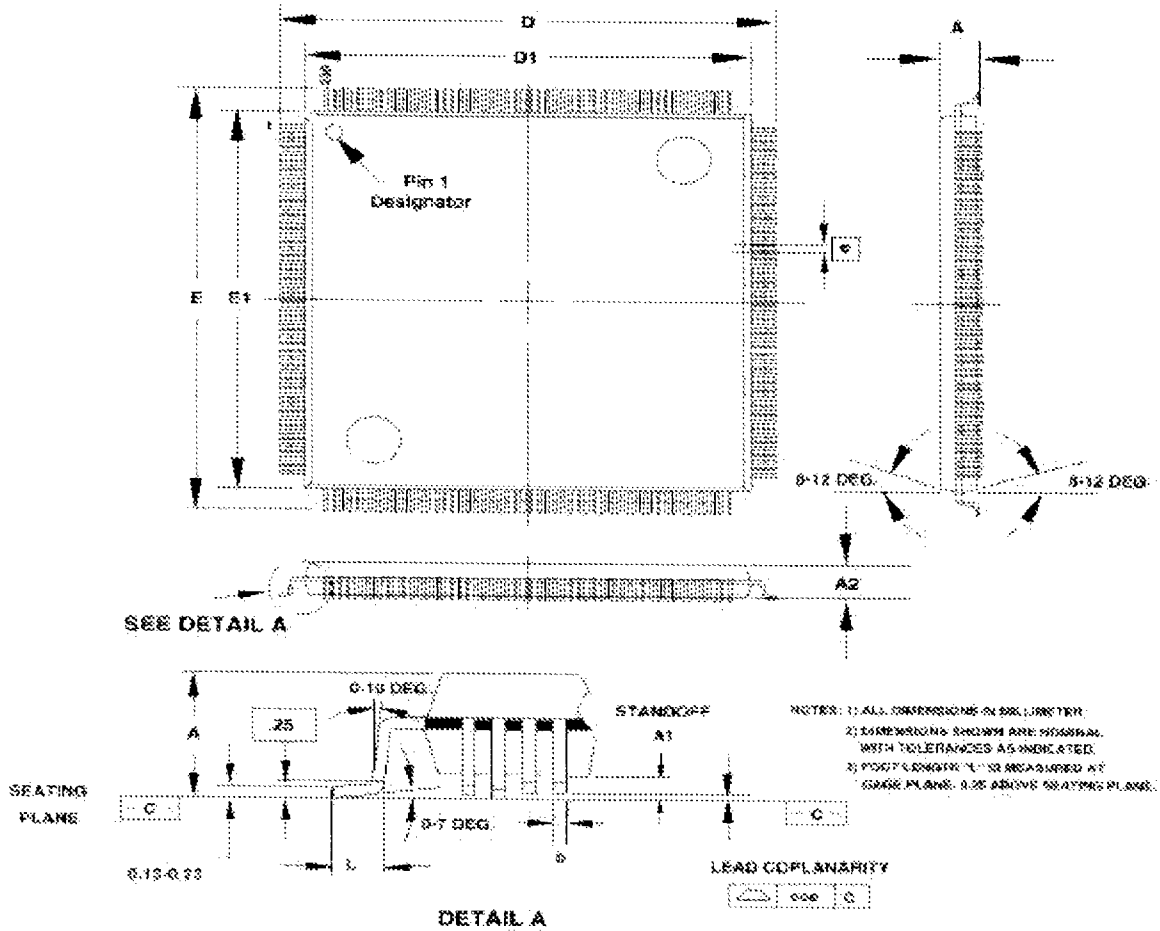
17. ORDERING AND THERMAL INFORMATION

PART NO.	DESCRIPTION
PM3304-RC	208 Plastic Quad Flat Pack (PQFP)

PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM3304-RC	0°C to 70°C	26 °C/W	15 °C/W

18. MECHANICAL INFORMATION

Fig. 18.1 208 Pin Plastic Quad Flat Pack



PACKAGE TYPE: 208 PIN METRIC PLASTIC QUAD FLATPACK MQFP											
BODY SIZE: 28 x 28 x 3.49 MM											
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc
Min.	3.64	0.25	3.38	30.45	27.90	30.45	27.90	0.55		0.17	
Nom.			3.49	30.60	28.00	30.60	28.00	0.60	0.50	0.22	
Max.	4.07	0.48	3.59	30.65	28.10	30.80	28.10	0.75		0.27	0.10