XLAS076 – MAY 1995

- CMOS Technology
- Versatile Multiplexing Interface Allows Lower Pixel Bus Rate
- High Level of Integration Provides Lower System Cost and Complexity
- Direct VGA Pass-Through Capability
- Versatile Pixel Bus Interface Supports Little- and Big-Endian Data Formats
- True-Color (Direct Addressing) Modes Support Various 24- and 16-Bit Formats
- XGA™-Format Compatible (5–6–5)
- TARGA™-Format Compatible (5–5–5)
- Directly Interfaces to TMS34010/TMS34020 and Other Graphics Processors
- Triple 8-Bit D/A Converters
- 85-, 110-, 135-, and 170- MHz Versions
- 256-Word Color Palette RAM
- Palette Page Register
- On-Chip Voltage Reference
- RS-343A-Compatible Outputs
- TTL-Compatible Inputs
- Standard MPU Interface
- Pixel Word Mask
- On-Chip Clock Selection
- Directly Interfaces to Video RAM
- Supports Split Shift-Register Transfers
- Software Downward-Compatible With INMOS IMSG176/8 and Brooktree™ BT476/8 Color Palettes
- TIGA™ Software-Standard Compatible
- Data Manual Available†

description

The TLC34076 video interface palette (VIP) is designed to provide lower system cost with a higher level of integration. The device incorporates all of the high-speed timing, synchronization, and multiplexing logic usually associated with graphics systems into one device, thus greatly reducing chip count. Since all high-speed signals (excluding the clock source) are contained on-chip, RF noise considerations are simplified. Maximum flexibility is provided through the pixel multiplexing scheme, which allows for 32-, 16-, 8-, and 4-bit pixel buses to be accommodated without any circuit modification. This enables the system to be easily reconfigured for varying amounts of available video RAM. Data can be split into 1-, 2-, 4-, or 8-bit planes. The TLC34076 is software-compatible with the IMSG176/8 and Brooktree BT476/8 color palettes.

The TLC34076 VIP is terminal-for-terminal compatible with the TLC34075 VIP but contains additional 24- and 16-bit true-color modes as well as the ability to select little- or big-endian data formats for the pixel bus frame-buffer interface.

The TLC34076 features a separate video graphics adapter (VGA) bus that allows data from the feature connector of most VGA-supported personal computers to be fed directly into the palette without the need for external data multiplexing. This allows a replacement graphics board to remain downward compatible by utilizing the existing graphics circuitry often located on the motherboard.

The 24- and 16-bit true-color modes that are provided allow bits of color information to be transferred directly from the pixel port to the digital-to-analog converters (DACs). Depending on which true-color mode is selected, an overlay function is provided using the remaining bits of the pixel bus. The 24-bit modes allow overlay with the eight remaining bits of the pixel bus, while the TARGA (5-5-5) 16-bit mode allows overlay with the one remaining bit of the divided pixel bus.

The TLC34076 has a 256-by-24 color-lookup table with triple, 8-bit video, D/A converters capable of directly driving a doubly terminated, 75-Ω line. Synchronization generation is incorporated on the green output channel. $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are fed through the device and optionally inverted to indicate screen resolution to the monitor. A palette page register provides the additional bits of palette address when 1-, 2-, or 4-bit planes are used. This allows the screen colors to be changed with only one MPU write cycle.

† For the complete data manual, refer to the Graphics and Imaging Data Book (SLAD002).

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TARGA is a trademark of Truevision Incorporated.
Brooktree is a trademark of Brooktree Corporation.
TIGA is a trademark of Texas Instruments Incorporated.

description (continued)

Clocking is provided through one of four or five inputs (three TTL- and either one ECL- or two TTL-compatible) and is software selectable. The video and shift-clock outputs provide a software-selected divide ratio of the chosen clock input.

The TLC34076 can be connected directly to the serial port of VRAM devices, eliminating the need for any discrete logic. Support for split shift-register transfers is also provided.

AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE	
			PLASTIC CHIP CARRIER (FN)	GRID ARRAY (GA)
0°C to 70°C	85 MHz	8 Bits	TLC34076-85FN	–
	110 MHz	8 Bits	TLC34076-110FN	–
	135 MHz	8 Bits	TLC34076-135FN	–
	170 MHz	8 Bits	TLC34076-170FN	–
–55°C to 125°C	135 MHz	8 Bits	–	TLC34076-135MGA

function block diagram

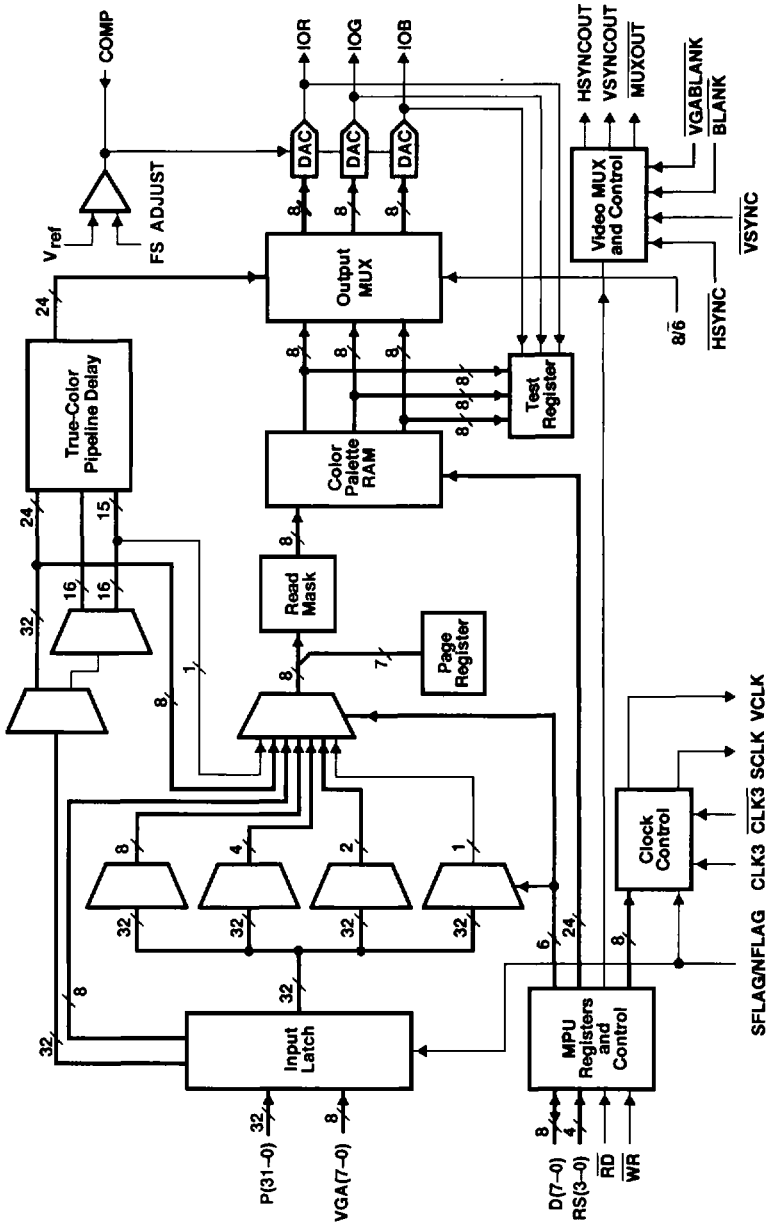

Figure 1. Functional Block Diagram