HM514101 Series

4,194,304-Word x 1-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514101 is a CMOS dynamic RAM organized 4,194,304 word x 1-bit. HM514101 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514101 offers Nibble Mode as a high speed access mode.

Multiplexed address input permits the HM514101 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time ..... 80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode ..... 495 mW/440 mW/385 mW (max)
  - Standby Mode ..... 11 mW (max)
- Nibble Mode Capability
- 1,024 Refresh Cycles ..... (16 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Test Function

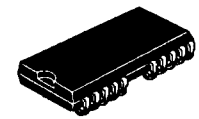
■ ORDERING INFORMATION

Part No.	Access Time	Package
HM514101JP-8	80 ns	350 mil 20-pin
HM514101JP-10	100 ns	Plastic SOJ
HM514101JP-12	120 ns	(CP-20DA)
HM514101ZP-8	80 ns	400 mil 20-pin
HM514101ZP-10	100 ns	Plastic ZIP
HM514101ZP-12	120 ns	(ZP-20)

■ PIN DESCRIPTION

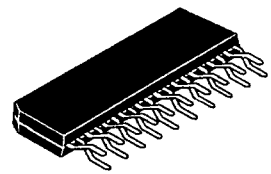
Pin Name	Function
A_0–A_{10}	Address Input
A_0–A_9	Refresh Address Input
D_{in}	Data-in
D_{out}	Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power (+ 5V)
V_{SS}	Ground

HM514101JP Series



(CP-20DA)

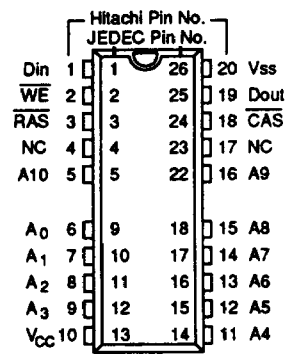
HM514101ZP Series



(ZP-20)

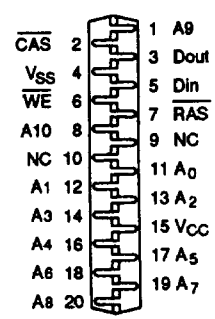
■ PIN OUT

HM514101JP Series



(Top View)

HM514101ZP Series



(Bottom View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	− 2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	80	—	70	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	90	—	80	—	70	mA	t_{RC} = Min	
Nibble Mode Current	I_{CC8}	—	90	—	80	—	70	mA	t_{NC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• Capacitance (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address, Data-in)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-out)	C_O	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 12, 13]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 14
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5, 14
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	ns	6

Write Cycle

Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	20	—	25	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	180	—	210	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	100	—	120	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	25	—	25	—	30	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	—	45	—	55	—	ns	10

Refresh Cycle

Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

Nibble Mode Cycle

Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Nibble Mode Access Time	t_{NAC}	—	25	—	25	—	30	ns	
Nibble Mode Cycle Time	t_{NC}	45	—	45	—	55	—	ns	
Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	10	—	10	—	15	—	ns	
Nibble Mode $\overline{CAS}$ Pulse Width	t_{NCA}	25	—	25	—	30	—	ns	
Nibble Mode $\overline{RAS}$ Hold Time	t_{NRSH}	25	—	25	—	30	—	ns	

Nibble Mode Read-Modify-Write Cycle

Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Nibble Mode Read-Modify-Write Cycle Time	t_{NRWC}	75	—	75	—	90	—	ns	
Nibble Mode Write Command to $\overline{CAS}$ Lead Time	t_{NCWL}	25	—	25	—	30	—	ns	
Nibble Mode $\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{NCWD}	25	—	25	—	30	—	ns	

Test Mode Cycle

Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	20	—	20	—	20	—	ns	

Counter Test Cycle

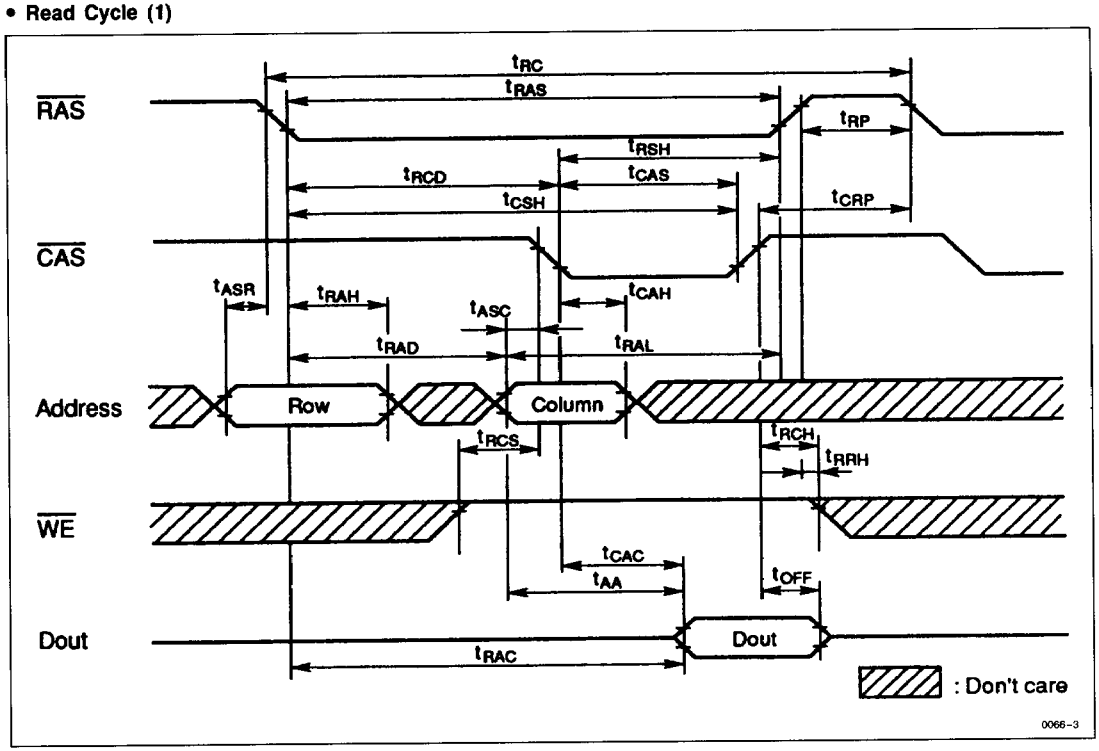
Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	50	—	60	—	ns	

Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RCD} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

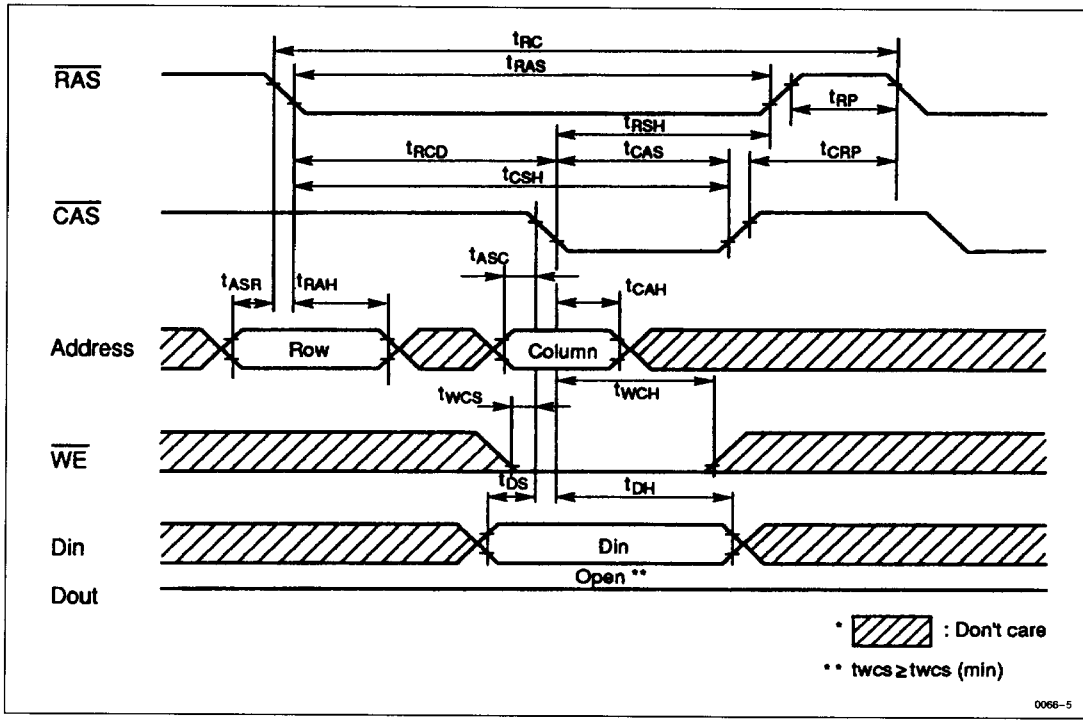
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
13. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits—RA10, CA10 and CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is D_{out} and data input pin is D_{in}. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
14. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{NAC} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

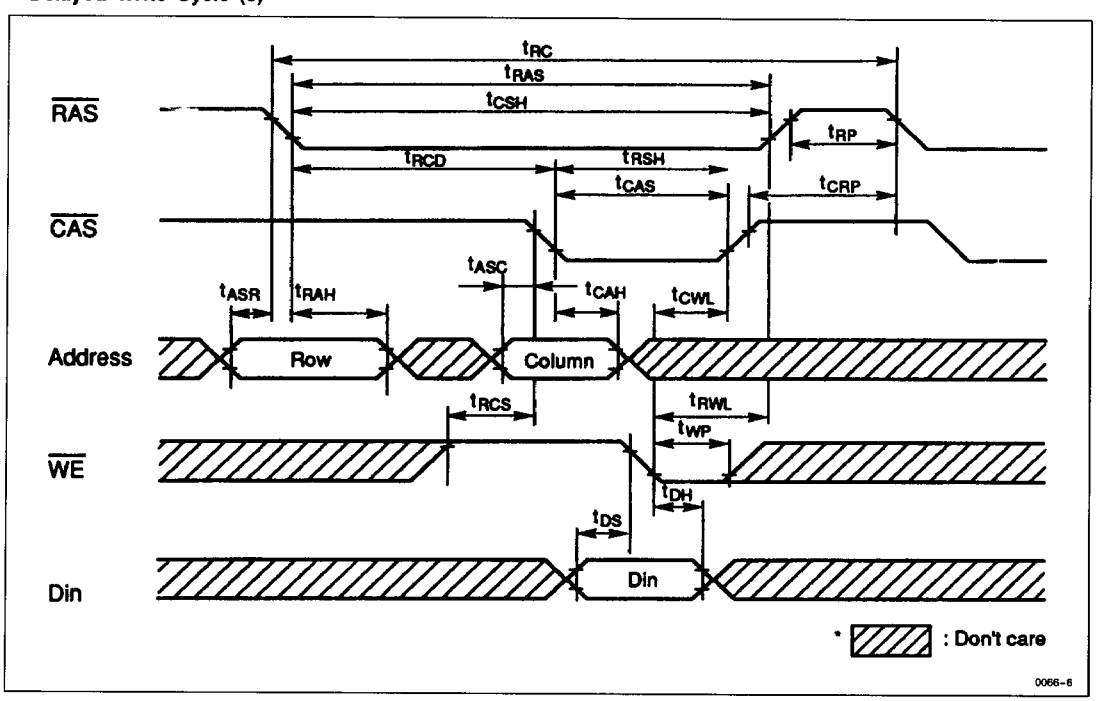
• Read Cycle (1)



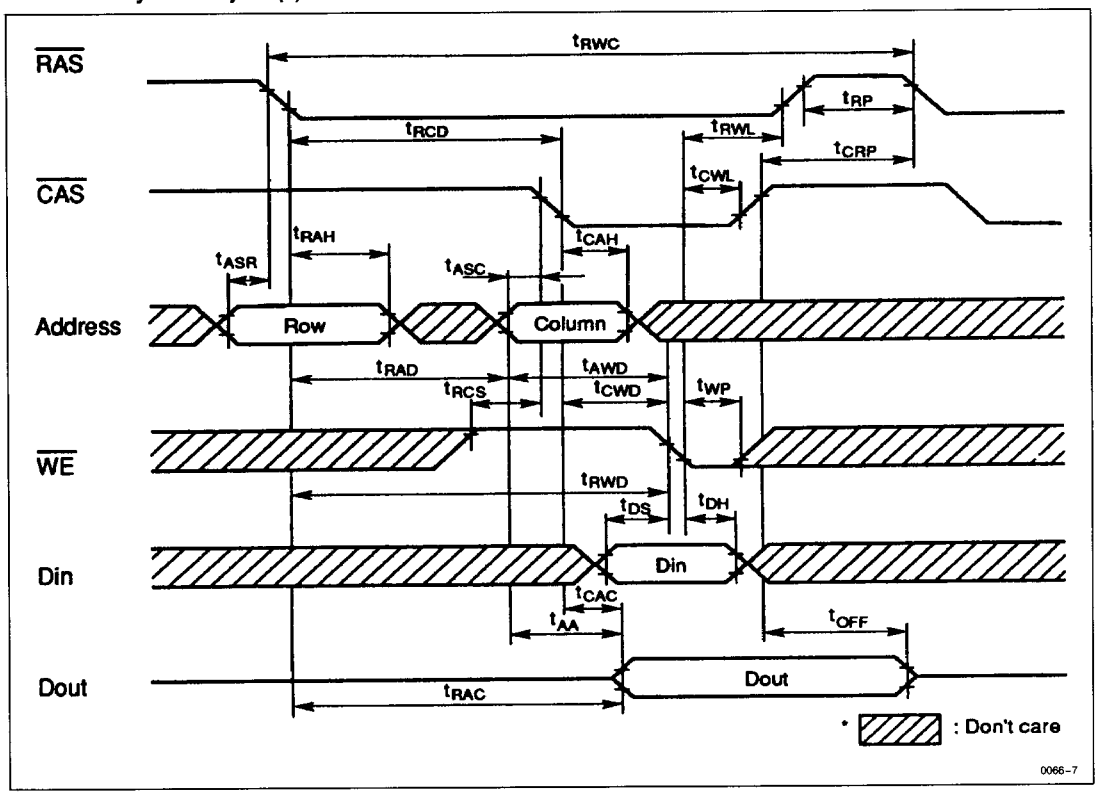
• Early Write Cycle (2)



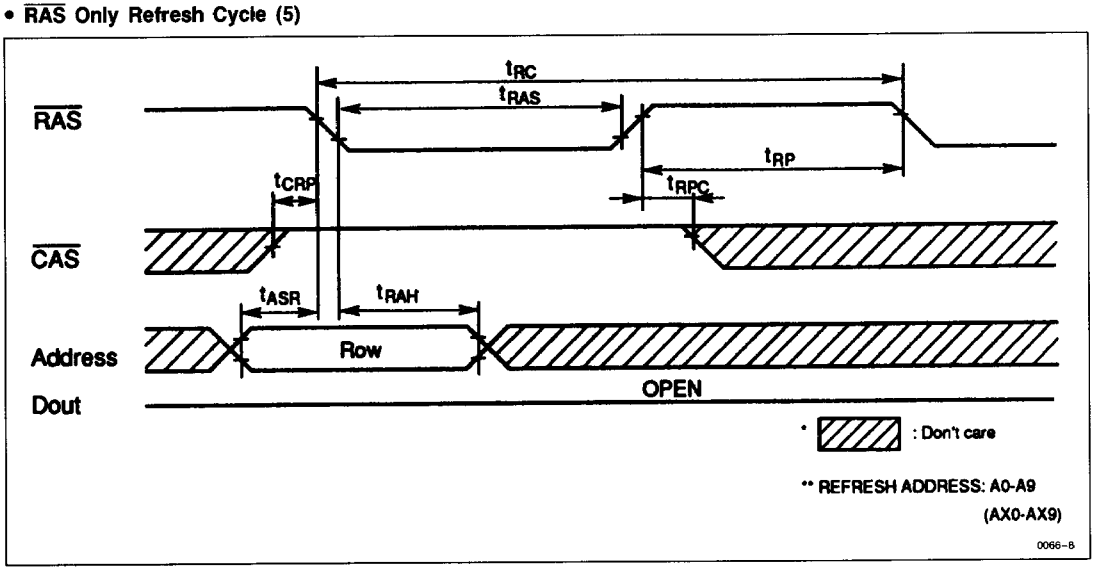
• Delayed Write Cycle (3)



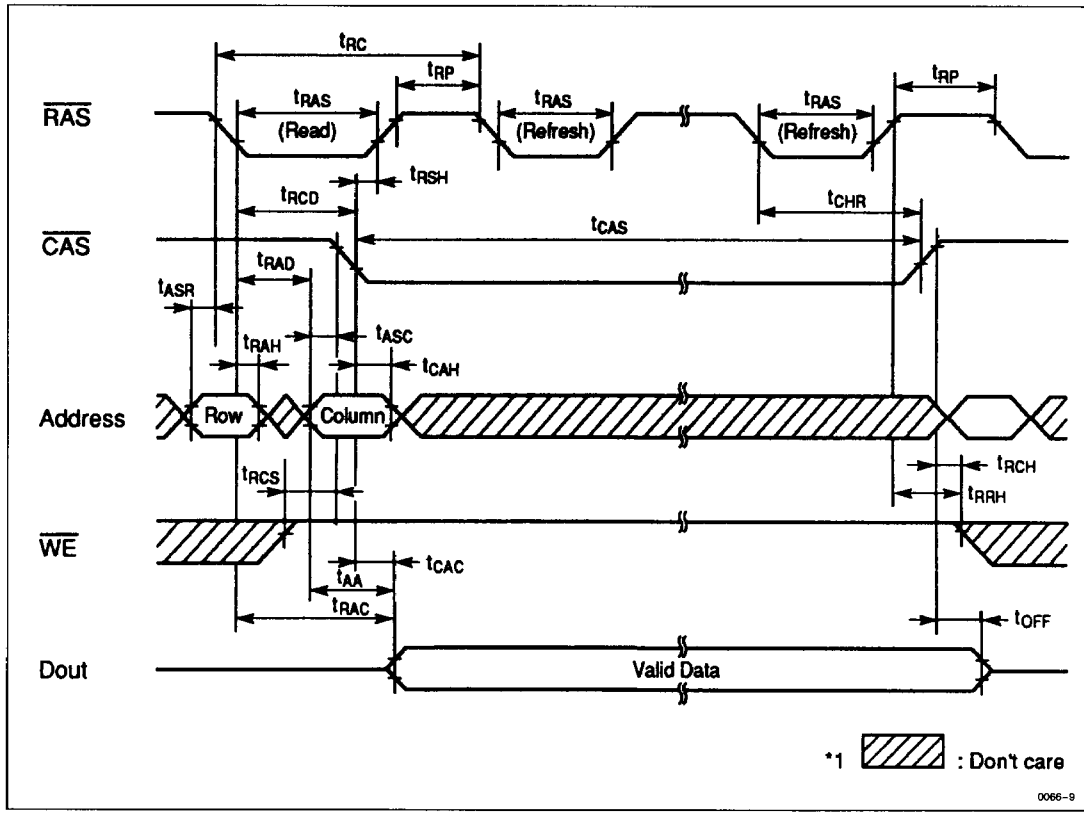
• **Read-Modify-Write Cycle (4)**



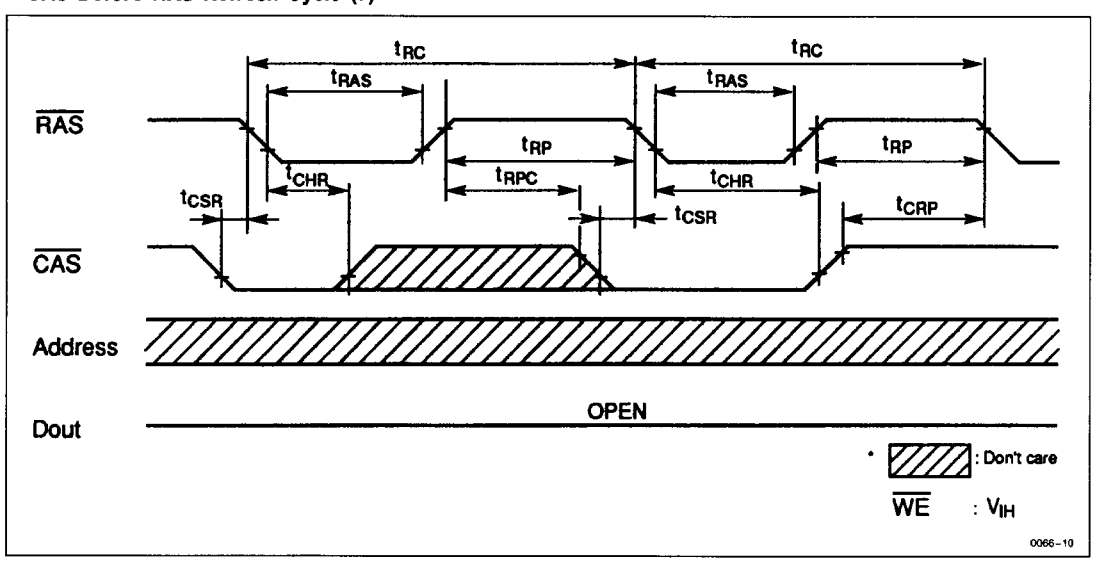
• **$\overline{RAS}$ Only Refresh Cycle (5)**



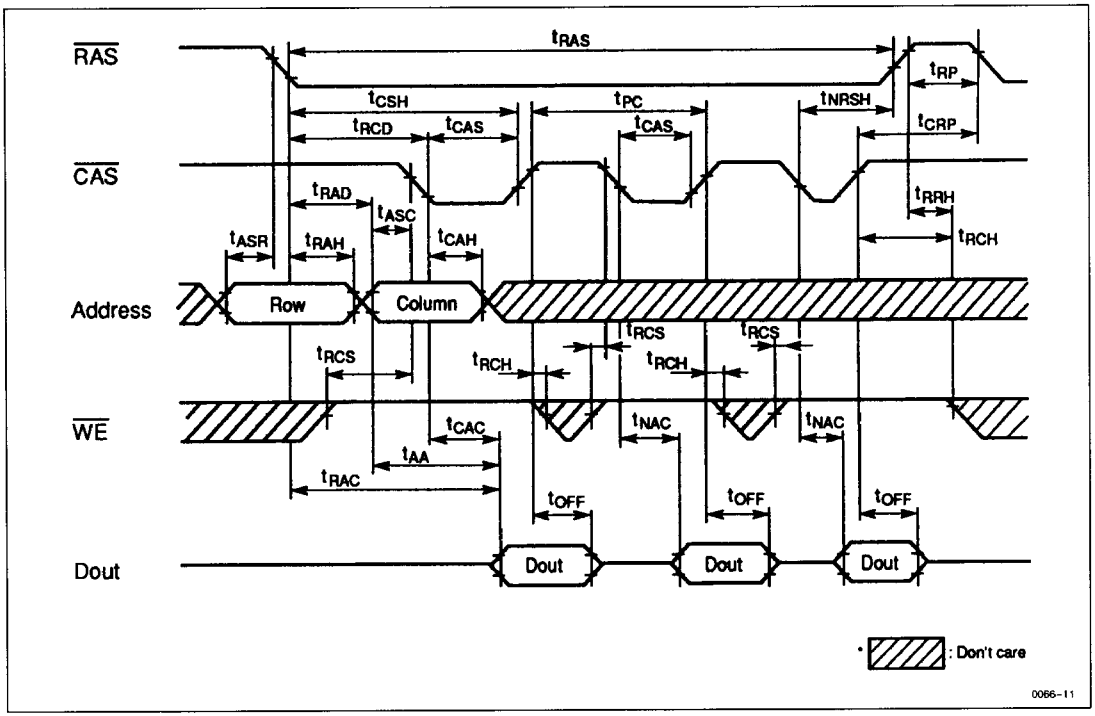
• Hidden Refresh Cycle (6)



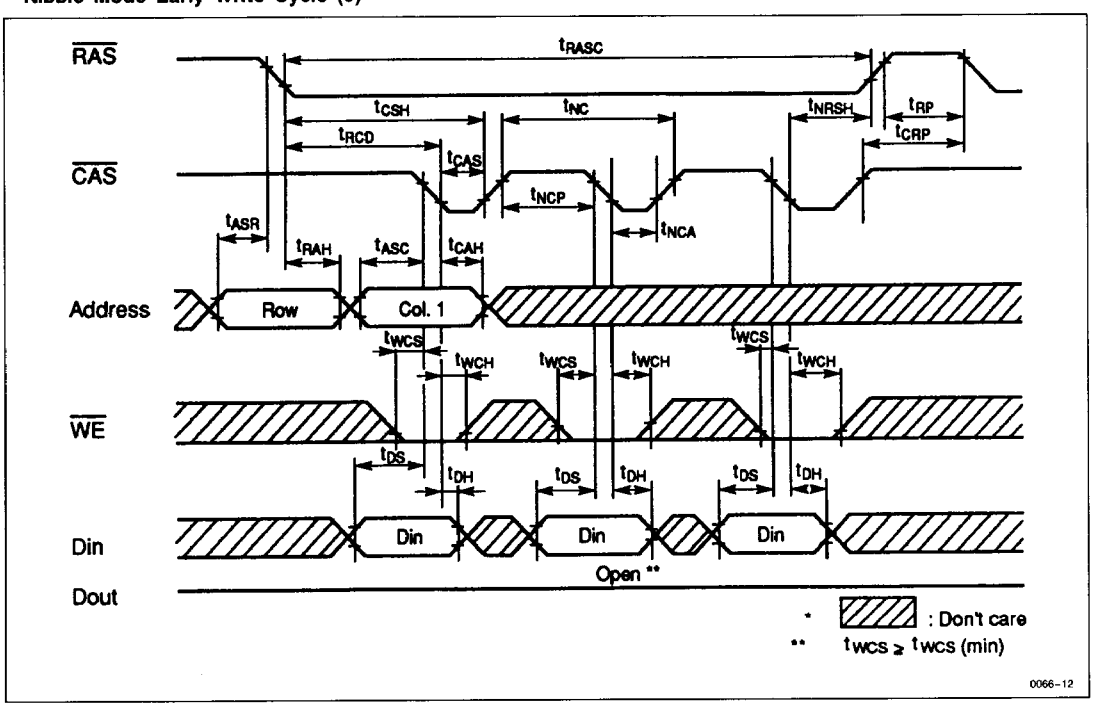
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle (7)



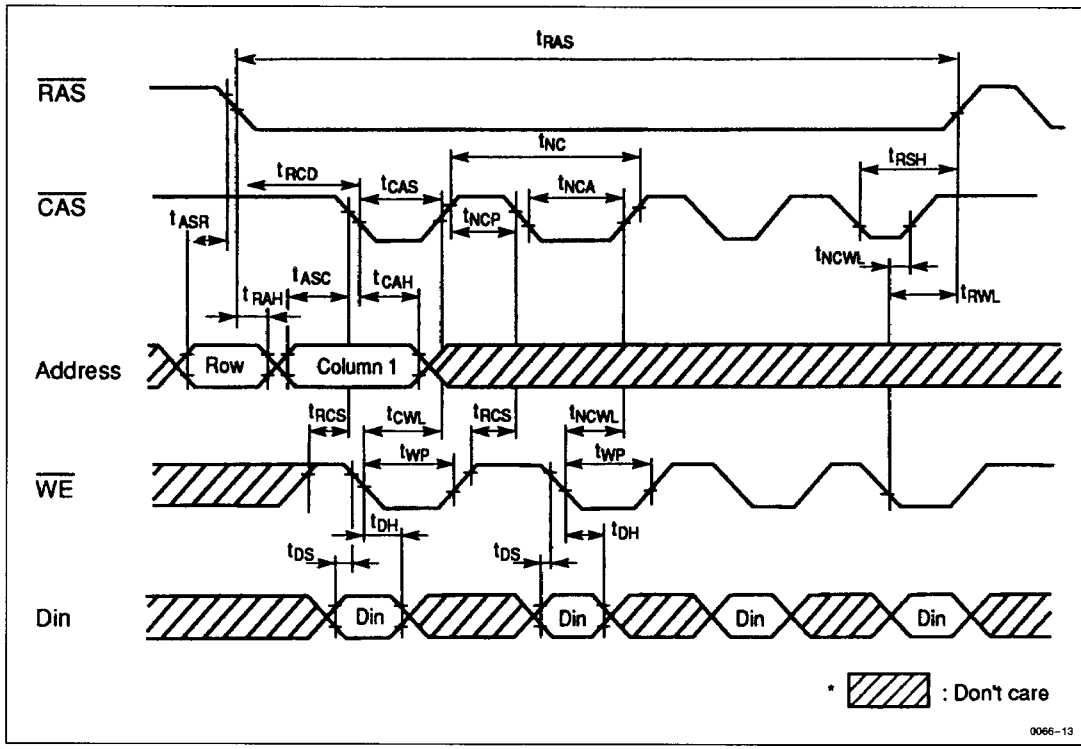
• **Nibble Mode Read Cycle (8)**



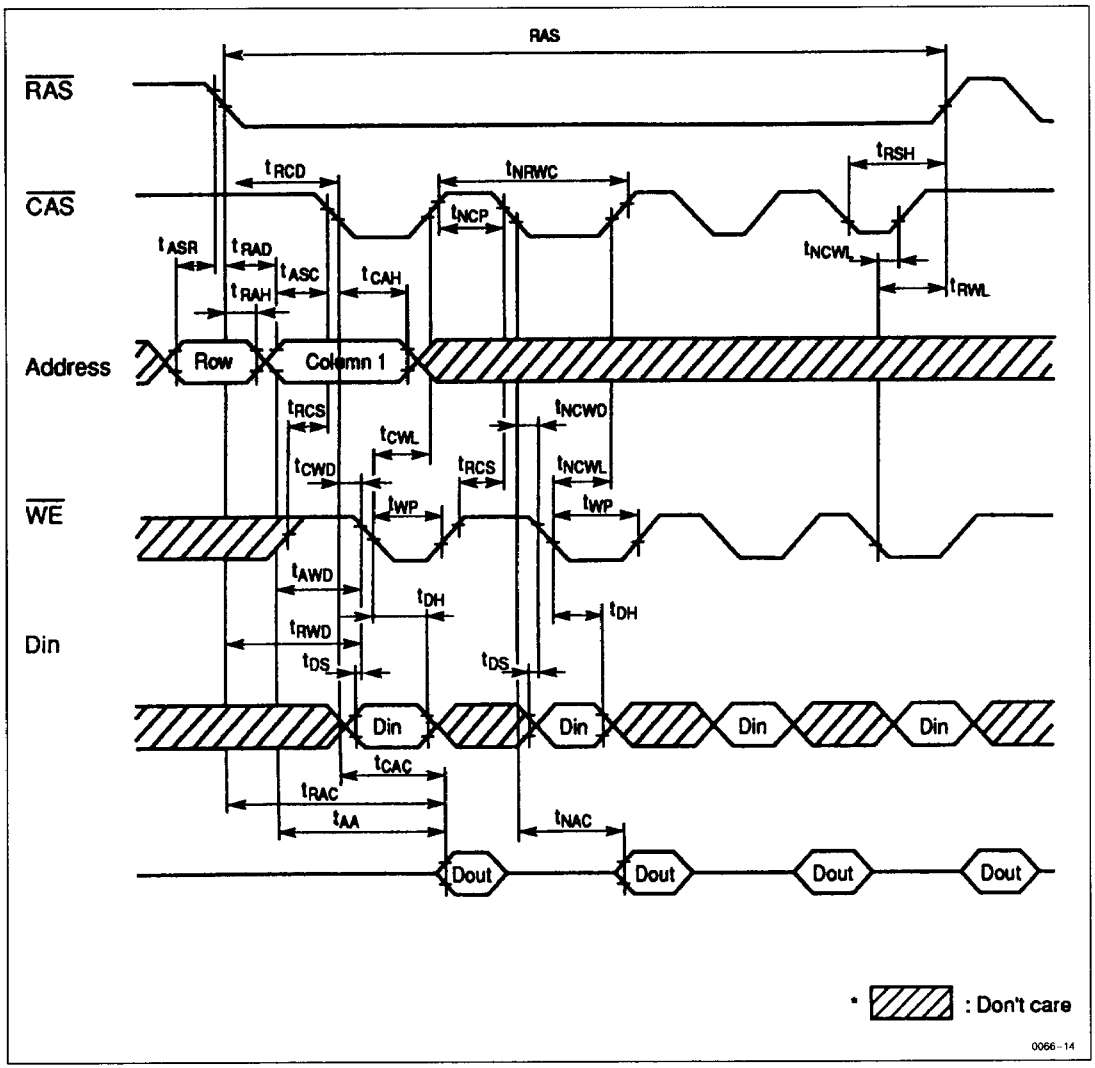
• **Nibble Mode Early Write Cycle (9)**



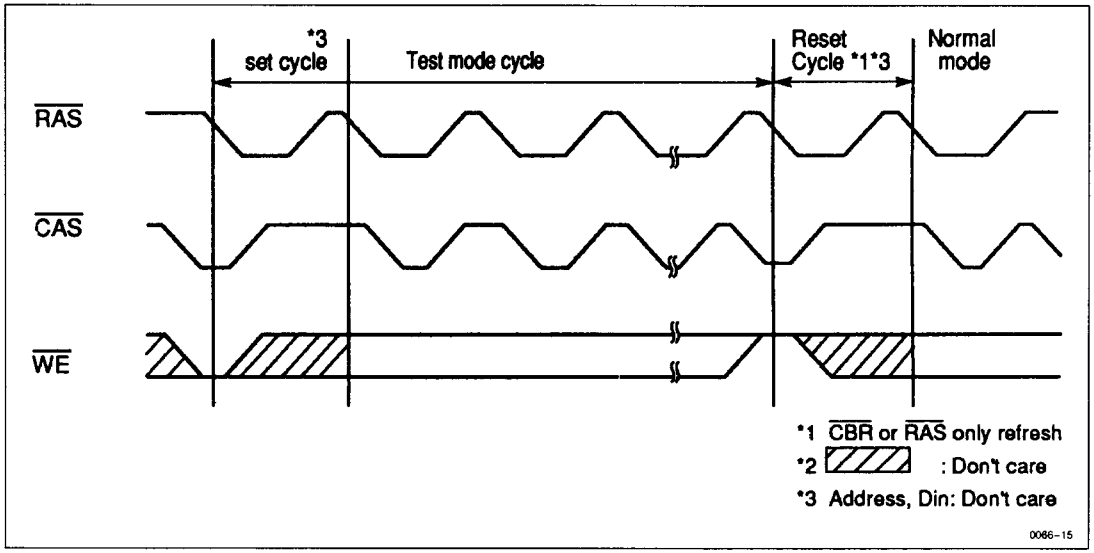
• **Nibble Mode Delayed Write Cycle (10)**



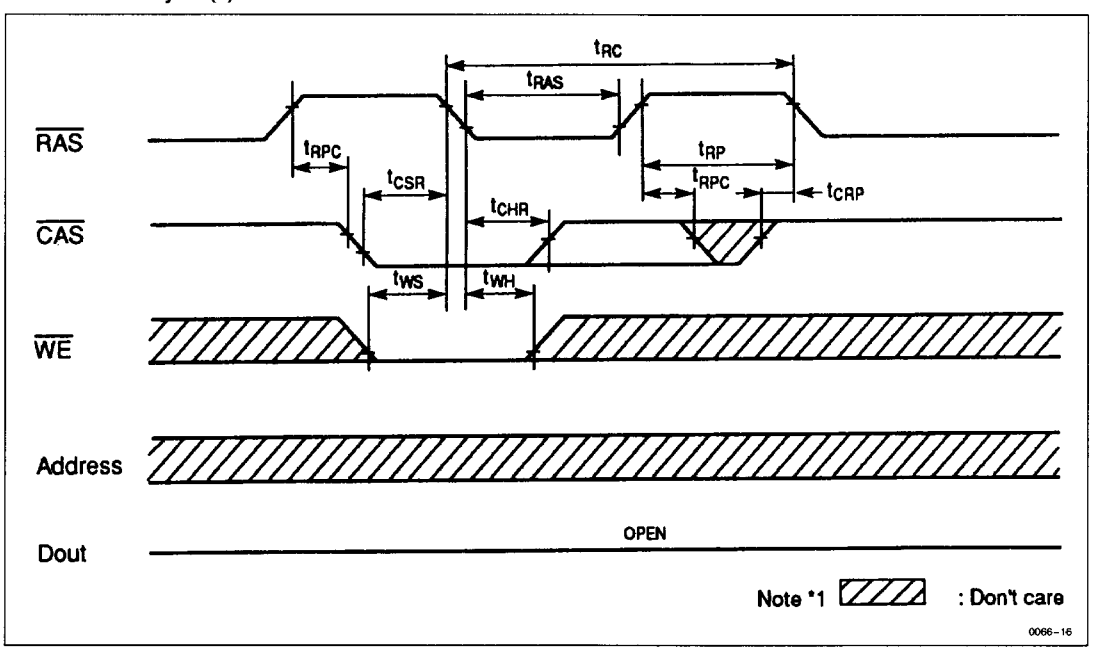
• **Nibble Mode Read-Modify-Write Cycle (11)**



• Test Mode Cycle

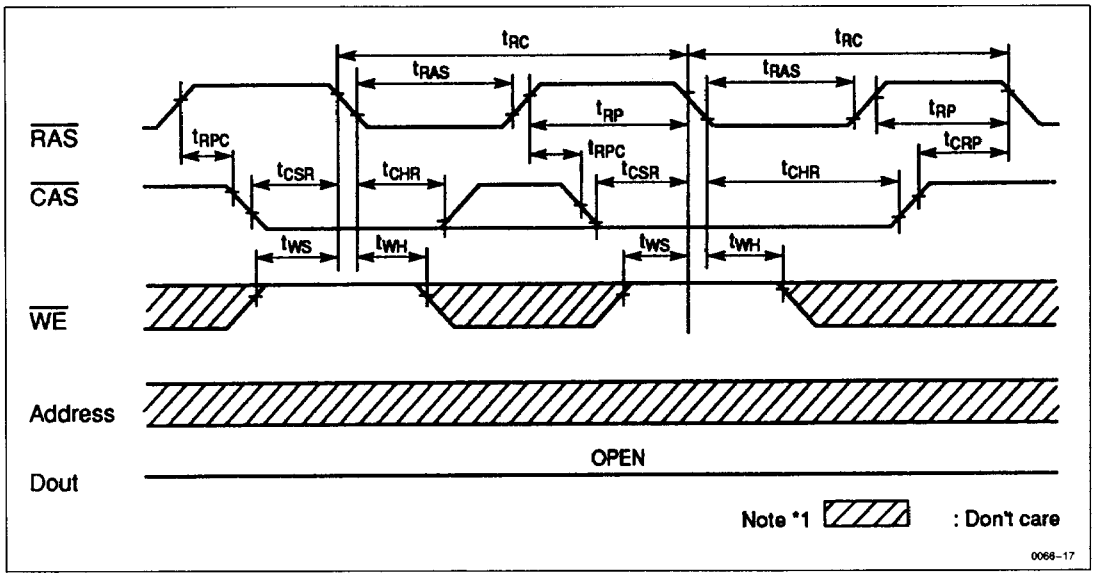


Test Mode Set Cycle (1)

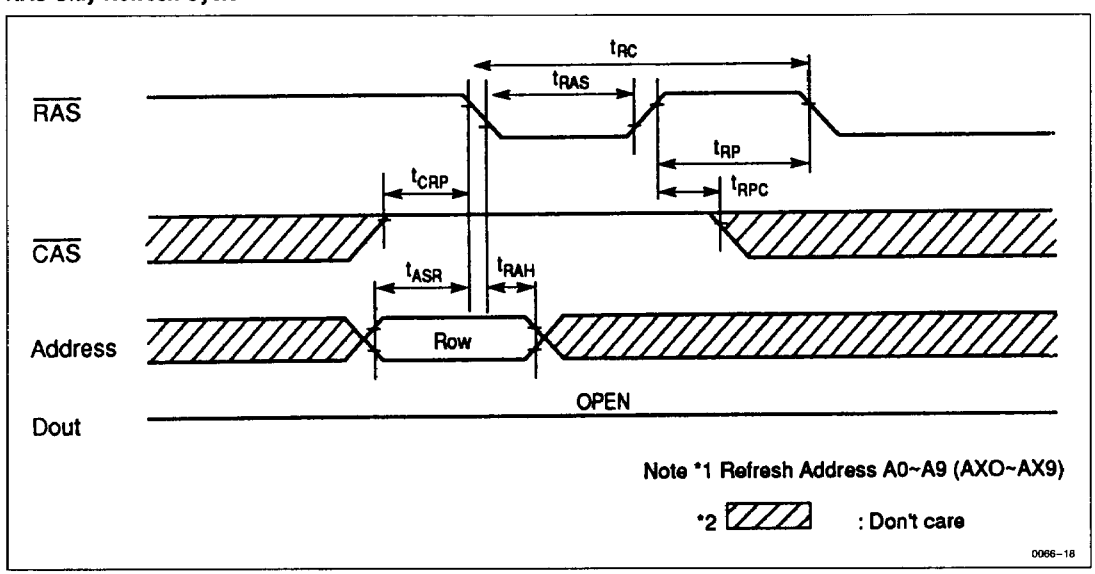


• **Test Mode Reset Cycle (2)**

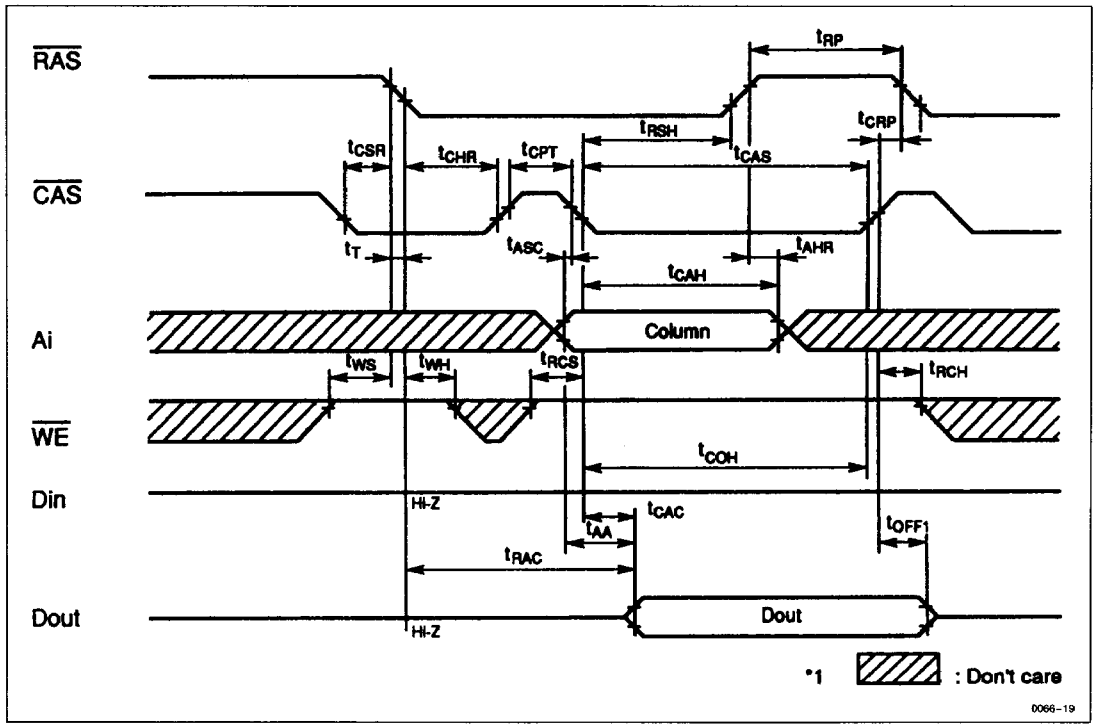
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



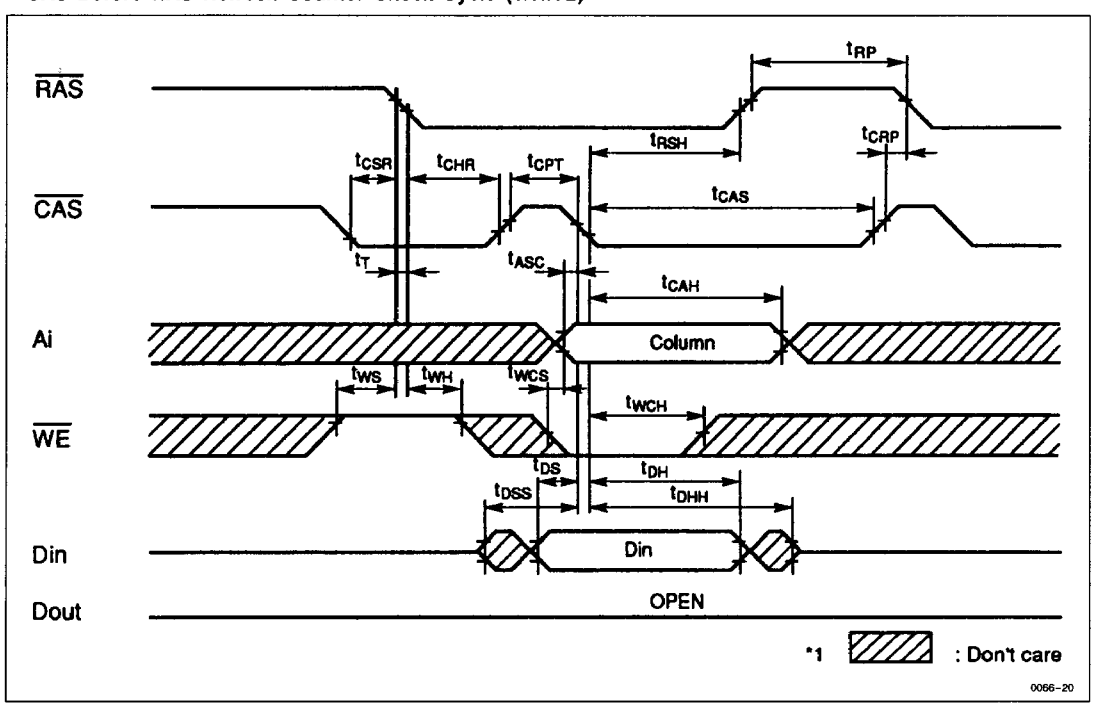
$\overline{RAS}$ Only Refresh Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (READ)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (WRITE)



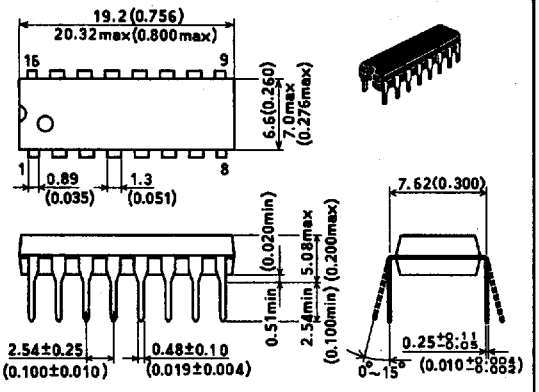
PACKAGE INFORMATION

T-90-20

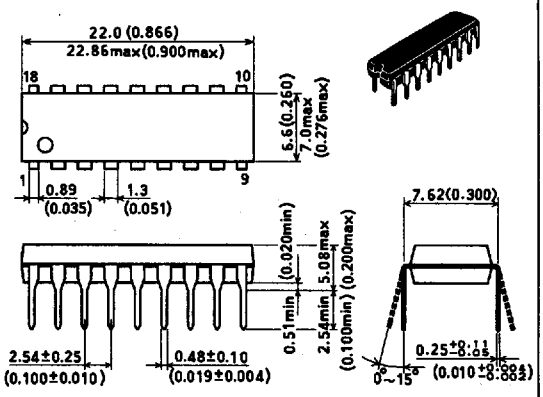
• Dual-in-line Plastic

Unit: mm (inch) Scale 3/2

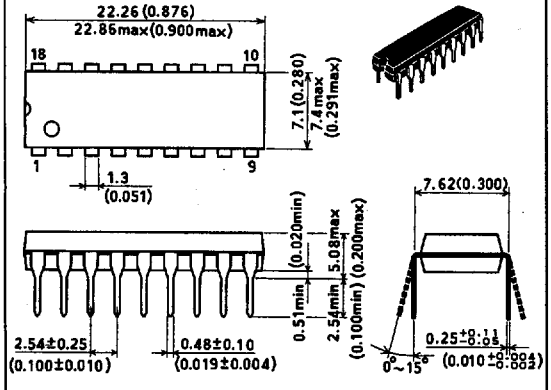
• DP-16B



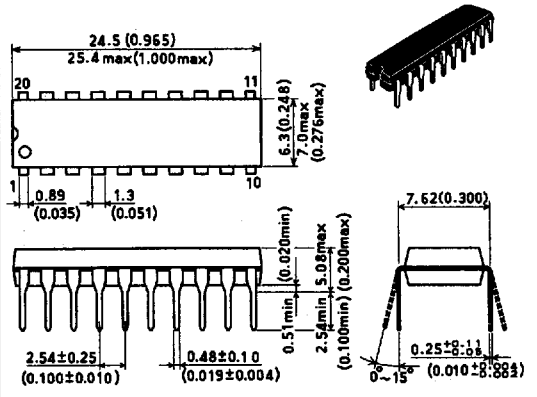
• DP-18B



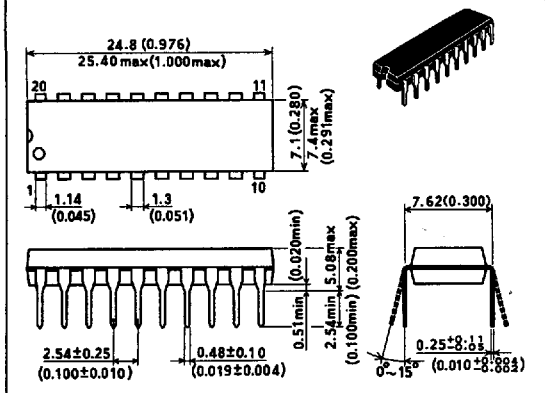
• DP-18C



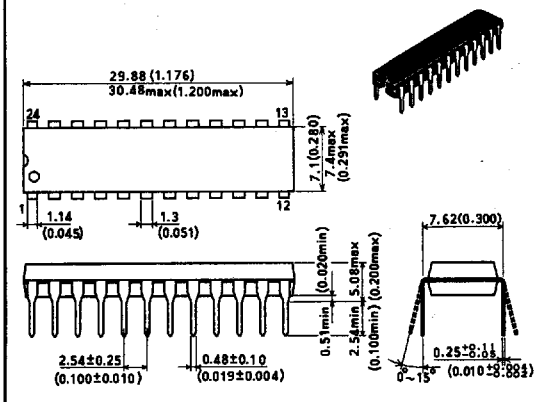
• DP-20N



• DP-20NA



• DP-20NC

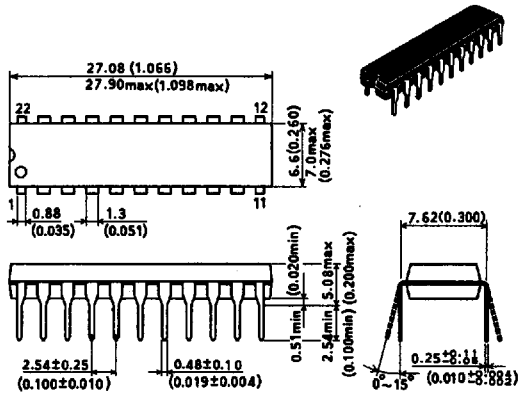


• Dual-in-line Plastic

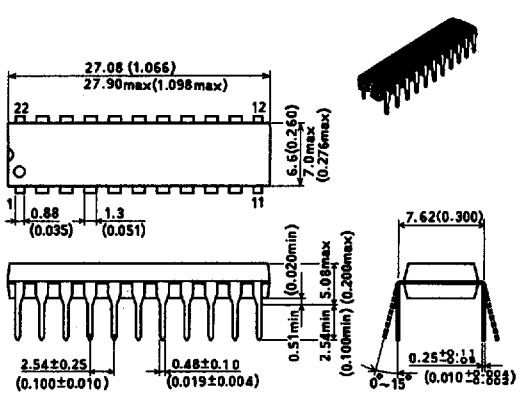
Unit: mm (inch) Scale 3/2

T-90-20

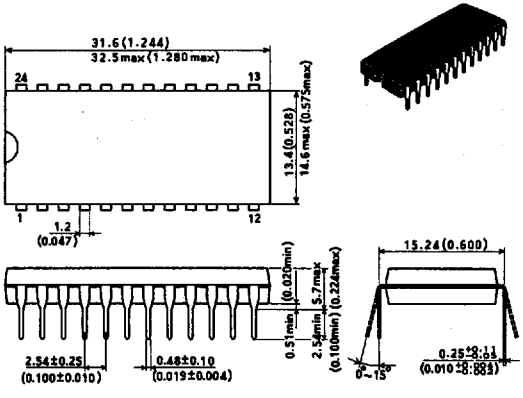
• DP-22N



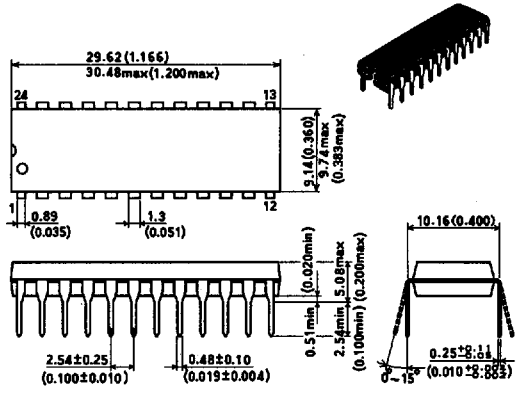
• DP-22NB



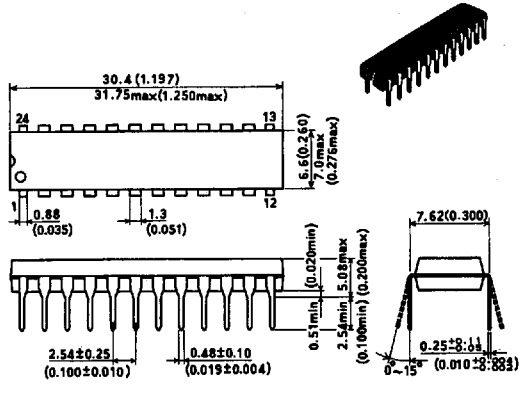
• DP-24



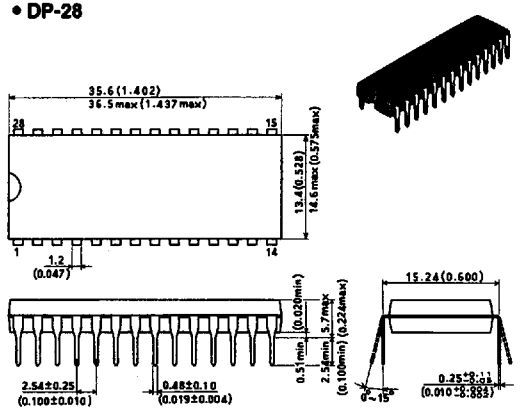
• DP-24A



• DP-24N



• DP-28



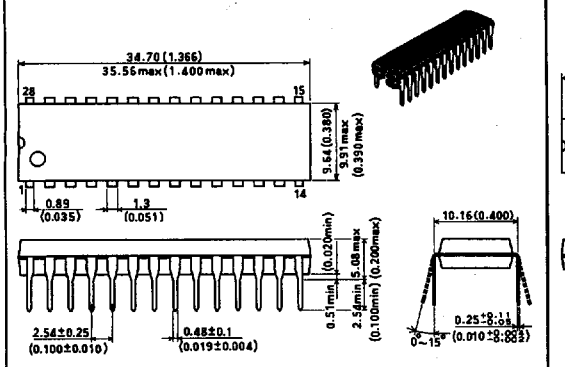
• Dual-in-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

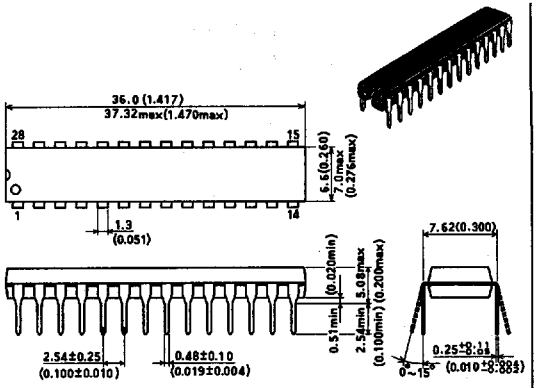
Unit: mm (inch) Scale 3/2

T-90-20

• DP-28C



• DP-28N

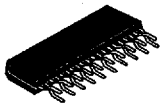


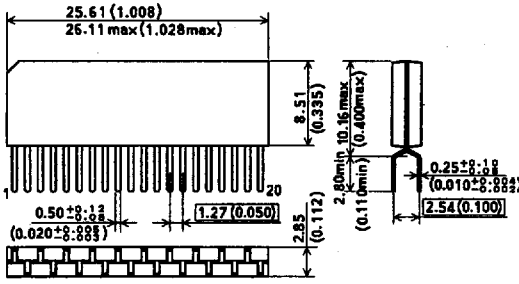
• Zigzag-in-line Plastic HITACHI/ LOGIC/ARRAYS/MEM

Unit: mm (inch) Scale 3/2

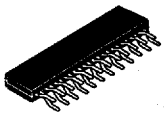
T-90-20

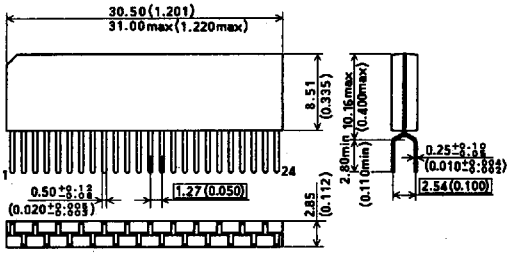
• ZP-20



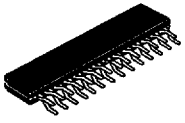


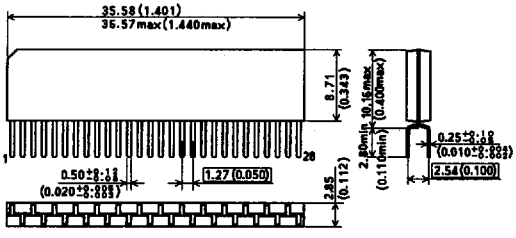
• ZP-24



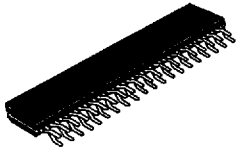


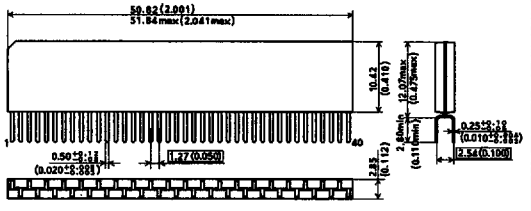
• ZP-28





• ZP-40





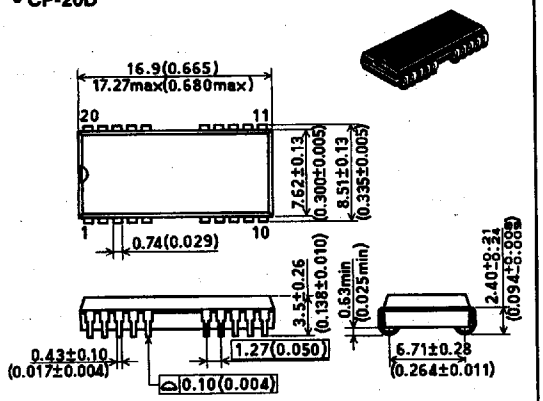
• Flat Package (J-bend Leads)

HITACHI/ LOGIC/ARRAYS/MEM

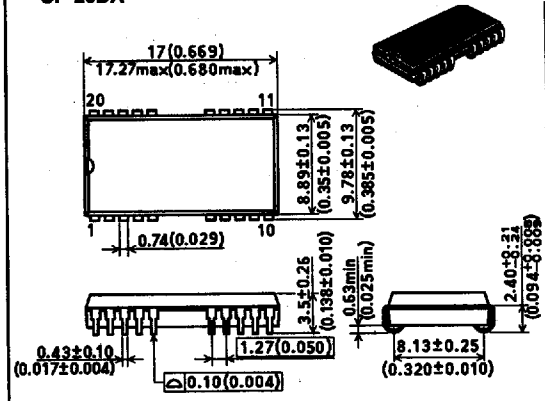
Unit: mm (inch) Scale 3/2

T-90-20

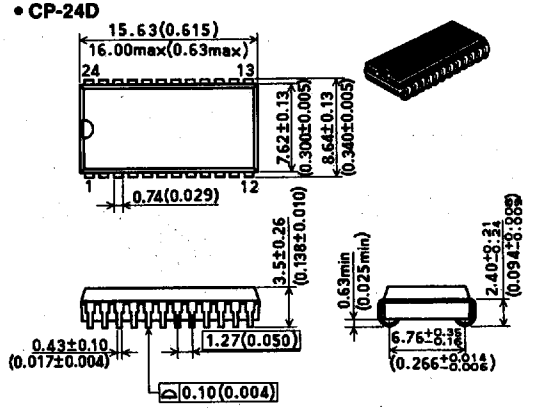
• CP-20D



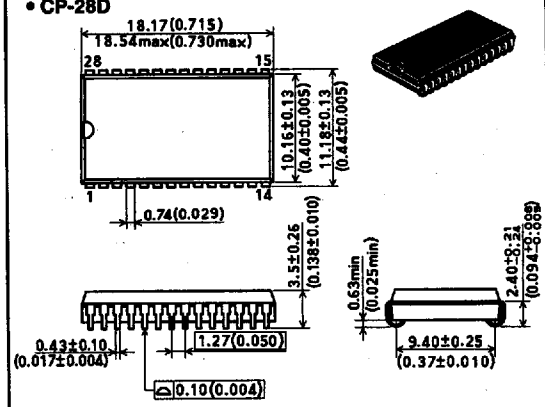
• CP-20DA



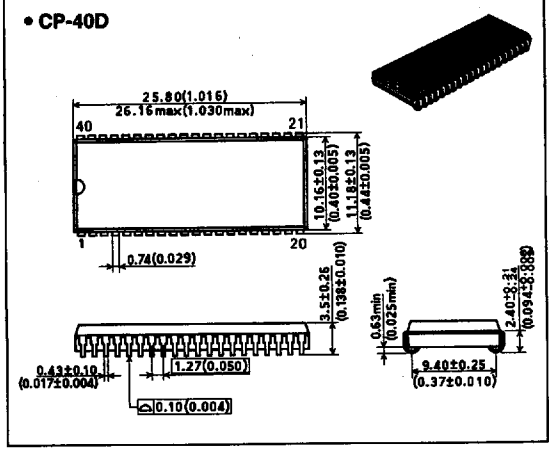
• CP-24D



• CP-28D



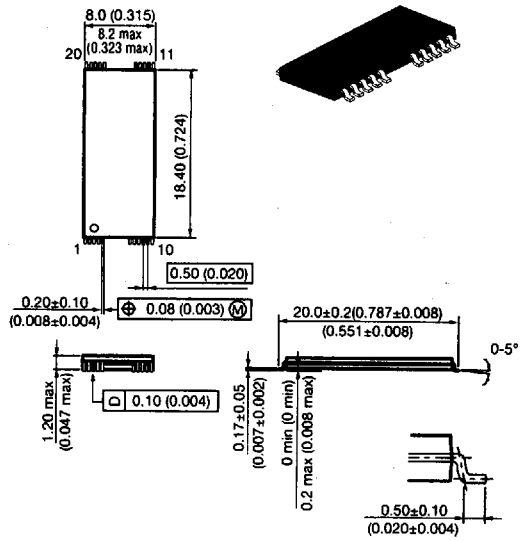
• CP-40D



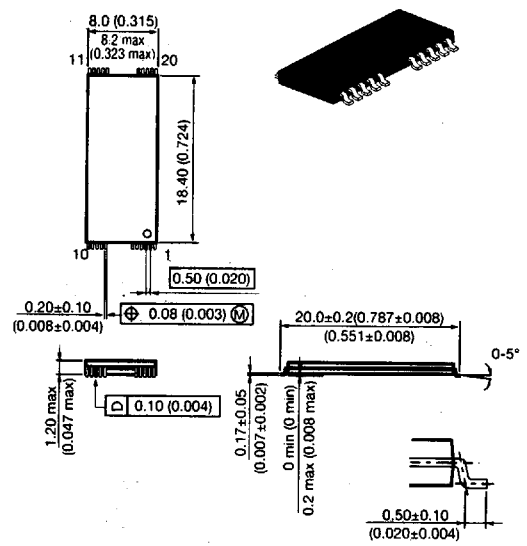
• TSOP (Thin Small Outline Package)

Unit: mm (inch) Scale 3/2

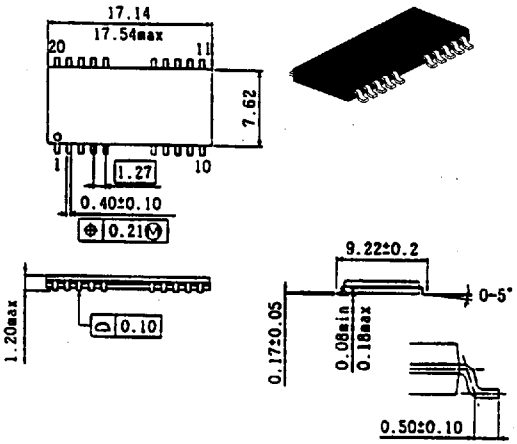
• TFP-20DA



• TFP-20DAR



• TTP-20D



• TTP-20DR