MOTOROLA

Military 54LS165

8-Bit Parallel-To-Serial Converter

ELECTRICALLY TESTED PER:
MIL-M-38510/30608

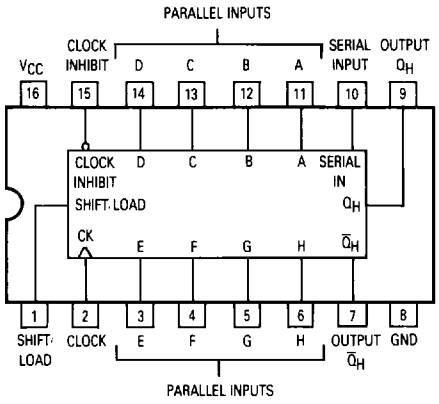
The 54LS165 is an 8-bit parallel load or serial-in register with complementary outputs available from the last stage. Parallel inputing occurs asynchronously when the Parallel Load or Shift Load ($\overline{SL}$) input is LOW. With $\overline{SL}$ HIGH, serial shifting occurs on the rising edge of the clock; new data enters via the Serial Data (SI) input. The 2-input OR clock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

AVAILABLE AS:

1) JAN: JM38510/30608BXA
2) SMD: 7700601
3) 883C: 54LS165/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2
*Call Factory for latest update

CONNECTION DIAGRAM



PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
SHIFT LOAD	1	1	2	GND
CLK	2	2	3	V_{CC}
E	3	3	4	V_{CC}
F	4	4	5	V_{CC}
G	5	5	7	V_{CC}
H	6	6	8	V_{CC}
$\overline{Q}_H$	7	7	9	OPEN
GND	8	8	10	GND
Q_H	9	9	12	V_{CC}
SERIAL IN	10	10	13	V_{CC}
A	11	11	14	V_{CC}
B	12	12	15	V_{CC}
C	13	13	17	V_{CC}
D	14	14	18	V_{CC}
CLK INHIB	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

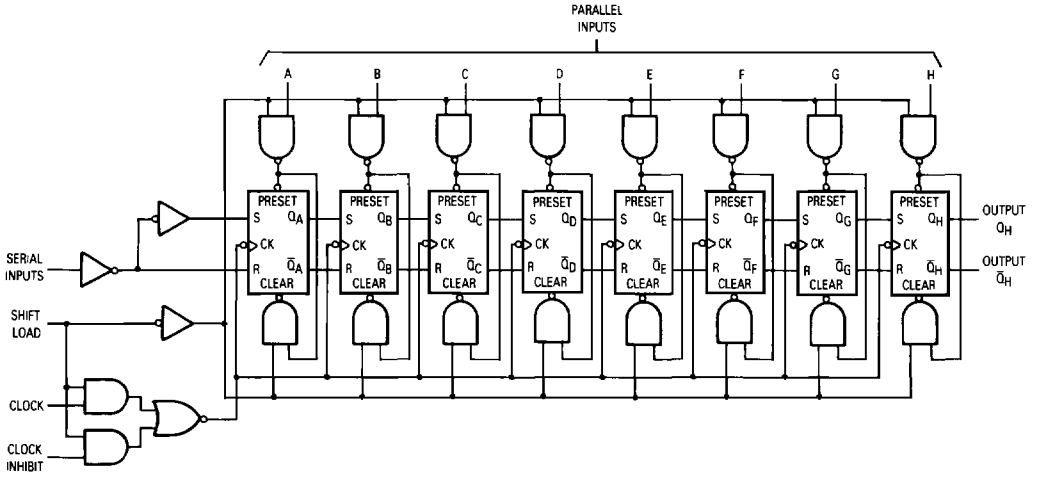
BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

SL	CP 1	CP 2	CONTENTS Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	RESPONSE
L	X	X	A	B	C	D	E	F	G	H	Parallel Entry
H	L	⎍	SI	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Right Shift
H	H	⎍	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	No Change
H	⎍	L	SI	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Right Shift
H	⎍	H	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The 54LS165 contains eight clocked master/slave RS flip-flops connected as a shift register, with auxiliary gating to provide overriding asynchronous parallel entry. Parallel data enters when the $\overline{SL}$ signal is LOW. The parallel data can change while $\overline{SL}$ is LOW, provided that the recommended setup and hold times are observed.

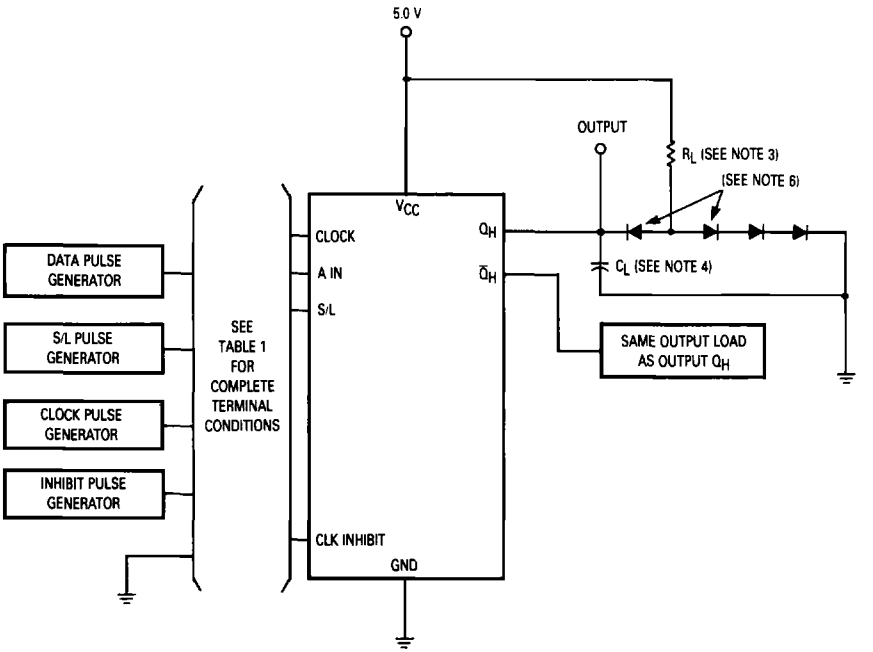
For clock operation, $\overline{SL}$ must be HIGH. The two clock inputs perform identically; one can be used as a clock inhibit by applying a HIGH signal. To avoid double clocking, however, the inhibit signal should only go HIGH while the clock is HIGH. Otherwise, the rising inhibit signal will cause the same response as a rising clock edge. The flip-flops are edge-triggered for serial operations. The serial input data can change at any time, provided only that the recommended setup and hold times are observed, with respect to the rising edge of the clock.

Pin Names		Loading (Note a)	
		HIGH	LOW
CLK, $CLK_{INHIBIT}$	Clock (LOW-to-HIGH Going Edge) Inputs	0.5 U.L.	0.25 U.L.
SI	Serial Data Input	0.5 U.L.	0.25 U.L.
$\overline{SL}$	Asynchronous Parallel Load (Active LOW) Input	1.5 U.L.	0.75 U.L.
A–H	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_H	Serial Output from Last State (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q}_H$	Complementary Output (Note b)	10 U.L.	5(2.5) U.L.

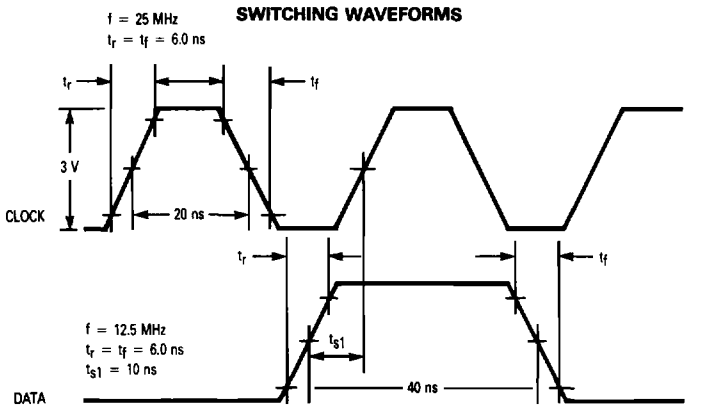
NOTES:
a. One TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) Temperature Ranges.

6

TEST CIRCUIT



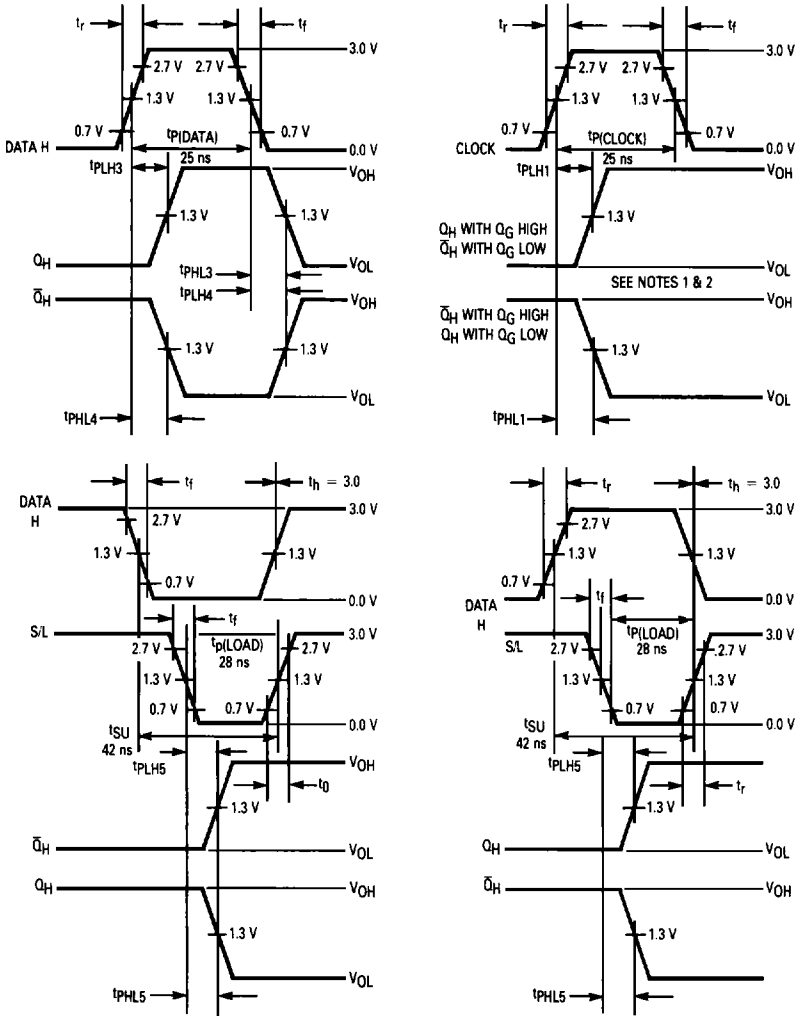
SWITCHING WAVEFORMS



f_{MAX} WAVEFORM

6

SWITCHING WAVEFORMS



NOTES:

1. For t_{PHL2} measurement, internal output G must be set to a low and Q_H to a high prior to test.
2. For t_{PLH2} measurements, internal output G must be set to a high and Q_H to a low prior to test.
3. R_L = 2.0 kΩ ± 5.0%.
4. C_L = 50 pF ± 10%, which includes probe and jig capacitance.
5. All pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$, t_r = 6.0 ns, t_f = 6.0 ns and PRR ≤ 1.0 MHz.
6. All diodes are 1N3064 or equivalent.
7. For f_{MAX}, Clock PRR = 25 MHz, $t_r = t_f$ = 6.0 ns, t_p = 20 ns and $Z_{out} \approx 50\ \Omega$; also, Serial data PRR = 12.5 MHz, $t_r = t_f$ = 6.0 ns, t_p = 40 ns and $Z_{out} \approx 50\ \Omega$.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −0.4 mA, V_{IN} = 2.0 V or 0.7 V, other inputs are open.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IN} = 0.7 V or 2.0 V, other inputs are open.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		0.1		0.1		0.1	mA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open.
$I_{IH(S/L)}$	Logical "1" Input Current		60		60		60	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
$I_{IHH(S/L)}$	Logical "1" Input Current		0.3		0.3		0.3	mA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open.
$I_{IL(CLK)}$	Logical "0" Input Current	−0.005	−0.72	−0.005	−0.72	−0.005	−0.72	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open.
I_{IL}	Logical "0" Input Current	−0.12	−0.38	−0.12	−0.38	−0.12	−0.38	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open, SHF/LD = GND.
I_{IL}, (SHF/LD)	Logical "0" Input Current	−0.005	−0.72	−0.005	−0.72	−0.005	−0.72	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open.
I_{OSH}	Output Short Circuit Current	−15	−100	−15	−100	−15	−100	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, Q_H & SHF/LD = GND, other inputs are open.
I_{OSL}	Output Short Circuit Current	−15	−100	−15	−100	−15	−100	mA	V_{CC} = 5.5 V, V_{IN} = GND, Q_H & SHF/LD = GND.
I_{CCH}	Power Supply Current Off		36		36		36	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V (all inputs).
I_{CCL}	Power Supply Current Off		36		36		36	mA	V_{CC} = 5.5 V, V_{IN} = GND, CLK & $CLK_{INHIBIT}$ = 4.5 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

6

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output CLK to Outputs	5.0	45 40	5.0	58 53	5.0	58 53	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output CLK to Outputs	5.0	45 40	5.0	58 53	5.0	58 53	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL3} t_{PHL3}	Propagation Delay /Data-Output H to Q_H	5.0	35 30	5.0	46 41	5.0	46 41	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH3} t_{PLH3}	Propagation Delay /Data-Output H to Q_H	5.0	30 25	5.0	39 34	5.0	39 34	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL4} t_{PHL4}	Propagation Delay /Data-Output H to $\overline{Q}_H$	5.0	30 25	5.0	39 34	5.0	39 34	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH4} t_{PLH4}	Propagation Delay /Data-Output H to $\overline{Q}_H$	5.0	35 30	5.0	46 41	5.0	46 41	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL5} t_{PHL5}	Propagation Delay /Data-Output S/L to Outputs	5.0	40 35	5.0	52 47	5.0	52 47	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH5} t_{PLH5}	Propagation Delay /Data-Output S/L to Outputs	5.0	40 35	5.0	52 47	5.0	52 47	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
f_{MAX}	Maximum Clock Frequency	25 25		20		20		MHz MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.