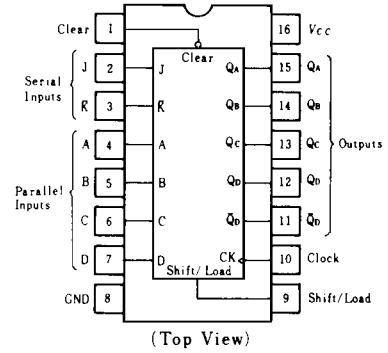


HD74HC195 ● 4-bit Parallel-Access Shift Register

This shift register features parallel inputs, parallel outputs, J-K serial inputs, Shift/Load control input, and a direct overriding clear. This shift register can operate in two modes: Parallel load; Shift from Q_A towards Q_D .

Parallel loading is accomplished by applying the four bits of data, and taking the Shift/Load control Input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the Shift/Load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs allow the first stage to perform as a J-K or toggle flip-flop as shown in the function table.

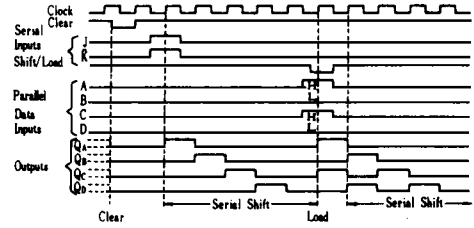
■ PIN ARRANGEMENT



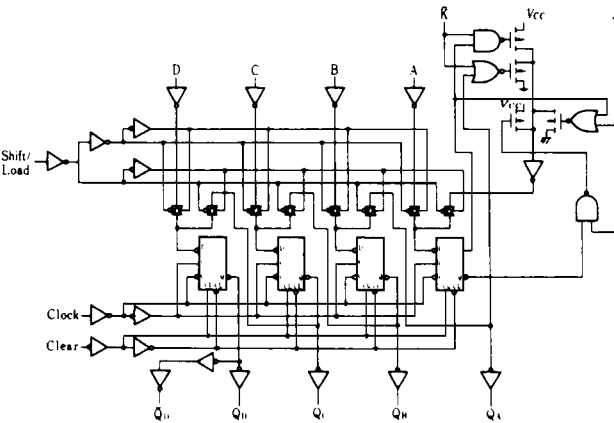
■ FEATURES

- High Speed Operation: t_{pd} (Clock to Q) = 13ns typ. ($C_L = 50pF$)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{cc} = 2 \sim 6V$
- Low Input Current: $1\mu A$ max.
- Low Quiescent Supply Current: I_{cc} (static) = $4\mu A$ max. ($T_a = 25^\circ C$)

■ TIMING DIAGRAM



■ LOGIC DIAGRAM



■ FUNCTION TABLE

Inputs			Outputs										
Clear	Shift/Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	\bar{Q}_D
			J	\bar{K}	A	B	C	D					
L	x	x	x	x	x	x	x	x	L	L	L	L	H
H	L	\nearrow	x	x	a	b	c	d	a	b	c	d	\bar{d}
H	H	L	x	x	x	x	x	x	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	\bar{Q}_{D0}
H	H	\nearrow	L	H	x	x	x	x	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	H	\nearrow	L	L	x	x	x	x	L	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	H	\nearrow	H	H	x	x	x	x	H	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	H	\nearrow	H	L	x	x	x	x	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}

H = high level (steady state)
 L = low level (steady state)
 x = don't care
 \nearrow = transition from low to high level
 a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

$Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}$ = the level of $Q_A, Q_B, Q_C,$ or $Q_D,$ respectively, before the indicated steady-state input conditions were established.
 $Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}$ = the level of $Q_A, Q_B, Q_C,$ or $Q_D,$ respectively, before the most-recent \nearrow transition of the clock.

■ DC CHARACTERISTICS

Item	Symbol	V _{CC} (V)	Test Conditions	T _a = 25°C			T _a = -40 ~ +85°C		Unit		
				min	typ	max	min	max			
Input Voltage	V _{IH}	2.0		1.5	—	—	1.5	—	V		
		4.5		3.15	—	—	3.15	—			
		6.0		4.2	—	—	4.2	—			
	V _{IL}	2.0		—	—	0.5	—	0.5	V		
		4.5		—	—	1.35	—	1.35			
		6.0		—	—	1.8	—	1.8			
Output Voltage	V _{OH}	2.0	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA		1.9	2.0	—	1.9	—	V
		4.5		4.4	4.5	—	4.4	—			
		6.0		5.9	6.0	—	5.9	—			
		4.5		I _{OH} = -4mA		4.18	—	—	4.13	—	
		6.0		I _{OH} = -5.2mA		5.68	—	—	5.63	—	
	V _{OL}	2.0	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA		—	0.0	0.1	—	0.1	V
		4.5		—	0.0	0.1	—	0.1			
		6.0		—	0.0	0.1	—	0.1			
		4.5		I _{OL} = 4mA		—	—	0.26	—	0.33	
		6.0		I _{OL} = 5.2mA		—	—	0.26	—	0.33	
Input Current	I _{IN}	6.0	V _{IN} = V _{CC} or GND	—	—	±0.1	—	±1.0	μA		
Quiescent Supply Current	I _{CC}	6.0	V _{IN} = V _{CC} or GND, I _{OUT} = 0 μA	—	—	4.0	—	40	μA		

■ AC CHARACTERISTICS (C_L = 50pF, Input t_r = t_f = 6ns)

Item	Symbol	V _{CC} (V)	Test Conditions	T _a = 25°C			T _a = -40 ~ +85°C		Unit	
				min	typ	max	min	max		
Maximum Clock Frequency	f _{max}	2.0		—	—	6	—	5	MHz	
		4.5		—	—	30	—	24		
		6.0		—	—	35	—	28		
Propagation Delay Time	t _{PHL}	2.0	Clock to Q	—	—	140	—	175	ns	
		4.5		—	13	28	—	35		
		6.0		—	—	24	—	30		
	t _{PLH}	2.0		—	—	140	—	175	ns	
		4.5		—	13	28	—	35		
		6.0		—	—	24	—	30		
	t _{PHL}	2.0		Clear to Q	—	—	150	—	190	ns
		4.5			—	15	30	—	38	
		6.0			—	—	26	—	33	
Pulse Width	t _w	2.0	Clock to Clear	80	—	—	100	—	ns	
		4.5		16	7	—	20	—		
		6.0		14	—	—	17	—		
Setup Time	t _{su}	2.0	A, B, C, D, J, \bar{K} to Clock	100	—	—	125	—	ns	
		4.5		20	6	—	25	—		
		6.0		17	—	—	21	—		
		2.0	Shift/ Load to Clock	100	—	—	125	—		
		4.5		20	13	—	25	—		
		6.0		17	—	—	21	—		
Hold Time	t _h	2.0	Any Input except Shift / Load	0	—	—	0	—	ns	
		4.5		0	-3	—	0	—		
		6.0		0	—	—	0	—		

Item	Symbol	V _{CC} (V)	Test Conditions	T _a = 25°C			T _a = -40~+85°C		Unit
				min	typ	max	min	max	
Removal Time	t _{rem}	2.0	Shift / Load to Clock	75	—	—	95	—	ns
		4.5		15	8	—	19	—	
		6.0		13	—	—	16	—	
		2.0	Clear inactive to Clock	25	—	—	31	—	
		4.5		5	0	—	6	—	
		6.0		4	—	—	5	—	
Output Rise / Fall Time	t _{TLH}	2.0		—	—	75	—	95	ns
		4.5		—	5	15	—	19	
	t _{THL}	6.0		—	—	13	—	16	
Input Capacitance	C _{in}	—		—	5	10	—	10	pF