Data sheet	
status	Objective specification
date of issue	July 1990

SAA9065P

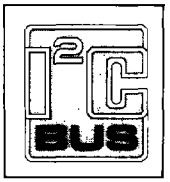
Video enhancement and digital-analog processor

GENERAL DESCRIPTION

The digital video signal processing system is based on the Digital Multistandard Decoder (DMSD) SAA7151 and the 'Video Enhancement and Digital-Analog processor' (VEDA) SAA9065. The decoder provides a reference signal for generating a line-locked clock which in turn allows simple application of memory based features.
The VEDA is the back end for the digital processing path which includes decoding and feature processing. The system supports a digital YUV bus for selection of different video signal sources.

The data rate supported by the bus is:
13.5 MHz = 858 x fh (NTSC) or 864 x fh (PAL/SECAM) and
27 MHz = 1716 x fh (NTSC) or 1728 x fh (PAL/SECAM).
The support organization is : 7 and 8 bit.
The number of active samples per line is : 720 on the YUV bus.
The system provides a line locked clock (LL27) of 27 MHz.

The YUV bus and the VEDA data input are fully synchronous with respect to the clock signal LL27. A line reference signal HREF, for timing control purposes, is provided by the decoder which controls the system timing independent of active signal sources or desired functions.



QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DD(d)}$	digital supply voltage	4.5	5.5	V
$V_{DD(a)}$	analog supply voltage	4.5	5.5	V
T_{amb}	operating ambient temperature range	0	+70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9065P	44	PLCC	plastic	SOT187AA,AGA

FUNCTIONAL DESCRIPTION

The VEDA will be produced in a CMOS process. The device operates at a frequency of either 13.5 MHz or 27.0 MHz (in progressive scan applications). 7 and 8 input signal wordwidths for luminance Y and colour difference signals U and V are supported.
The data formats on the external YUV data bus must correspond to the specified formats given in Tables 1 and 2.
For processing functions the VEDA contains (see Fig.1);

- a **formatter** unit at the digital input, to convert the supported data formats into a processable internal data stream
- a **timing control** block, which generates the necessary clock and synchronization signals for the internal processing
- an **I²C-bus** interface, which decodes the external control information into internal control switches
- an **H-peaking** unit, which performs horizontal peaking on the luminance information
- an **interpolation** filter for 4:1:1 and 4:2:2 formats in the chrominance path, to increase the data rate of the colour difference signals up to 13.5 (27.0) MHz in front of the digital-to-analog conversion
- a **DCTI** (Digital Colour Transition Improvement) block to increase the sharpness of colour transitions.

Prior to the digital-to-analog conversion, depending upon the connected RGB processor;

- it is possible to change the polarity of the colour difference components
- the data is matched to a unipolar DAC
- the digital outputs are clamped during the horizontal blanking period.

Table 1 The 4:2:2 signal format

BUS SIGNAL						
Y7	Y7	Y7	Y7	Y7	Y7	Y7
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y0	Y0	Y0	Y0	Y0	Y0	Y0
UV7	U7	V7	U7	V7	U7	V7
UV6	U6	V6	U6	V6	U6	V6
UV5	U5	V5	U5	V5	U5	V5
UV4	U4	V4	U4	V4	U4	V4
UV3	U3	V3	U3	V3	U3	V3
UV2	U2	V2	U2	V2	U2	V2
UV1	U1	V1	U1	V1	U1	V1
UV0	U0	V0	U0	V0	U0	V0
bus clock	0	1	2	3	4	5
time frame	0		1		2	

Data rate: 13.5 MHz

Sample frequency:

- Y = 13.5 MHz
- U = 6.75 MHz
- V = 6.75 MHz

The quoted frequencies are valid on the YUV bus if the bus clock is 13.5 MHz.
The time frames are controlled by the HREF signal.

Table 2 The 4:1:1 signal format

BUS SIGNAL								
Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
UV7	U7	U5	U3	U1	U7	U5	U3	U1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV4	V6	V4	V2	V0	V6	V4	V2	V0
bus frame	0	1	2	3	4	5	6	7
time frame	0				1			

Data rate: 13.5 MHz

Sample frequency:

- Y = 13.5 MHz
- U = 3.375 MHz
- V = 3.375 MHz

The quoted frequencies are valid on the YUV bus if the bus clock is 13.5 MHz.
The time frames are controlled by the HREF signal.

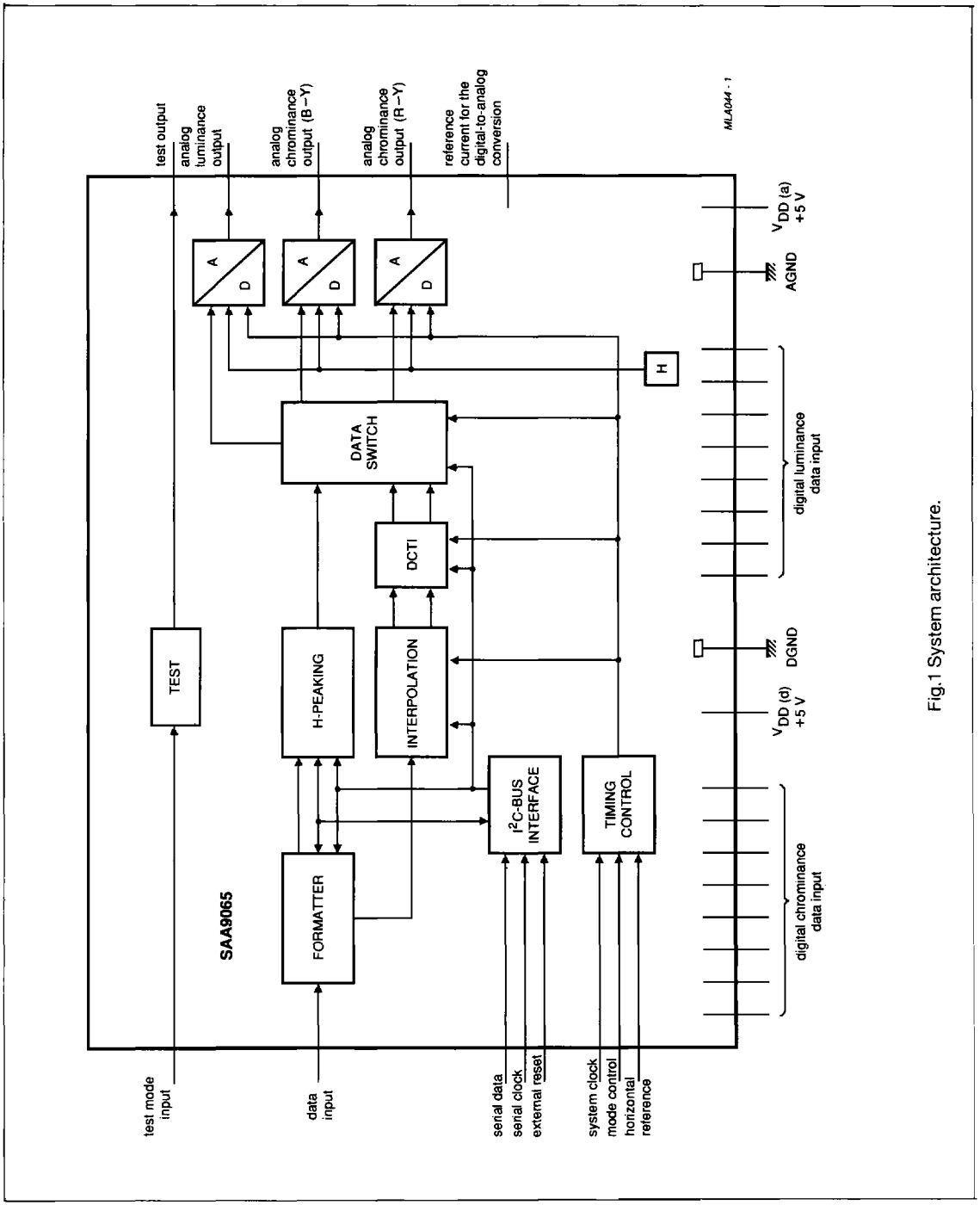


Fig.1 System architecture.

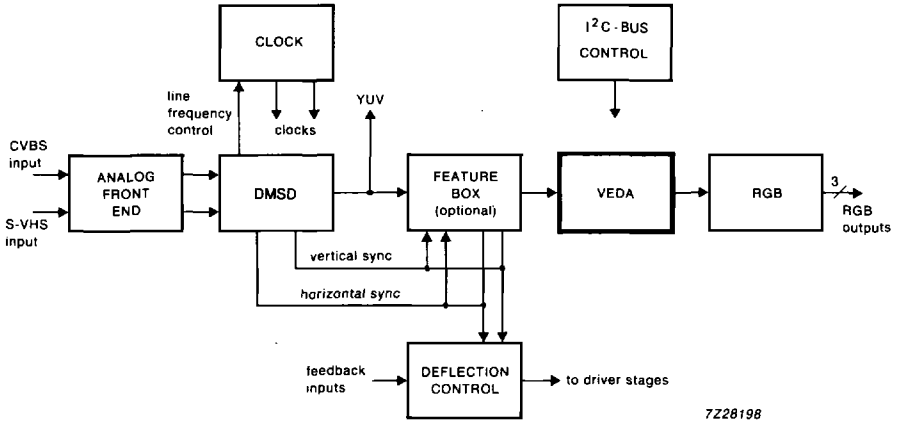


Fig.2 VEDA block diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.