MC-421000A36
1,048,576 x 36-Bit
Dynamic CMOS RAM Module

Description

The MC-421000A36 is a fast-page dynamic RAM module organized as 1,048,576 words by 36 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 1024 address combinations of A_0 - A_9 during a 16-ms period.

The MC-421000A36 is packaged in a variety of 72-pin Single Inline Memory Modules (SIMM™). Each SIMM contains eight 1,048,576 x 4-bit DRAMs (μPD424400), four 1,048,576 x 1-bit DRAMs (μPD421000), and 12 power supply decoupling capacitors for noise reduction.

Features

- 1,048,576-word by 36-bit organization
- Single +5-volt power supply
- Fast-page option
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 1024 refresh cycles every 16 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

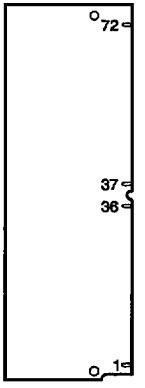
SIMM is a trademark of Wang Laboratories.

Pin Identification

Name	Function
A_0 - A_9	Address inputs
$\overline{CAS_0}$ - $\overline{CAS_3}$	Column address strobes
DQ_0 - DQ_{35}	Common data inputs/outputs
$\overline{RAS_0}$, $\overline{RAS_2}$	Row address strobes
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configuration

72-Pin SIMM



Pin	Symbol
1	GND
2	DQ_0
3	DQ_{18}
4	DQ_1
5	DQ_{19}
6	DQ_2
7	DQ_{20}
8	DQ_3
9	DQ_{21}
10	V_{CC}
11	NC
12	A_0
13	A_1
14	A_2
15	A_3
16	A_4
17	A_5
18	A_6

Pin	Symbol
19	NC
20	DQ_4
21	DQ_{22}
22	DQ_5
23	DQ_{23}
24	DQ_6
25	DQ_{24}
26	DQ_7
27	DQ_{25}
28	A_7
29	NC
30	V_{CC}
31	A_8
32	A_9
33	NC
34	$\overline{RAS_2}$
35	DQ_{26}
36	DQ_8

Pin	Symbol
37	DQ_{17}
38	DQ_{35}
39	GND
40	$\overline{CAS_0}$
41	$\overline{CAS_2}$
42	$\overline{CAS_3}$
43	$\overline{CAS_1}$
44	$\overline{RAS_0}$
45	NC
46	NC
47	$\overline{WE}$
48	NC
49	DQ_9
50	DQ_{27}
51	DQ_{10}
52	DQ_{28}
53	DQ_{11}
54	DQ_{29}

Pin	Symbol
55	DQ_{12}
56	DQ_{30}
57	DQ_{13}
58	DQ_{31}
59	V_{CC}
60	DQ_{32}
61	DQ_{14}
62	DQ_{33}
63	DQ_{15}
64	DQ_{34}
65	DQ_{16}
66	NC
67	[Note 1]
68	[Note 1]
69	[Note 1]
70	[Note 1]
71	NC
72	GND

Notes:

[1] Pins 67-70 are defined by access time:

Pin	60 ns	70 ns	80 ns	100 ns
67	GND	GND	GND	GND
68	GND	GND	GND	GND
69	NC	GND	NC	GND
70	NC	NC	GND	GND

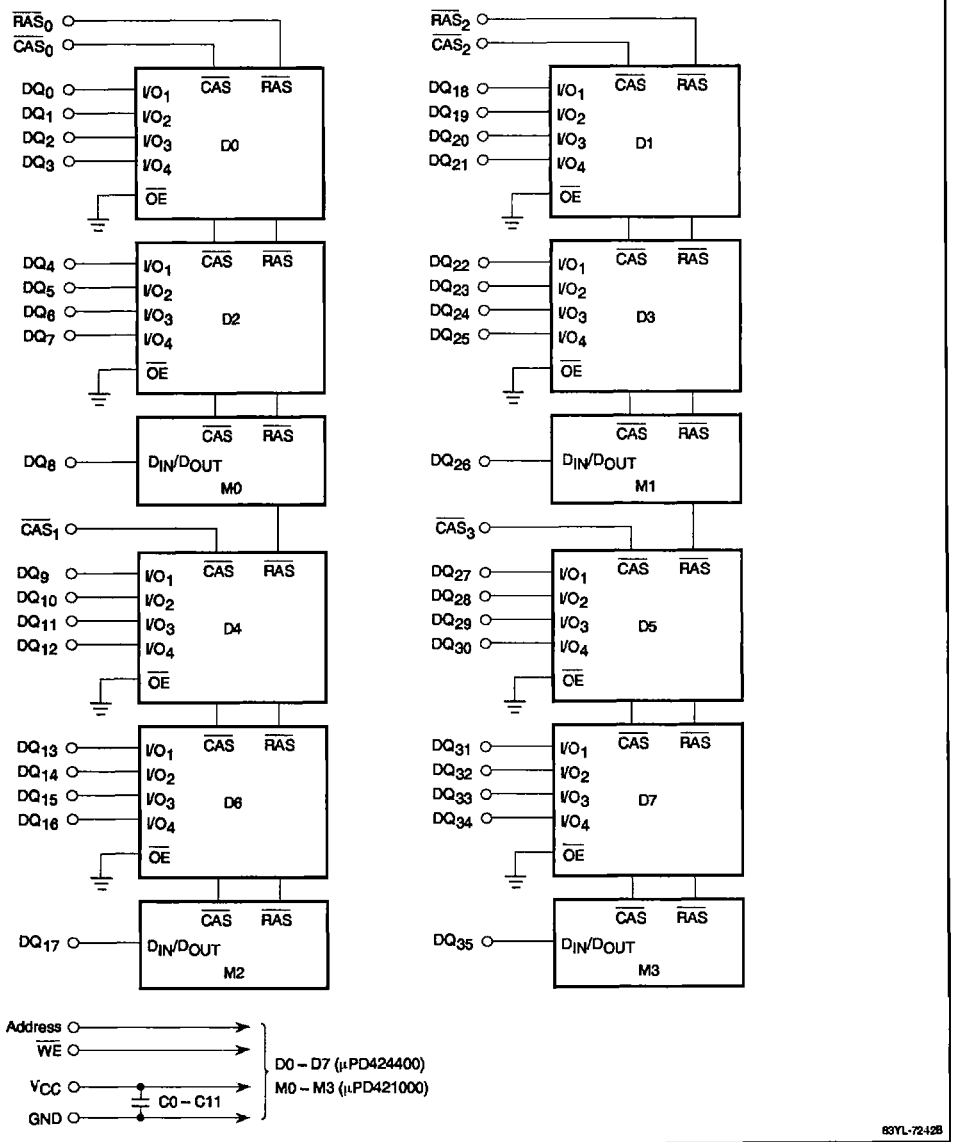
63FM-8163A

Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-421000A36B-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.0 inch)	5.28 mm (0.208 inch)	Eight μPD424400LA Four μPD421000GX
B-70	70 ns				
B-80	80 ns				
MC-421000A36F-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
F-70	70 ns				
F-80	80 ns				
MC-421000A36BD-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.0 inch)	9.3 mm (0.366 inch)	Eight μPD424400LB Four μPD421000LA
BD-70	70 ns				
BD-80	80 ns				
MC-421000A36FD-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FD-70	70 ns				
FD-80	80 ns				
MC-421000A36BE-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.0 inch)	9.3 mm (0.366 inch)	Eight μPD424400LA Four μPD421000LA
BE-70	70 ns				
BE-80	80 ns				
MC-421000A36FE-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FE-70	70 ns				
FE-80	80 ns				
MC-421000A36BH-60	60 ns	72-pin socket-mountable SIMM (solder plating)	31.75 mm (1.250 inch)	5.28 mm (0.208 inch)	Eight μPD424400LB Four μPD421000LA
BH-70	70 ns				
BH-80	80 ns				
MC-421000A36FH-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FH-70	70 ns				
FH-80	80 ns				
MC-421000A36BJ-60	60 ns	72-pin socket-mountable SIMM (solder plating)	31.75 mm (1.250 inch)	5.28 mm (0.208 inch)	Eight μPD424400LA Four μPD421000LA
BJ-70	70 ns				
BJ-80	80 ns				
MC-421000A36FJ-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FJ-70	70 ns				
FJ-80	80 ns				
MC-421000A36BT-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.0 inch)	2.68 mm (0.106 inch)	Eight μPD424400GS Four μPD421000GX
BT-70	70 ns				
BT-80	80 ns				
MC-421000A36FT-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FT-70	70 ns				
FT-80	80 ns				

10d

MC-421000A36 Connection Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	12 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	88	pF	A_0 - A_9
	C_{I2}	104	pF	$\overline{WE}$
	C_{I3}	57	pF	$\overline{RAS}$
	C_{I4}	36	pF	$\overline{CAS}$
Input/output capacitance	C_{I1}/C_{O1}	17	pF	DQ_0 - DQ_7, DQ_9 - DQ_{16}, DQ_{18} - DQ_{25}, DQ_{27} - DQ_{34}
	C_{I2}/C_{O2}	22	pF	DQ_8, DQ_{17}, DQ_{26}, DQ_{35}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		24	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			12	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−120	120	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	DQ_0 to DQ_{35} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		1320		1120		1000	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		1320		1120		1000	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$; $t_{RC} = t_{RC}$ min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		1040		920		800	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		1320		1120		1000	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; $t_{RC} = t_{RC}$ min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		30		35		40	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		17		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		0		ns	(Note 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		10		ns	
Nonpage $\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	15		15		20		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	ns	(Note 10)
Fast-page cycle time	t_{PC}	40		45		50		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Random read or write cycle time	t_{RC}	120		140		160		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		15		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		ns	
$\overline{WE}$ setup time	t_{WSR}	10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

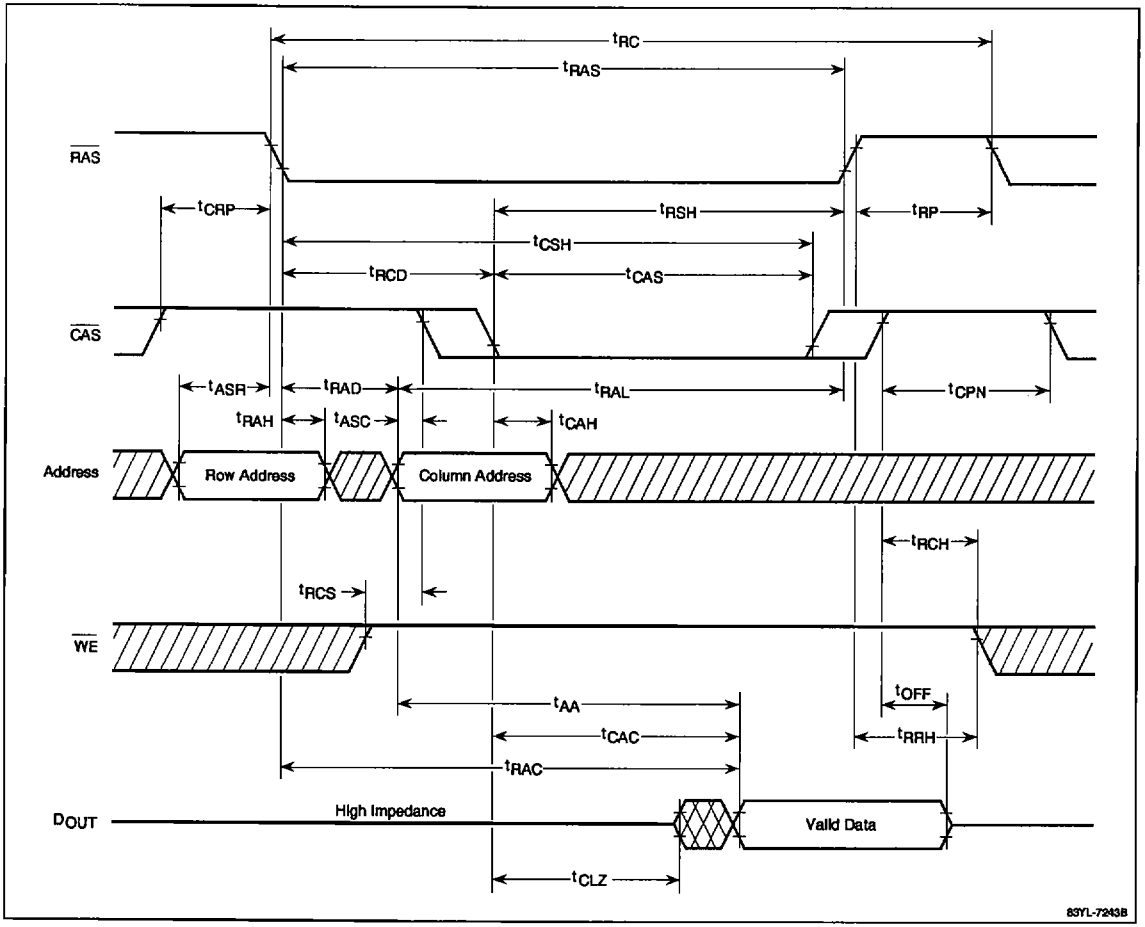
(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

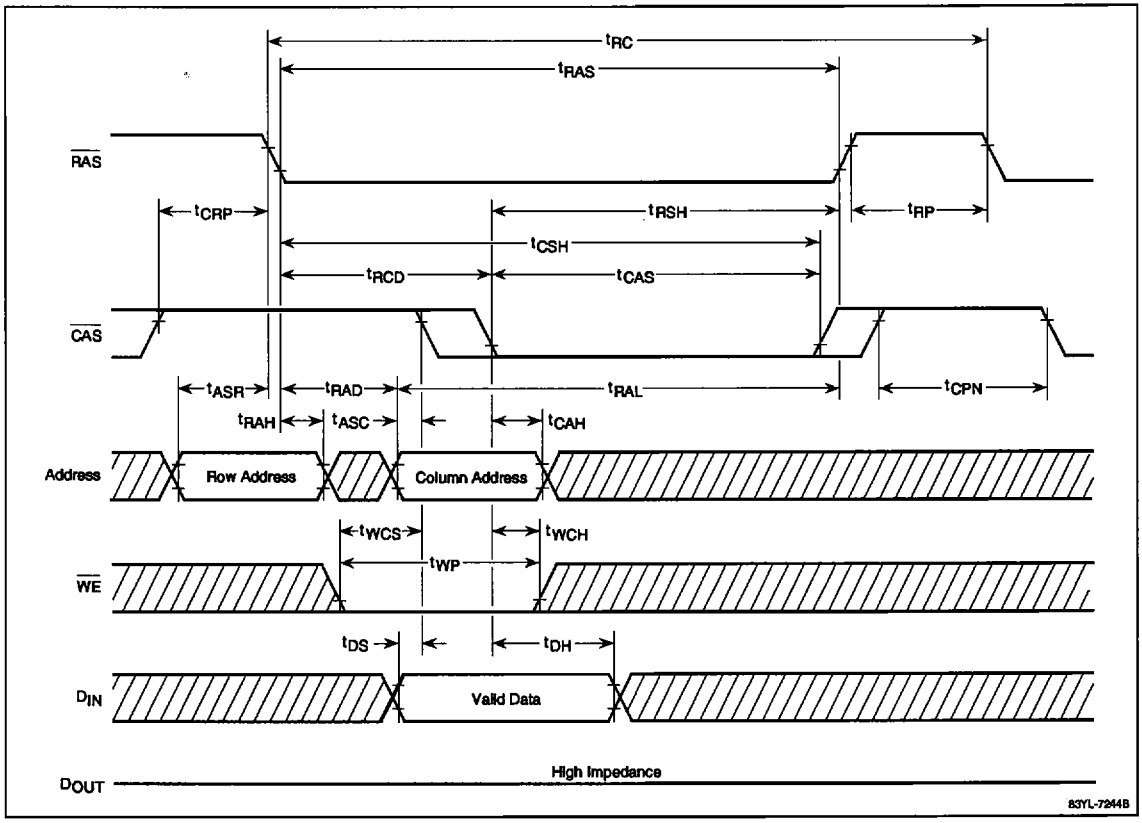
Timing Waveforms

Read Cycle



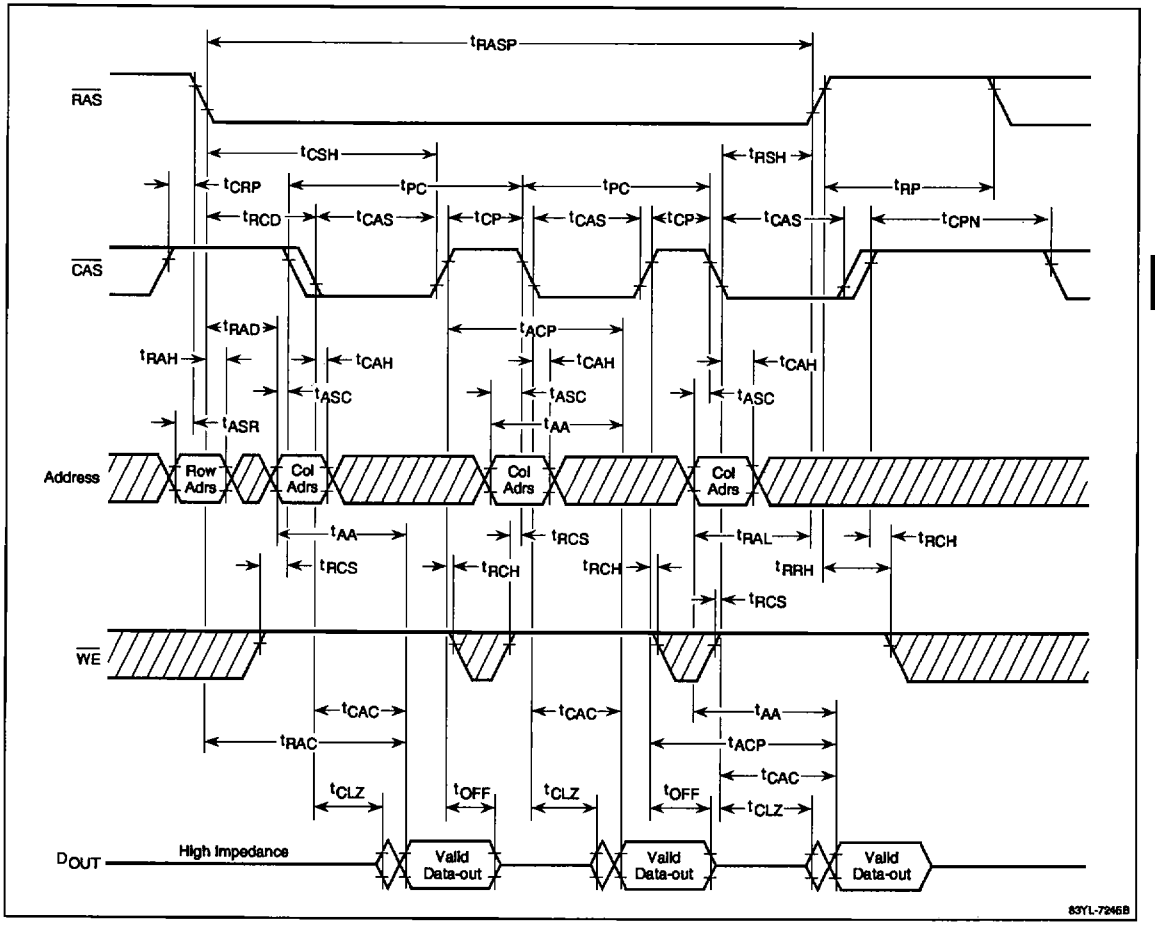
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

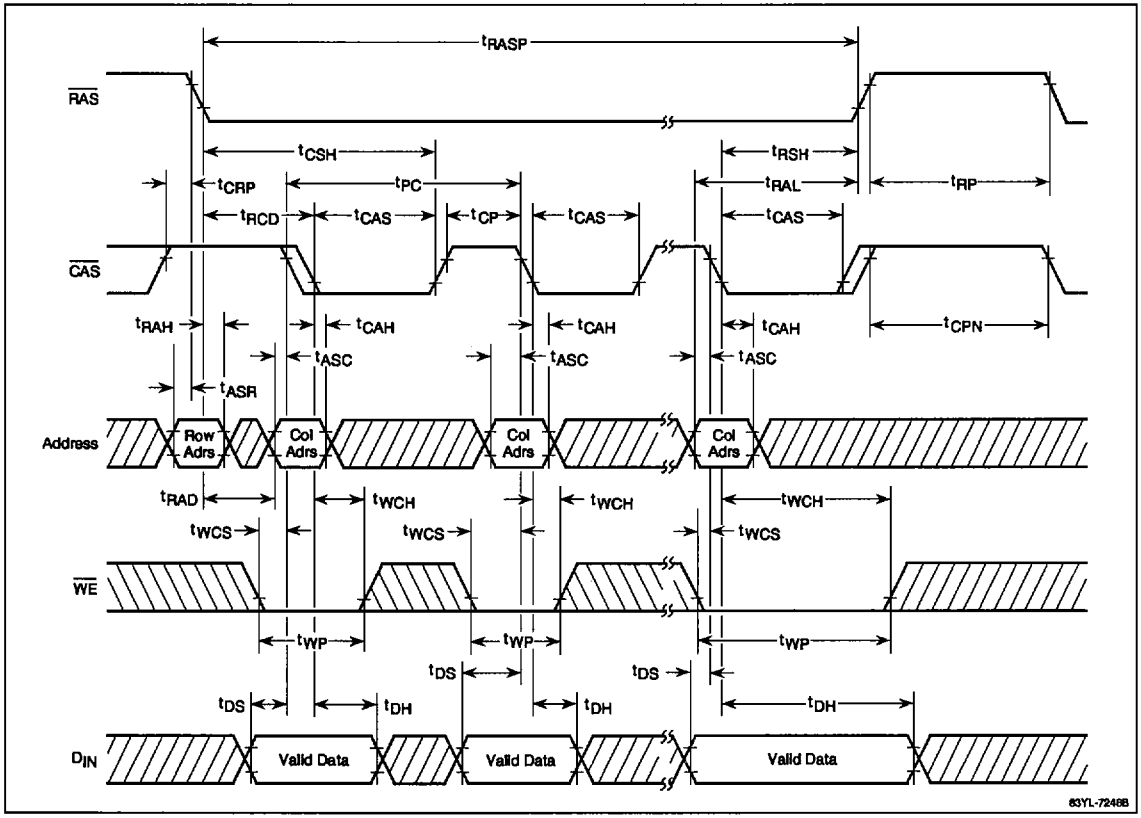
Fast-Page Read Cycle



10d

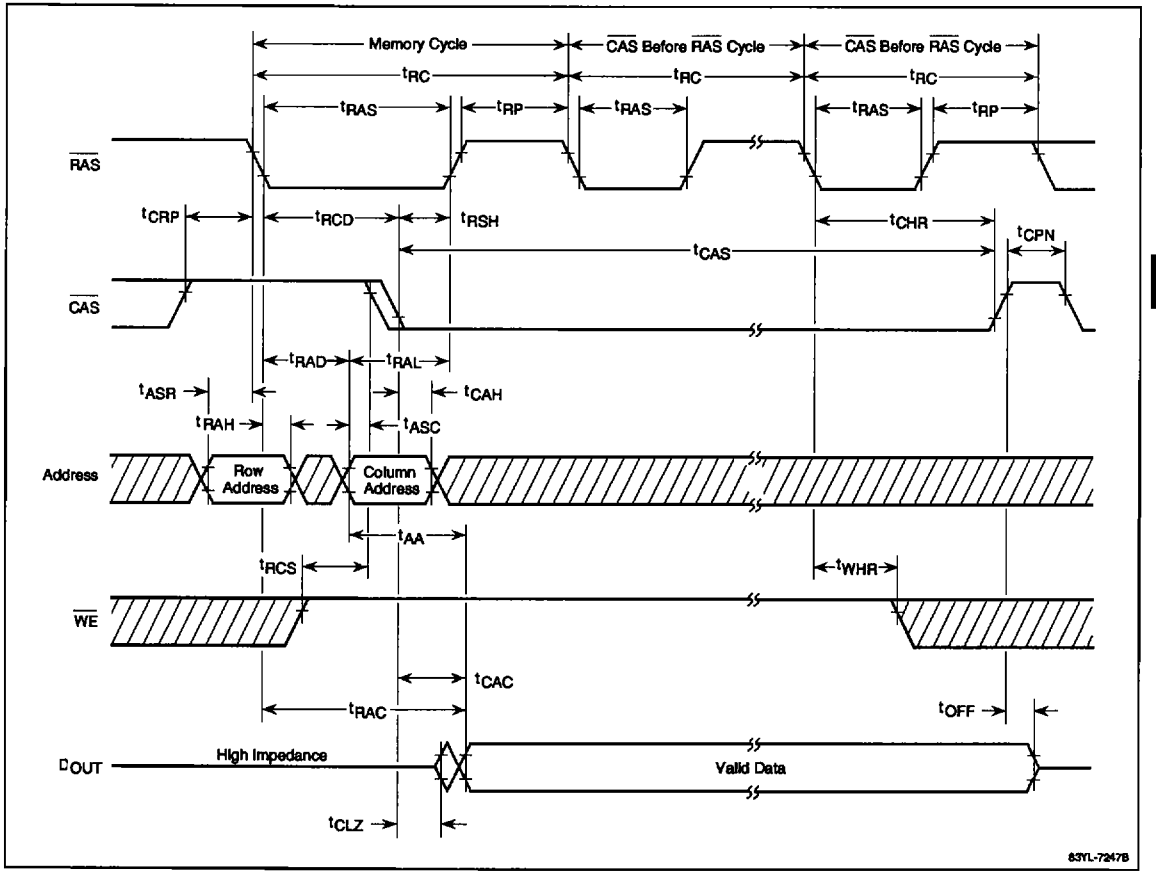
Timing Waveforms (cont)

Fast-Page Early Write Cycle



Timing Waveforms (cont)

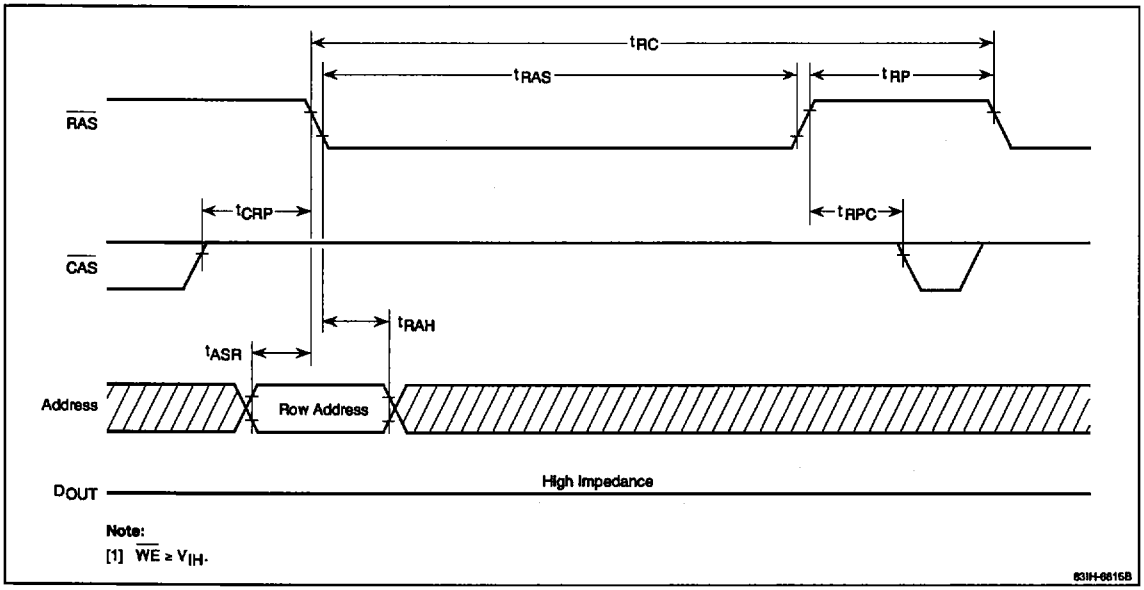
Hidden Refresh Cycle



10d

Timing Waveforms (cont)

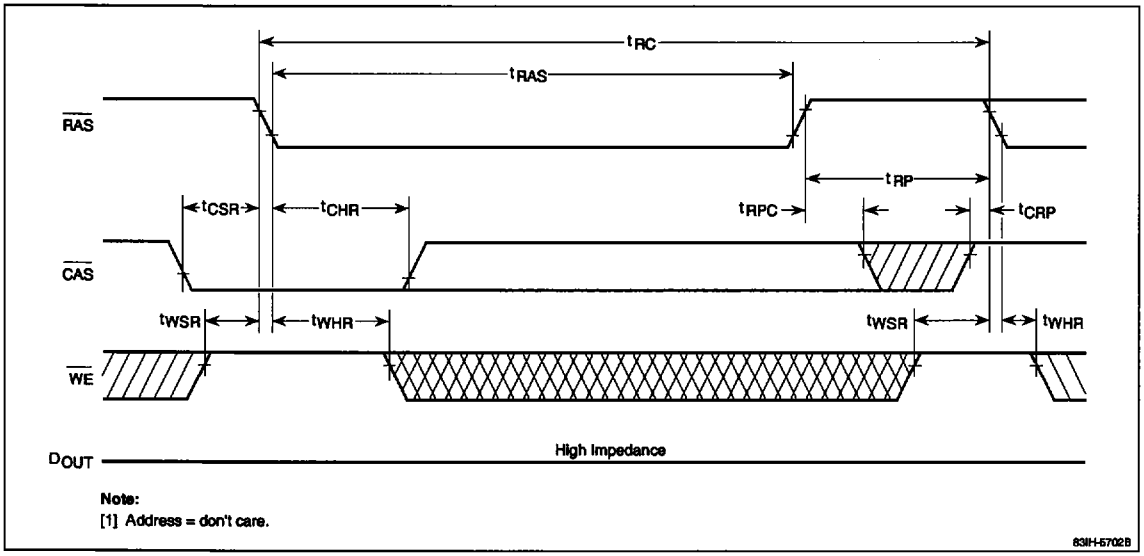
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6816B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] Address = don't care.

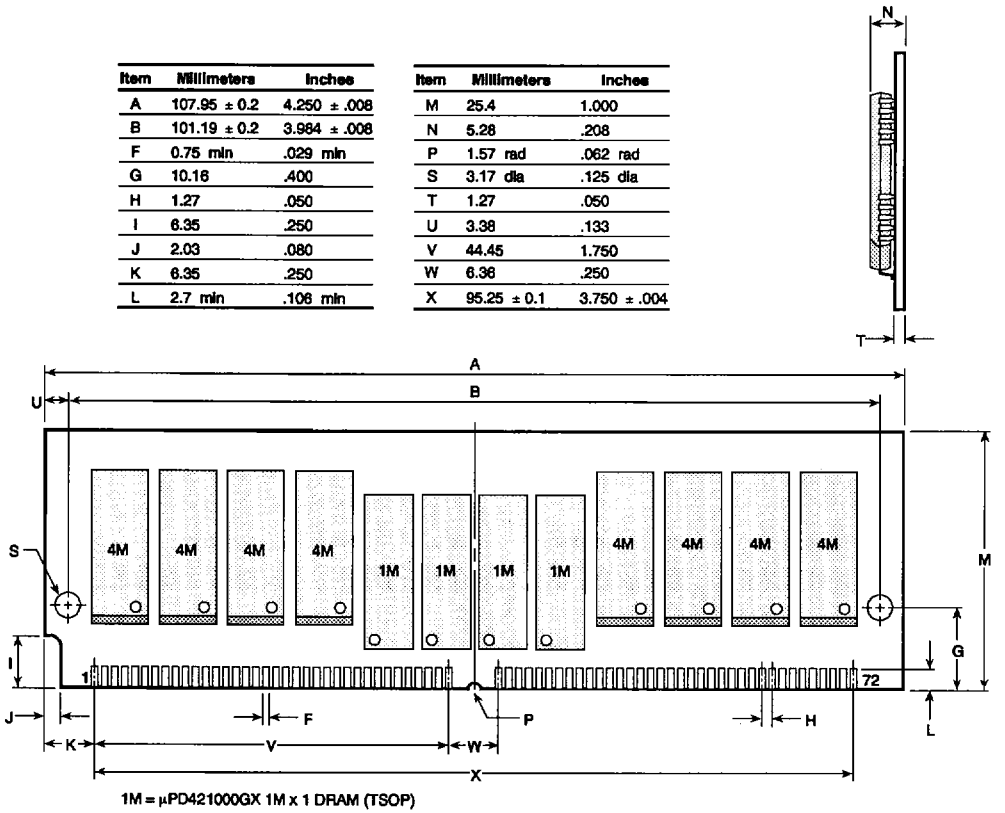
83IH-5702B

Package Drawings

72-Pin Socket-Mountable SIMM (MC-421000A36B/F)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	25.4	1.000
N	5.28	.208
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



1M = μPD421000GX 1M x 1 DRAM (TSOP)

4M = μPD424400LA 1M x 4 DRAM (300-mil SOJ)

MC-421000A36B/F

83NR-6165B (6/92)

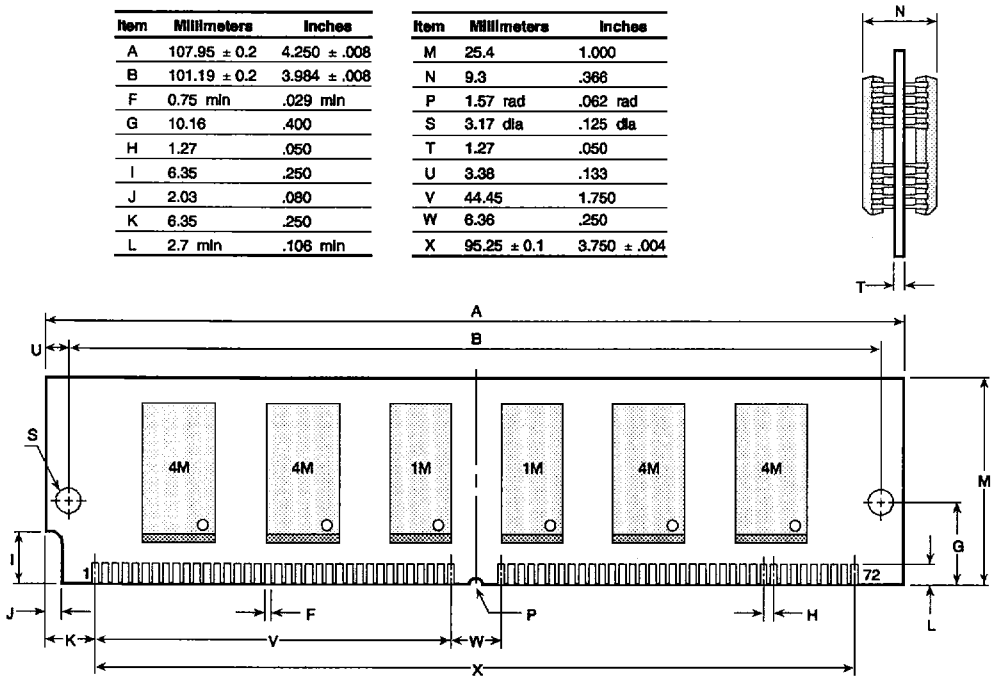
10d

Package Drawings (cont)

72-Pin Socket-Mountable SIMM (MC-421000A36BD/FD, BE/FE)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	25.4	1.000
N	9.3	.366
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



MC-421000A36	4M	1M
BD	μPD424400LB, 1M x 4 DRAM (350-mil SOJ)	μPD421000LA, 1M x 1 DRAM (300-mil SOJ)
FD		
BE	μPD424400LA, 1M x 4 DRAM (300-mil SOJ)	
FE		

MC-421000A36BD/FD

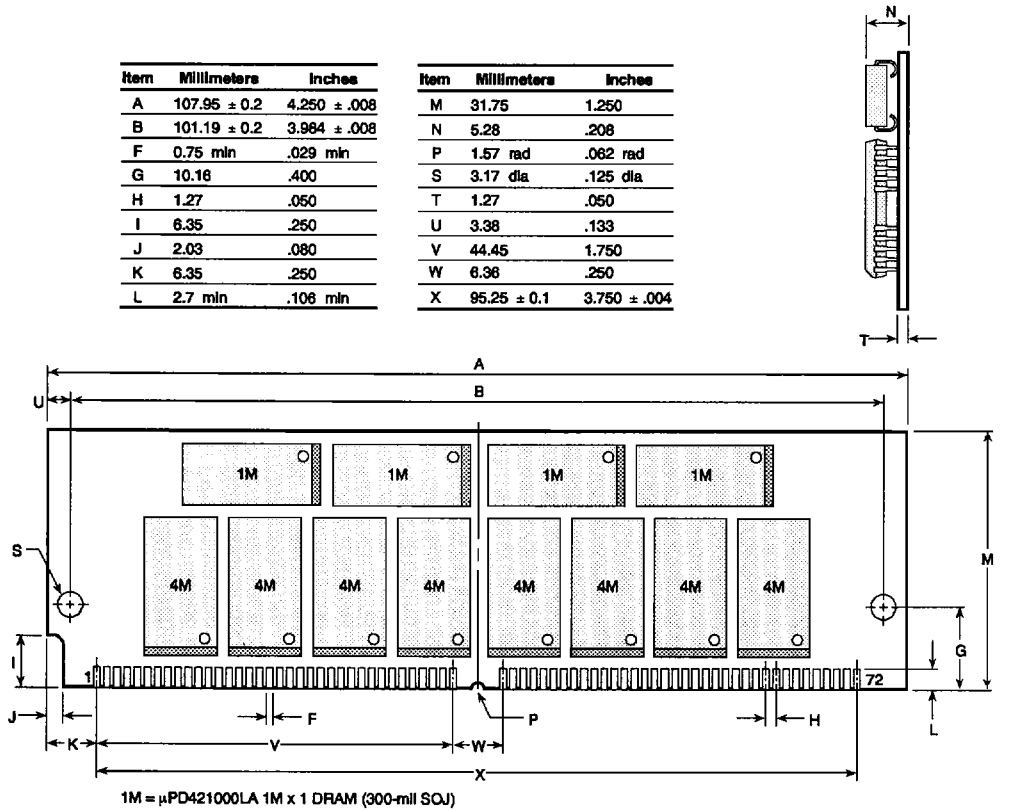
83NR-8177B (9/92)

Package Drawings (cont)

72-Pin Socket-Mountable SIMM (MC-421000A36BH/FH)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	31.75	1.250
N	5.28	.208
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



1M = μPD421000LA 1M x 1 DRAM (300-mil SOJ)
4M = μPD424400LB 1M x 4 DRAM (350-mil SOJ)

MC-421000A36BH/FH

46NR-713B (10/91)

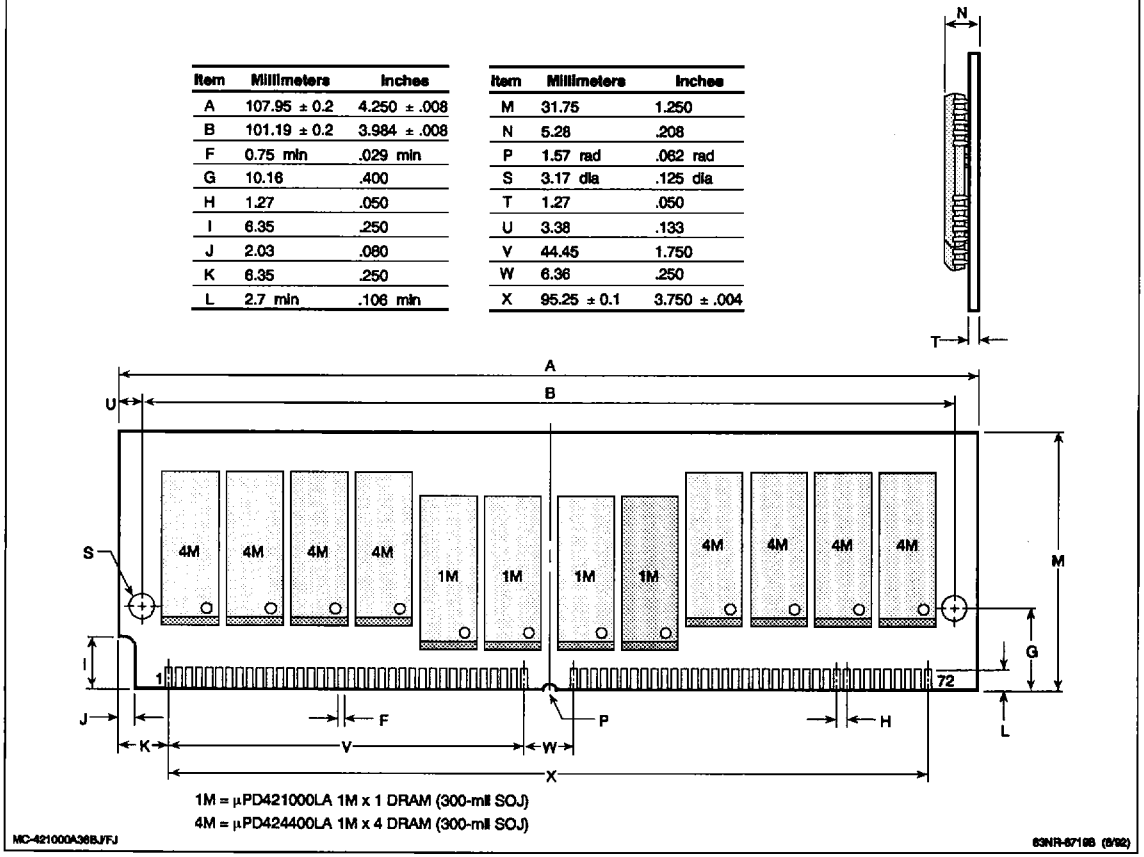
10d

Package Drawings (cont)

72-Pin Socket-Mountable SIMM (MC-421000A36BJ/FJ)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	31.75	1.250
N	5.28	.208
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



1M = μPD421000LA 1M x 1 DRAM (300-mil SOJ)
4M = μPD424400LA 1M x 4 DRAM (300-mil SOJ)

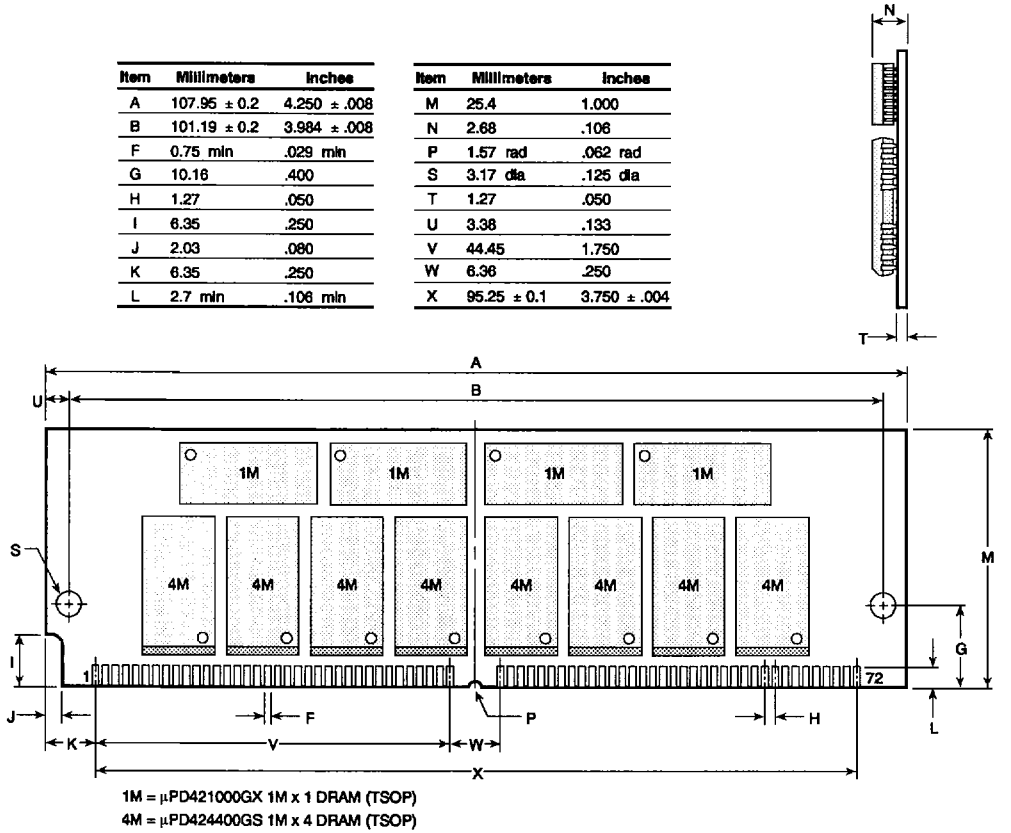
MC-421000A36BJ/FJ

Package Drawings (cont)

72-Pin Socket-Mountable SIMM (MC-421000A36BT/FT)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	25.4	1.000
N	2.68	.106
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



1M = μPD421000GX 1M x 1 DRAM (TSOP)
4M = μPD424400GS 1M x 4 DRAM (TSOP)

MC-421000A36BT/FT

49NR-8166B (10/91)

10d