PRELIMINARY

HYUNDAI SEMICONDUCTOR

HY51C1002/L

1M×1-Bit CMOS Dynamic RAM

DESCRIPTION

The HY51C1002/L is high speed, low power 1,048,576×1 bit CMOS dynamic random access memory. Fabricated with the HYUNDAI CMOS process, the HY51C1002/L offers a static column decode for high data bandwidth and clock-free page operation, fast usable speed, CMOS standby current and extended $\overline{RAS}$-only refresh for low standby power.

All inputs and outputs are TTL compatible. Input and output capacitance has been significantly lowered to allow increased system performance.

Static column operation allows random or sequential of up to 1,024 bits within a row with cycle time as short as 55ns. Because of completely static circuitry, $\overline{CS}$ is not required to either clock or gate the column addresses and, since $\overline{CS}$ is not in the critical access time path, system design is easier, and inherent device speed is more usable. These features make the HY51C1002/L ideal for computer peripherals and control systems.

When $\overline{RAS}$ is ≥ $V_{DD}-0.2V$, CMOS standby operation mode is active, and power drops to 1.5 mW (typically).

FEATURES

- **Low power dissipation for the HY51C1002L**
  - **-Operating Current, −12 : 70 mA (max.)**
  - **-TTL Standby Current : 2.5 mA (max.)**
  - **-CMOS Standby Current : 1.5 mA (max.)**
- **Read-Modify-Write, $\overline{RAS}$-only Refresh, and $\overline{CS}$-before-$\overline{RAS}$ refresh capability.**
- **Common I/O capability.**
- **Static Column Mode Operation – Continuous data rate up to 18 MHz**
- **512 refresh cycles/8ms**
- **High reliability 18 pin 300 mil P-DIP, 26/20 pin SOJ**
- **Fast access time and cycle time (ns)**

	HY51C1002/L-85	HY51C1002/L-10	HY51C1002/L-12
Max $\overline{RAS}$ Access Time, t_{RAC}	85	100	120
Max Column Address Access Time, t_{CAA}	40	45	55
Min Static Column Mode Cycle Time, t_{SRC}, t_{SWC}	55	60	70
Min Cycle Time, t_{RC}	160	190	220

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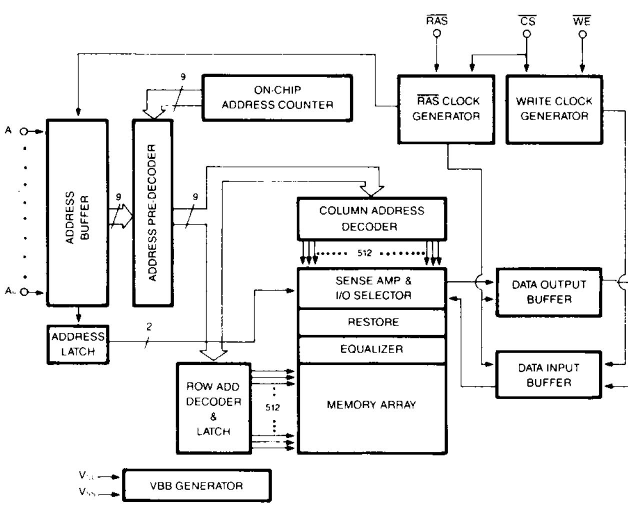
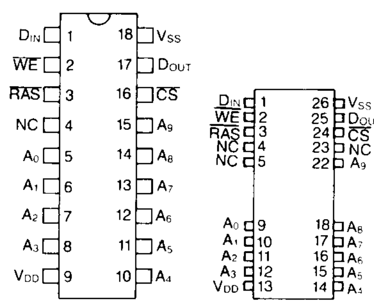
BLOCK DIAGRAM



PIN CONNECTIONS



(P-DIP) (SOJ)

PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CS}$	CHIP SELECT
$\overline{WE}$	WRITE ENABLE
A_0—A_9	ADDRESS INPUT
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{DD}	POWER (+5V)

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_{BIAS}	Ambient Temperature Under Bias	−10 to + 80	°C
T_{STG}	Storage Temperature (Plastic)	−55 to +125	°C
V_{TERM}	Voltage on Any Pin Except V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OUT}	Data Out Current	50	mA
P_T	Power Dissipation	1.0	W

NOTE:
1. Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

DC CHARACTERISTICS

(T_A = 0°C to +70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY51C1002/L MIN.	HY51C1002/L MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$			10	μA	
I_{LO}	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}			10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC} = t_{RC}$ (min.)	−85		95	mA	1,2
			−10		75		
			−12		70		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH}, other inputs $\geq V_{SS}$			4/2.5	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC} = t_{RC}$ (min.)	−85		95	mA	2
			−10		75		
			−12		70		
I_{DD4}	V_{DD} Supply Current, Static Column Mode	Minimum Cycle	−85		50	mA	2
			−10		40		
			−12		35		
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled	$\overline{RAS} = V_{IH}$, $\overline{CS} = V_{IL}$, other inputs $\geq V_{SS}$			4/2.5	mA	1
I_{DD6}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \geq V_{DD} - 0.2V$, $\overline{CS} = V_{IH}$, other inputs $\geq V_{SS}$			3/1.5	mA	
V_{IL}	Input Low Voltage (all inputs)			−0.5	0.8	V	3
V_{IH}	Input High Voltage (all inputs)			2.4	$V_{DD}+1$	V	3
V_{OL}	Output Low Voltage	$I_{OL} = 4.2mA$			0.4	V	
V_{OH}	Output High Voltage	$I_{OH} = -5mA$		2.4		V	

NOTES:
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) measured with output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in static column mode.
3. Specified V_{IL} (min.) is steady state operation. During transitions, V_{IL} may undershoot to −1.0V for a period not to exceed 20ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.

AC CHARACTERISTICS
(T_A = 0°C to +70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY51C1002/L-85		HY51C1002/L-10		HY51C1002/L-12		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	85	85K	100	85K	120	85K	ns	
2	t_{RC}	Random Read or Write Cycle Time	160		190		220		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	65		80		90		ns	
4	t_{ASR}	Row Address Set-up Time	0		0		0		ns	
5	t_{RAH}	Row Address Hold Time	15		15		20		ns	
6	t_{CAR}	Column Address to $\overline{RAS}$ Set-up Time	40		45		55		ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	45	20	55	25	65	ns	1
8	t_{ARH}	Column Address Hold Time to $\overline{RAS}$	5		5		5		ns	
9	t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay	25	65	25	75	30	90	ns	2
10	t_{RAC}	Access Time From $\overline{RAS}$		85		100		120	ns	3,4,5
11	t_{CAA}	Access Time From Column Address		40		45		55	ns	5,6
12	t_{CAC}	Access Time From $\overline{CS}$		20		25		30	ns	5
13	$t_{CAS(R)}$	$\overline{CS}$ Pulse Width in Read Cycle	20		25		30		ns	
14	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	20		25		30		ns	
15	t_{RCS}	Read Command Set-up Time	0		0		0		ns	
16	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5		5		5		ns	7
17	t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	15		15		15		ns	
18	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	25	0	30	ns	8
19	t_{OH}	Output Data Hold Time From $\overline{CS}$	0		0		0		ns	8
20	t_{AWS}	Column Address to Write Command Set-up Time	0		0		0		ns	
21	t_{AWH}	Column Address to Write Command Hold Time	15		20		25		ns	
22	t_{ARW}	Column Address Hold Time From $\overline{RAS}$ (Write)	60		70		80		ns	
23	$t_{CAS(W)}$	$\overline{CS}$ Pulse Width in Write Cycle	25		30		35		ns	
24	$t_{RSH(W)}$	$\overline{RAS}$ Hold Time (Write Cycle)	25		30		35		ns	
25	t_{WCR}	Write Command Hold Time From $\overline{RAS}$	60		70		80		ns	
26	t_{WCS}	Write Command Set-up Time	0		0		0		ns	9,10
27	t_{WHC}	Write Command Hold Time Referenced to $\overline{CS}$	0		0		0		ns	9,11
28	t_{WHR}	Write Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	9,11
29	t_{DS}	Data-In Set-up Time	0		0		0		ns	12
30	t_{DH}	Data-In Hold Time	15		20		25		ns	12
31	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	60		70		80		ns	
32	t_{RWC}	RMW Cycle Time	190		225		260		ns	
33	t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	115		135		160		ns	
34	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in RMW Cycle	85		100		120		ns	9
35	t_{CWD}	$\overline{CS}$ to $\overline{WE}$ Delay	20		25		30		ns	9
36	t_{AWD}	Column Address to $\overline{WE}$ Delay	40		45		55		ns	9
37	t_{ARR}	Column Address Hold Time From $\overline{RAS}$ (Read)	85		100		120		ns	
38	t_{RCH}	Read Command Hold Time Referenced to $\overline{CS}$	5		5		5		ns	7

#	SYMBOL	PARAMETER	HY51C1002/L-85		HY51C1002/L-10		HY51C1002/L-12		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
39	t_{SRC}	Static Column Mode Read Cycle Time	55		60		70		ns	
40	t_{OHA}	Output Hold Time From Address Change	0		0		0		ns	
41	t_{CP}	$\overline{CS}$ Precharge Time	20		25		30		ns	
42	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25		30		35		ns	
43	t_{SWC}	Static Column Mode Write Cycle Time	55		60		70		ns	
44	t_{WP}	Write Pulse Width	20		25		30		ns	
45	t_{WRA}	Write Read Access Time		95		105		125	ns	13
46	t_{WPA}	Write Precharge Access Time		20		25		30	ns	13
47	t_{WOH}	Output Data Hold Time From $\overline{WE}$	0		0		0		ns	
48	t_{CSR}	$\overline{CS}$ Set-up Time ($\overline{CS}$ Before $\overline{RAS}$ Cycle)	10		10		10		ns	
49	t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ Before $\overline{RAS}$ Cycle)	25		30		40		ns	
50	t_{RPC}	$\overline{RAS}$ to $\overline{CS}$ Precharge Time	0		0		0		ns	
51	t_{CWL}	Write Command to $\overline{CS}$ Lead Time	25		30		35		ns	
52	t_{CSH}	$\overline{CS}$ Hold Time	85		100		120		ns	
53	t_T	Transition Time (Rise and fall)	3	25	3	25	3	25	ns	14,15
54	t_{RI}	Refresh Interval (512 Cycle)		8		8		8	ms	16

NOTES:

1. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RAD} (max.) is specified as a referenced point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then the access time is controlled by t_{CAA} and t_{CAC}.
2. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) and t_{RAD} (max.) limit insure that t_{RAC} (max.), t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.) then the access time is controlled by t_{CAA} and t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
4. Assume $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
5. Measured with a load equivalent to two TTL loads and 100 PF.
6. Assume $t_{RAD} \geq t_{RAD}$ (max.).
7. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
8. t_{OFF} and t_{OH} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
9. t_{WCS}, t_{WHC}, t_{RWD}, t_{AWD}, t_{CWD} are not restrictive operating parameters.
10. t_{WCS} (min.) must be satisfied in the early write cycle.
11. Either t_{WHC} (min.) or t_{WHR} (min.) must be satisfied in the early write cycle and read-modify write cycle.
12. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CS}$ or $\overline{WE}$.
13. Access time is determined by the longer of t_{CAA} or t_{WPA}.
14. t_T is measured between V_{IH} (min.) any V_{IL} (max.).
15. AC measurements assume $t_T = 5$ ns.
16. An initial pause of 200 μs is required after power-up and followed by a minimum of 8 initialitation cycle (any combination of cycles containing a $\overline{RAS}$ clock such as a $\overline{RAS}$-only Refresh). Eight initialization cycles are required after extended period of bias without clocks.

CAPACITANCE(1)

($T_A = 25°C$, $V_{SS} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.)

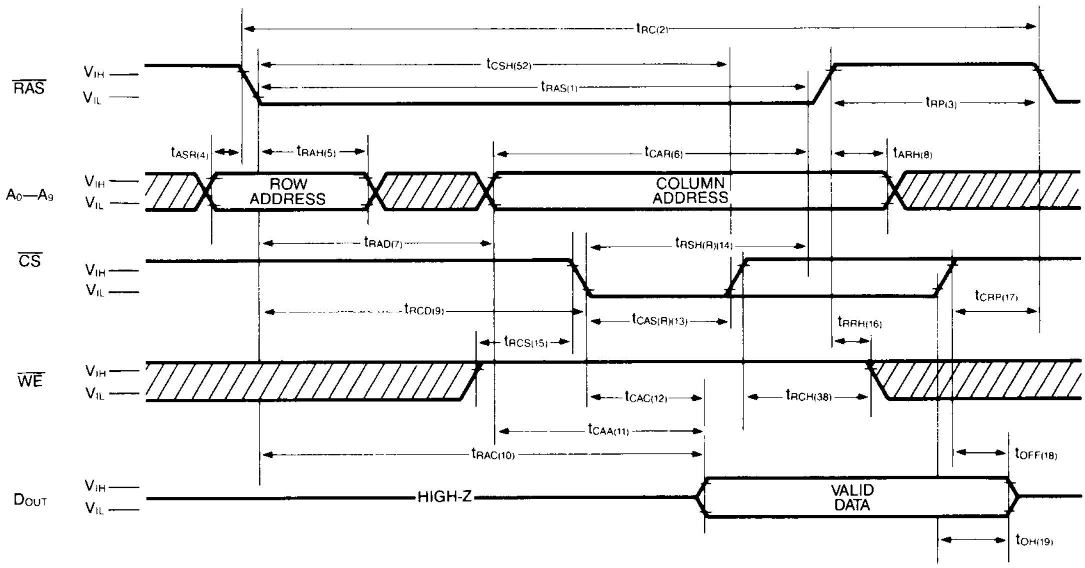
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Address, Data In	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CS}$, $\overline{WE}$	4	5	pF
C_{OUT}	Data Out	4	6	pF

NOTE:

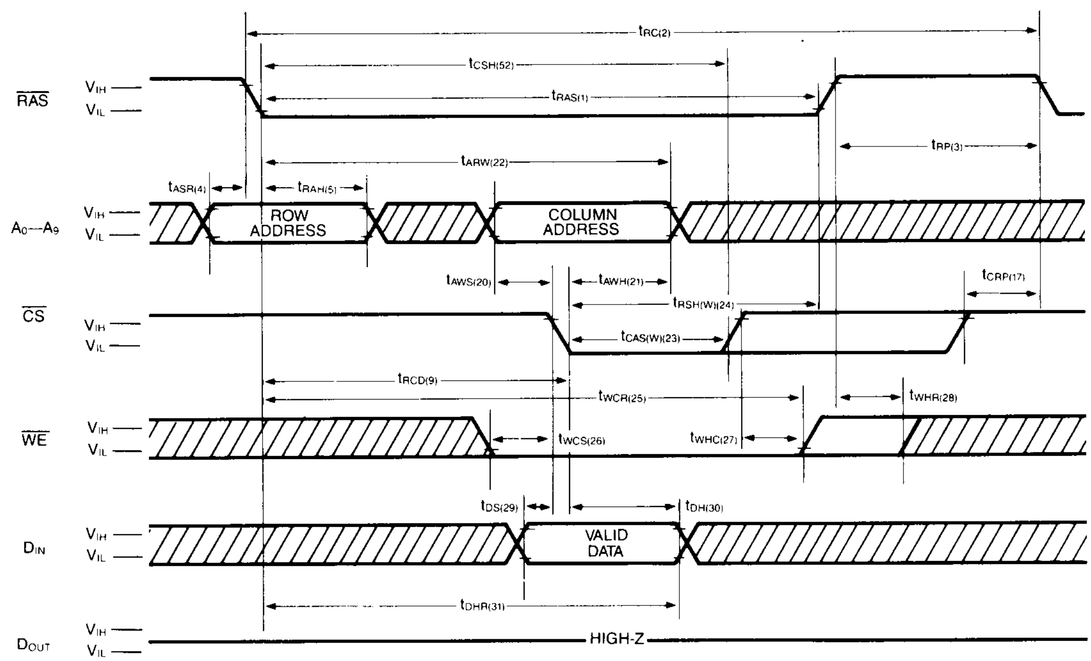
1. Capacitance is measured at worst case voltage levels with a programmable capacitance meter.

TIMING DIAGRAMS

READ CYCLE



ERALY WRITE CYCLE



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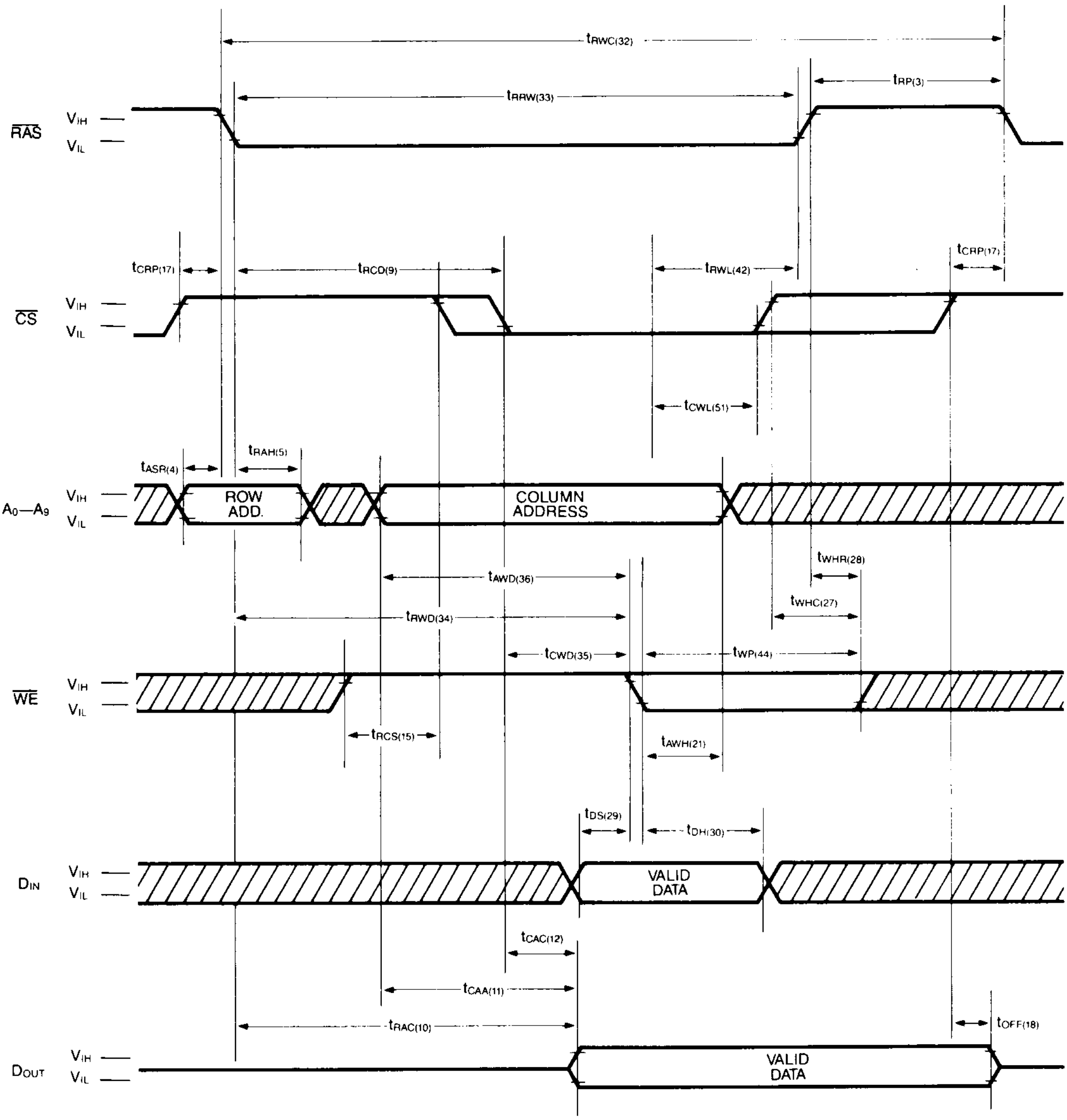
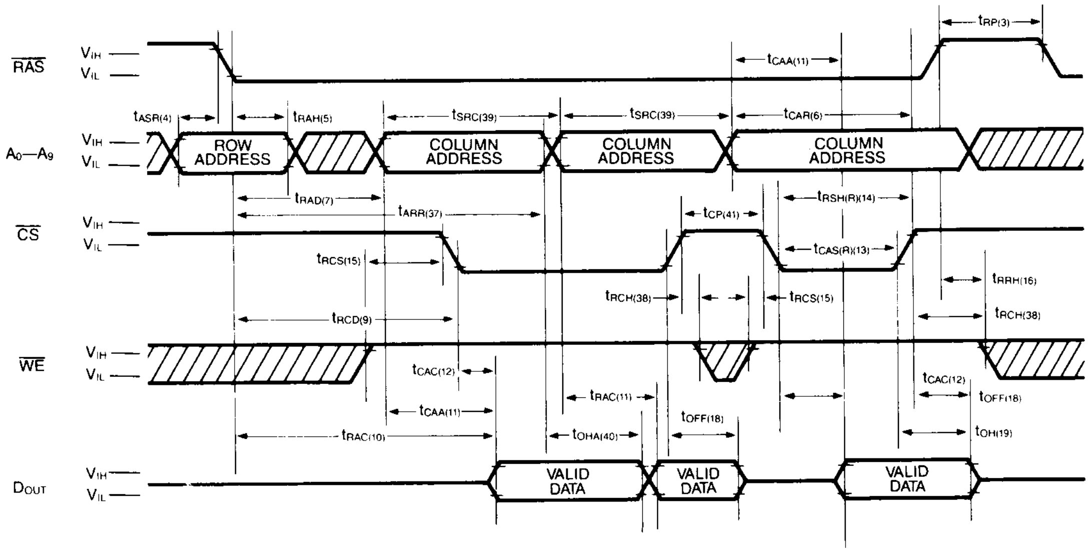
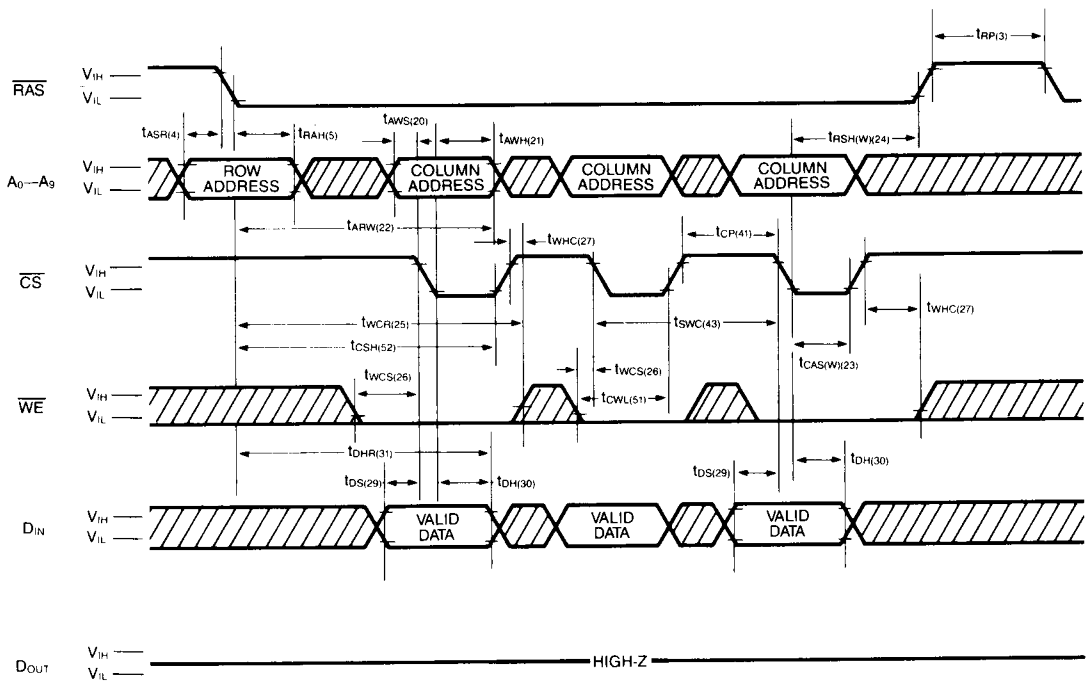
READ-MODIFY-WRITE CYCLE



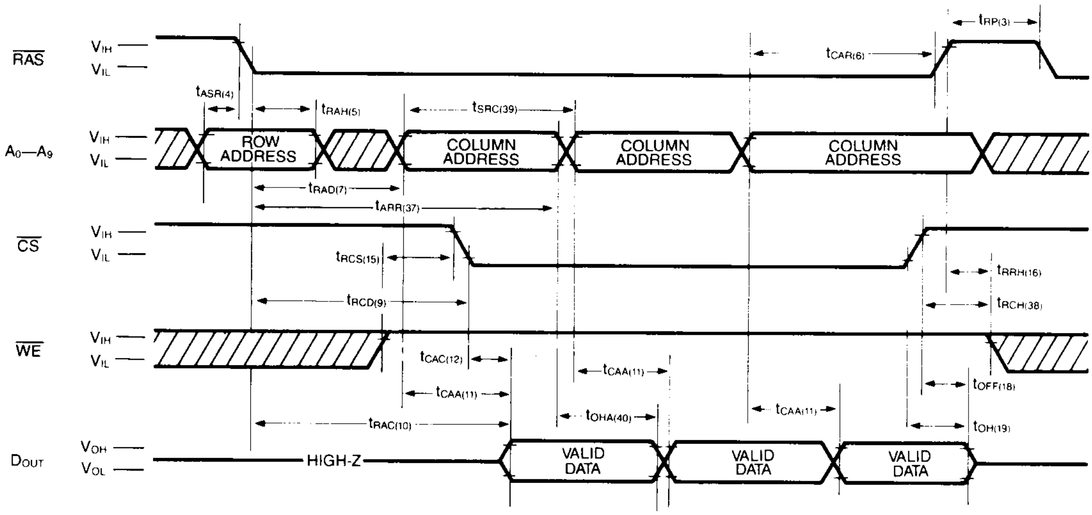
STATIC COLUMN MODE READ CYCLE ($\overline{CS}$ CONTROLLED)



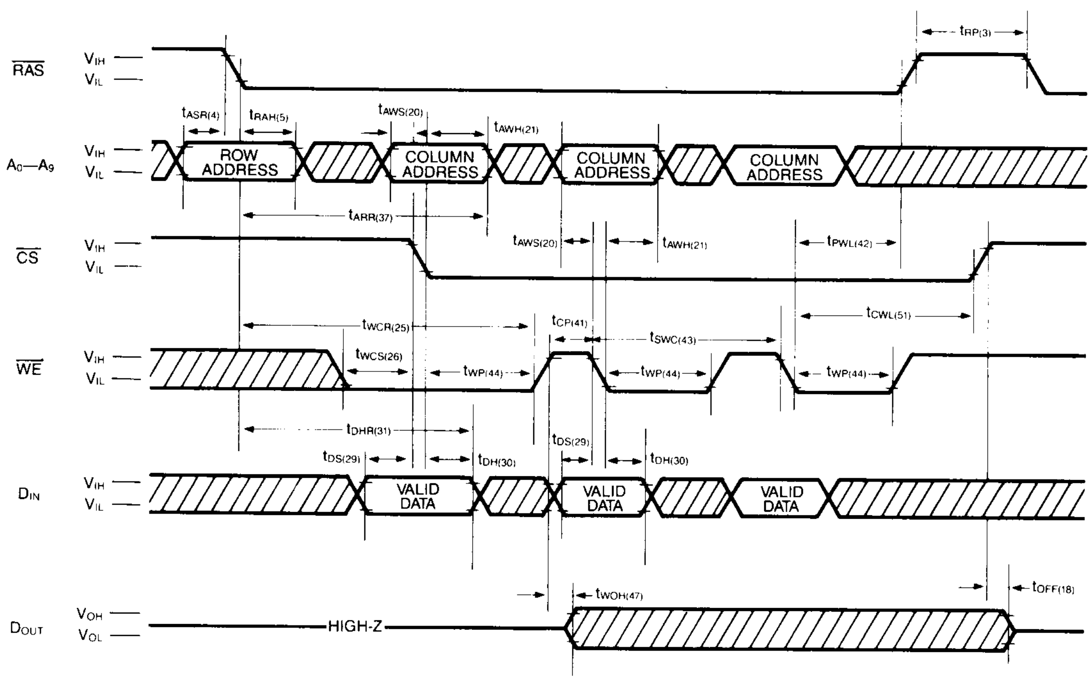
STATIC COLUMN MODE EARLY WRITE CYCLE ($\overline{CS}$ CONTROLLED)



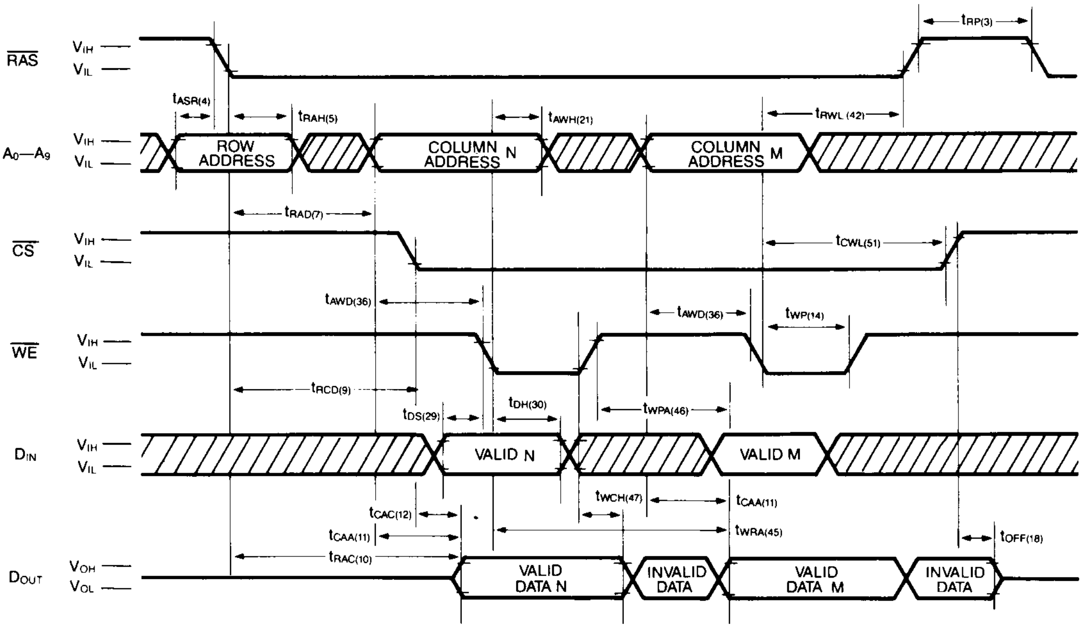
STATIC COLUMN MODE READ CYCLE (WE CONTROLLED)



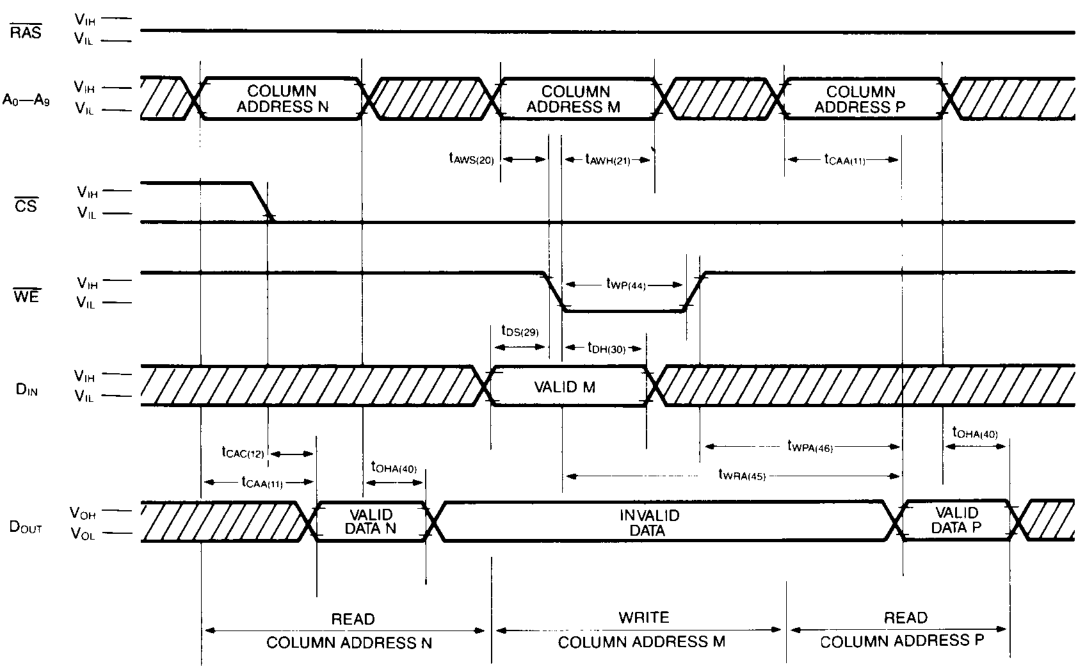
STATIC COLUMN MODE EARLY WRITE CYCLE (WE CONTROLLED)



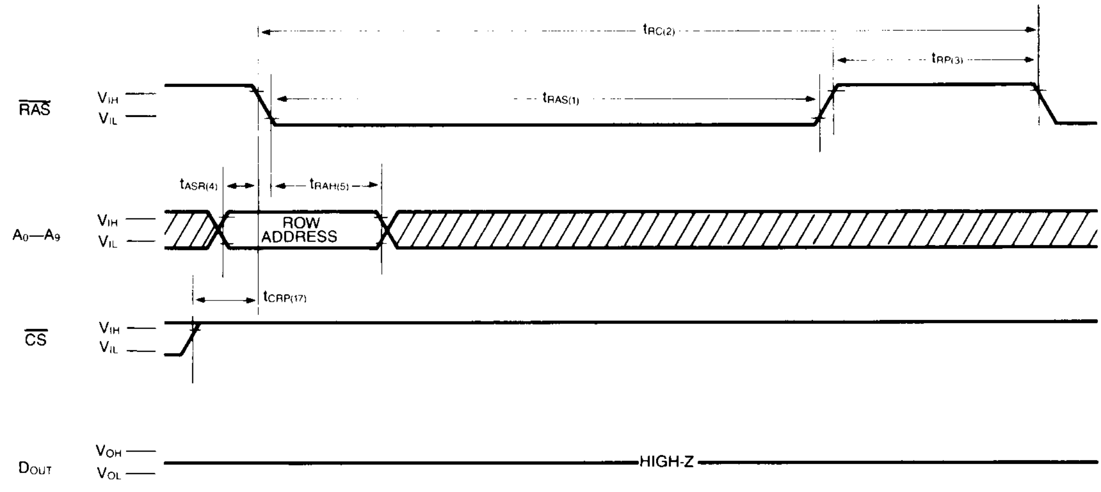
STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



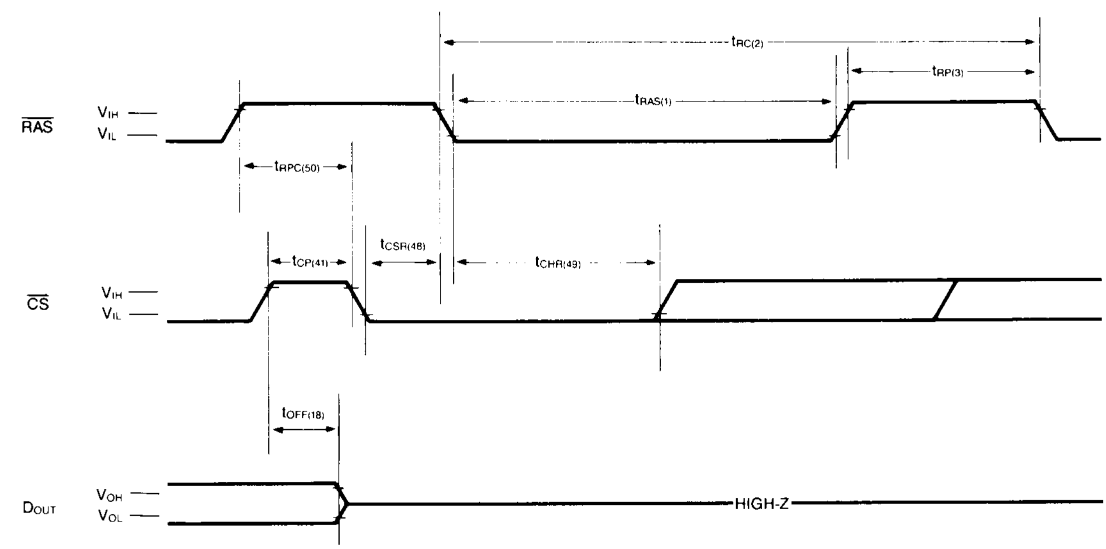
STATIC COLUMN MODE READ-WRITE-READ CYCLE



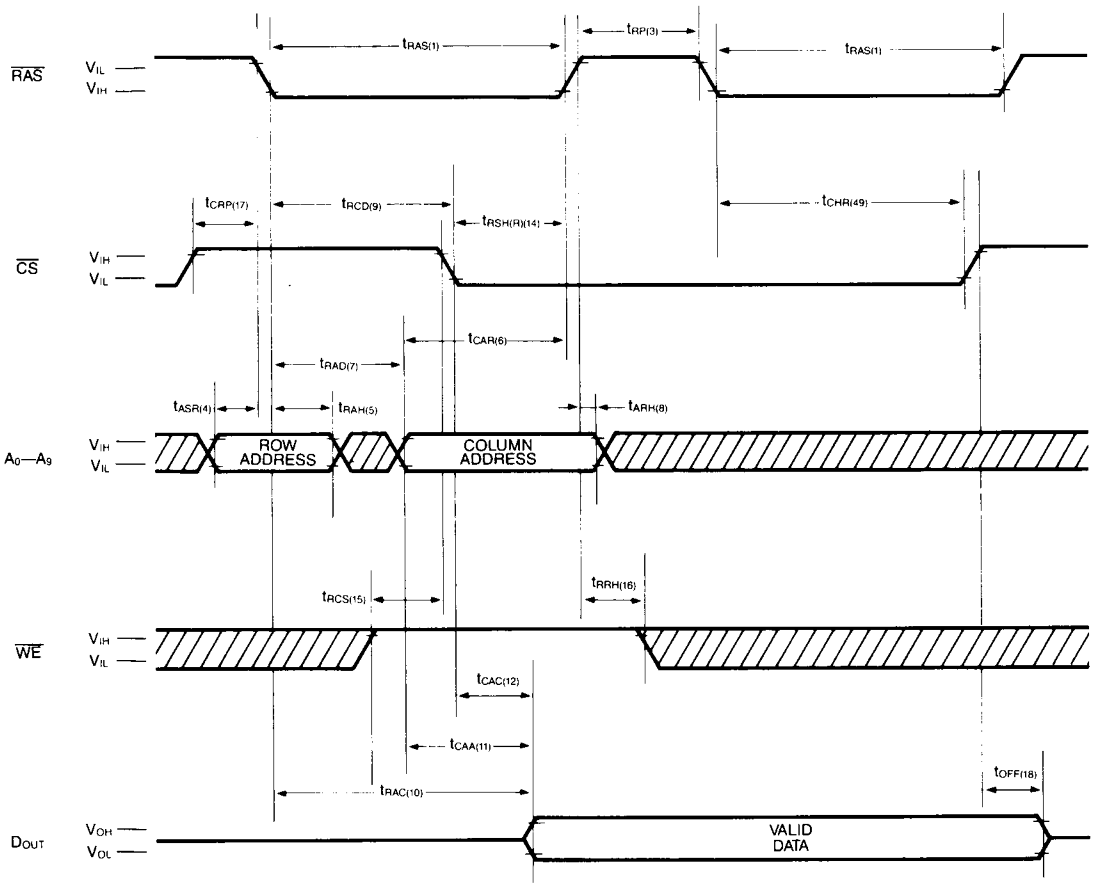
$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE (READ)



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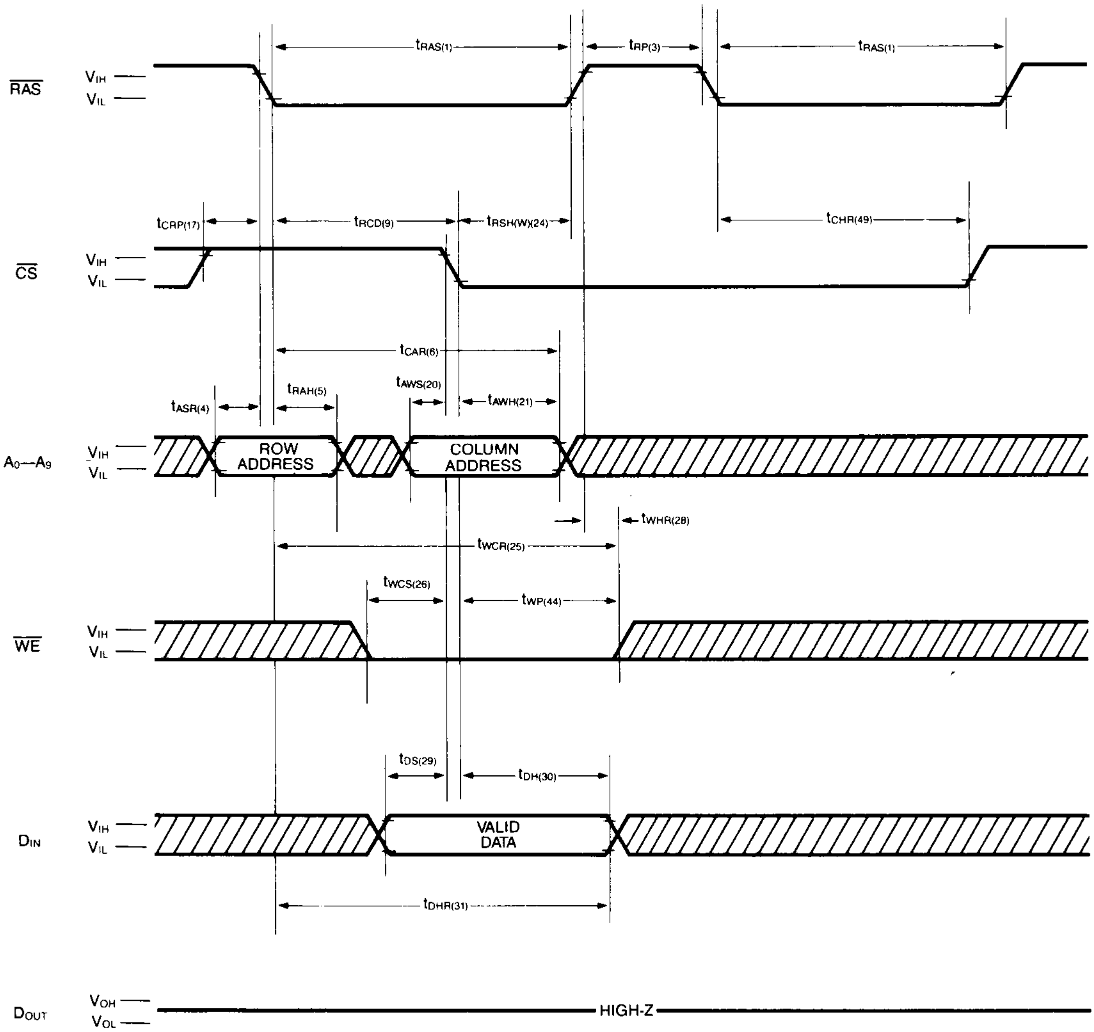
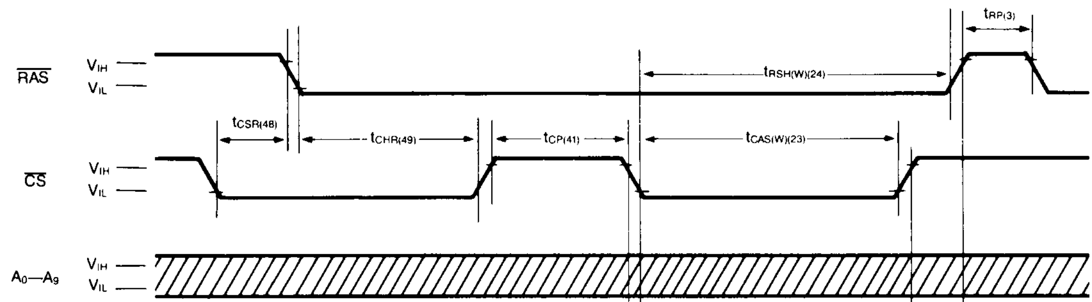
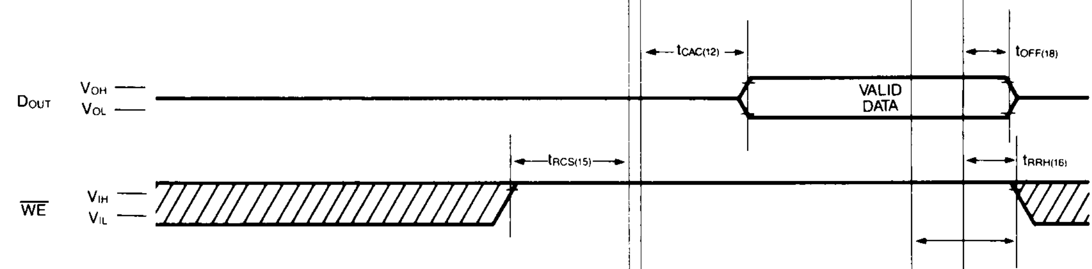
HIDDEN REFRESH CYCLE (WRITE)



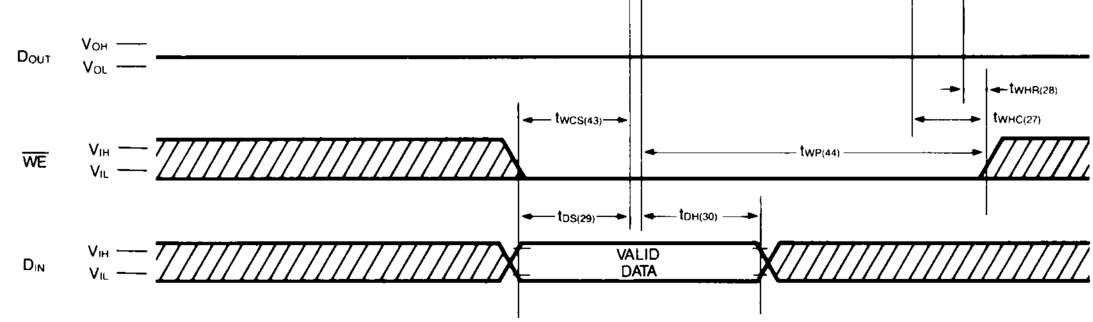
$\overline{\text{CS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



READ CYCLE



WRITE CYCLE



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FUNCTIONAL DESCRIPTION

The HY51C1002/L is CMOS dynamic RAM optimized for high data bandwidth and low power applications. The functionality is similar to a traditional dynamic RAM. The HY51C1002/L reads and write one bit of data at a time by multiplexing 20 bit address into 10 bit row and 10 bit column address. The row address is latched in by the Row Address Strobe ($\overline{RAS}$). The column address, however, is only latched during a write cycle by the later of either chip select ($\overline{CS}$) or write enable ($\overline{WE}$). During the read cycle, the column address is not latched and continuously flows through the internal input latches. Access time is primarily dependent on a valid column address. $\overline{CS}$ acts as output enable signal in the access path.

MEMORY CYCLE

The memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle can not be initiated until the minimum precharge time, t_{RP}, has elaspsed.

READ CYCLE

A read cycle is performed by holding the Write Enable ($\overline{WE}$) signal high during a $\overline{RAS}/\overline{CS}$ operation. The column address is not latched and must be held valid until data output becomes valid. Data output becomes valid only when t_{RAC}, t_{CAC}, and t_{CAA} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC}, t_{CAC} and t_{CAA}. For example, the access time is limited by t_{CAA} when t_{RAC} and t_{CAC} are both satisfied.

WRITE CYCLE

A write cycle is performed by taking $\overline{WE}$ and $\overline{CS}$ low during a $\overline{RAS}$ operation. The column address is latched in the latter of $\overline{WE}$ or $\overline{CS}$. The input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CS}$ whichever occurs last. Consequently, the write cycle can be $\overline{WE}$ controlled or $\overline{CS}$ controlled depending upon the latter of $\overline{WE}$ or $\overline{CS}$ low transition. In a $\overline{CS}$ controlled write cycle (the leading edge of $\overline{WE}$ occurs prior to or coincident with $\overline{CS}$ transition), the data output pin will be in the high impedence state at the beginning of the write function. Terminating the write action with $\overline{CS}$ going high will maintain the data output pin in the high impedence state. Terminating the write action with $\overline{WE}$ going high allows the output to go active and starts the read action (read after write). $\overline{WE}$ going high will release the column address and data input latch, then sample the new column address and start the read action. The user has total control of read and write action by $\overline{WE}$ timing.

REFRESH CYCLE

To retain data, 512 $\overline{RAS}$ refresh cycles are required in an 8 ms period. The refresh operation can be performed two ways:

1. Clocking each of 512 row address (A_0 through A_8) with $\overline{RAS}$ at least every 8 ms period. Any combination of $\overline{RAS}$ cycle such as read, write, read-modify-write, or $\overline{RAS}$-only refresh cycle will perform a refresh on the selected row.
2. $\overline{CS}$-before-$\overline{RAS}$ refresh cycle
   If $\overline{CS}$ go low prior to $\overline{RAS}$ go low, the chip enters a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle. In a $\overline{CS}$ before-$\overline{RAS}$ refresh cycle the HY51C1002/L will use an internal nine-bit counter output as the source of the row address and will ignore the external address input.

In $\overline{CS}$-before-$\overline{RAS}$ refresh mode is a refresh only mode and no data access is allowed. Also, the $\overline{CS}$-before-$\overline{RAS}$ refresh cycle does not cause device selection and the state of the data output pin will remain in a high impedence state.

In order to guarantee the reliable operation of the $\overline{CS}$-before-$\overline{RAS}$ refresh mode, a internal counter test mode is provided. The user can use the counter test mode to write in a data pattern consecutively (512 write cycles) and then verify the data which have been written by 512 consecutive read cycles. In the counter test mode the HY51C1002/L will ignore the external row/column address and take the internal counter output as the row/column address.

DATA RETENTION MODE

The HY51C1002/L offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the HY51C1002/L power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I=\frac{(t_{RC})\times(I\ active)+(t_{RX}-t_{RC})\times(I_{DD6})}{t_{RX}}$$

Where t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval/512

STATIC COLUMN MODE OPERATION

Static column mode operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Read, write, and read-write-read cycles can be performed during static column mode operation. The row address is internally retained by maintaining $\overline{RAS}$ active. Following the entry cycle into static column mode operation, the data are accessed simply by changing the column address. Because the column address buffer acts as a transparent or flow-through latch, access begins from a valid column address. Thus the HY51C1002/L operates like a Static RAM for multiple accesses within the same row and $\overline{CS}$ acts as an output enable. Static column mode allows mixed read and write operation cycles. Terminating the write cycle with $\overline{WE}$ going high will release column address latch and data input and then start the read cycle by sampling new column address. The user has total control of read and write cycles by $\overline{WE}$ timing. Static column mode provide a sustained data rate over 18 MHz for applications that require high clocks (greater than the refresh interval).
calculate the data rate:

$$\text{Data Rate}=\frac{1024}{t_{RC}+1023\times t_{SRC}}$$

DATA OUTPUT OPERATION

The HY51C1002/L data output (D_{OUT}), which tri-state capability, is controlled by $\overline{CS}$. During a $\overline{CS}$ high state ($\overline{CS}$ at V_{IH}), the data output is in a high impedence state. The following talbe summarize the D_{OUT} state for various types of cycles.

CYCLE	D_{OUT} STATE
Read cycle	Data from addressed memory cell
$\overline{CS}$ controlled write cycel (early write)	High impedance
$\overline{WE}$ controlled write cycle (late write)	Active, Not valid
Read-modify-write cycle	Data from addressed memory cell
$\overline{RAS}$-only refresh cycle	High-impedance
Early write-read cycle ($\overline{CS}=V_{IL}$ $\overline{WE}$ controlled)	From high-impedance to valid data (new Y address).
Read-Modify-Write cycle to read cycle ($\overline{CS}=V_{IL}$, $\overline{WE}$ controlled)	Valid data from previous Y address to Valid data of new Y address

POWER ON

An initial pause of 200 μs is required after the application of V_{DD} power supply, followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh cycle). Eight initialization cycles are required after extended periods of bias without clocks (greater than the refresh interval).

The V_{DD} current (I_{DD}) requirement of the HY51C1002/L during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CS}$. If $\overline{RAS}=V_{IL}$ during power on, the device will go into an active cycle and I_{DD} will exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CS}$ track with V_{DD} or be held at a valid V_{IH} level during power on.