



Integrated Device Technology Inc

# HIGH-SPEED CMOS OCTAL D REGISTER (3-STATE)

IDT54AHCT574

## FEATURES:

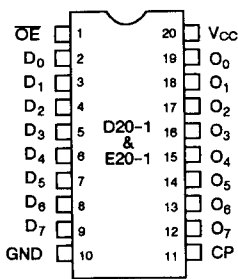
- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical address to output delay
- $I_{OL} = 14\text{mA}$  over full military temperature range
- CMOS power levels (5 $\mu\text{W}$  typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5 $\mu\text{A}$  max.)
- Octal D register (3-state)
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

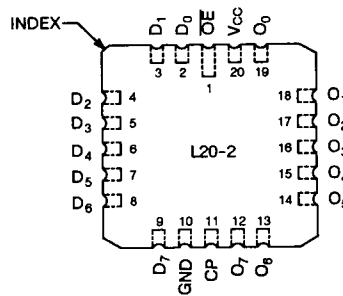
The IDT54AHCT574 are 8-bit registers built using advanced CEMOS™, a dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered three-state output control. When the output enable ( $\overline{OE}$ ) input is LOW, the eight outputs are enabled. When the  $\overline{OE}$  input is HIGH, the outputs are in the three-state condition.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

## PIN CONFIGURATIONS



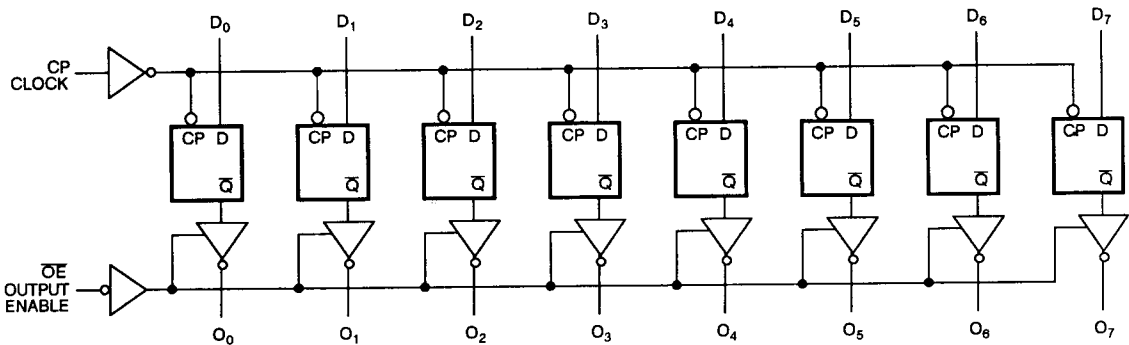
DIP/CERPACK  
TOP VIEW



LCC  
TOP VIEW

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## FUNCTIONAL BLOCK DIAGRAM



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MILITARY TEMPERATURE RANGE

DECEMBER 1987

**ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>**

SYMBOL	RATING	VALUE	UNIT
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	0.5	W
I <sub>OUT</sub>	DC Output Current	120	mA

**NOTE:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**CAPACITANCE** (T<sub>A</sub> = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER <sup>(1)</sup>	CONDITIONS	TYP.	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

**NOTE:**

- This parameter is measured at characterization but not tested.

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Following Conditions Apply Unless Otherwise Specified:

T<sub>A</sub> = -55°C to +125°C

V<sub>CC</sub> = 5.0V ± 10%

V<sub>LC</sub> = 0.2V

V<sub>HC</sub> = V<sub>CC</sub> - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS <sup>(1)</sup>	MIN.	TYP. <sup>(2)</sup>	MAX.	UNIT
V <sub>IH</sub>	Input HIGH Level	Guaranteed Logic High Level	2.0	—	—	V
V <sub>IL</sub>	Input LOW Level	Guaranteed Logic Low Level	—	—	0.8	V
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>CC</sub>	—	—	5	µA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND	—	—	-5	µA
I <sub>OZ</sub>	Off State (High Impedance) Output Current	V <sub>CC</sub> = Max. V <sub>O</sub> = V <sub>CC</sub>	—	—	10	µA
		V <sub>O</sub> = GND	—	—	-10	
I <sub>SC</sub>	Short Circuit Current	V <sub>CC</sub> = Max. <sup>(3)</sup>	-60	-120	—	mA
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 3V, V <sub>IN</sub> = V <sub>LC</sub> or V <sub>HC</sub> , I <sub>OH</sub> = -32µA	V <sub>HC</sub>	V <sub>CC</sub>	—	V
		V <sub>CC</sub> = Min., I <sub>OH</sub> = -150µA	V <sub>HC</sub>	V <sub>CC</sub>	—	
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OH</sub> = -1.0mA	2.4	4.3	—	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 3V, V <sub>IN</sub> = V <sub>LC</sub> or V <sub>HC</sub> , I <sub>OL</sub> = 300µA	—	GND	V <sub>LC</sub>	V
		V <sub>CC</sub> = Min., I <sub>OL</sub> = 300µA	—	GND	V <sub>LC</sub>	
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OL</sub> = 14mA	—	—	0.4	

**NOTES:**

- For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

**POWER SUPPLY CHARACTERISTICS**

$V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS <sup>(1)</sup>	MIN.	TYP. <sup>(2)</sup>	MAX.	UNIT	
$I_{CCQ}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} \geq V_{HC}; V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$	—	0.001	1.5	mA	
$I_{CCT}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$	—	0.5	2.0	mA	
$I_{CCD}$	Dynamic Power Supply Current <sup>(5)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = \text{GND}$ One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/MHz
$I_{CC}$	Total Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 1.0\text{MHz}$ , 50% Duty Cycle $\overline{OE} = \text{GND}$ One Bit Toggling at $f_I = 500\text{kHz}$ 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			$V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	—	0.65	3.8	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 1.0\text{MHz}$ , 50% Duty Cycle $\overline{OE} = \text{GND}$ Eight Bits Toggling at $f_I = 250\text{kHz}$ 50% Duty Cycle	$V_{IN} \geq V_{HC}^{(6)}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.63	2.2	
			$V_{IN} = 3.4V^{(6)}$ or $V_{IN} = \text{GND}$	—	2.88	11.2	

**NOTES:**

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ , +25°C ambient and maximum loading.
- Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.
- $I_{CC} = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$   
 $I_{CCQ}$  = Quiescent Current  
 $I_{CCT}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )  
 $D_H$  = Duty Cycle for TTL inputs High  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input Transition pair (HLH or LHL)  
 $f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 $f_I$  = Input Frequency  
 $N_I$  = Number of inputs at  $f_I$   
 All currents are in milliamps and all frequencies are in megahertz.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.

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**DEFINITION OF FUNCTIONAL TERMS**

PIN NAMES	DESCRIPTION
D <sub>1</sub>	The D flip-flop data inputs. Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.
CP	
O <sub>1</sub>	The register three-state outputs. Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.
OE	

**TRUTH TABLE**

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	OE	CLOCK	D <sub>1</sub>	O <sub>1</sub>	Q <sub>1</sub>
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L		L	L	L
	L		H	H	H
	H		L	Z	L
	H		H	Z	H

H = HIGH  
L = LOW  
X = Don't Care  
Z = High Impedance  
 = LOW-to-HIGH transition  
NC = No Change

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

SYMBOL	PARAMETER	CONDITION <sup>(1)</sup>	TYP.	MIN. <sup>(2)</sup>	MAX.	UNIT
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to O <sub>N</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	10.0	2.0	15.0	ns
t <sub>ZH</sub> t <sub>ZL</sub>	Output Enable Time		11.0	1.5	21.0	ns
t <sub>HZ</sub> t <sub>LZ</sub>	Output Disable Time		9.0	1.5	15.0	ns
t <sub>S</sub>	Set-up Time HIGH or LOW D <sub>N</sub> to CP		2.0	2.0	—	ns
t <sub>H</sub>	Hold Time HIGH or LOW D <sub>N</sub> to CP		0.5	1.5	—	ns
t <sub>W</sub>	CP Pulse Width HIGH or LOW		10.0	6.0	—	ns

**NOTES:**

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

**ORDERING INFORMATION**

