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80C550/83C550/87C550

CMOS single-chip 8-bit microcontroller with A/D and watchdog timer

DESCRIPTION

The Philips 8XC550 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. This Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity. The CMOS 8XC550 has the same instruction set as the 80C51.

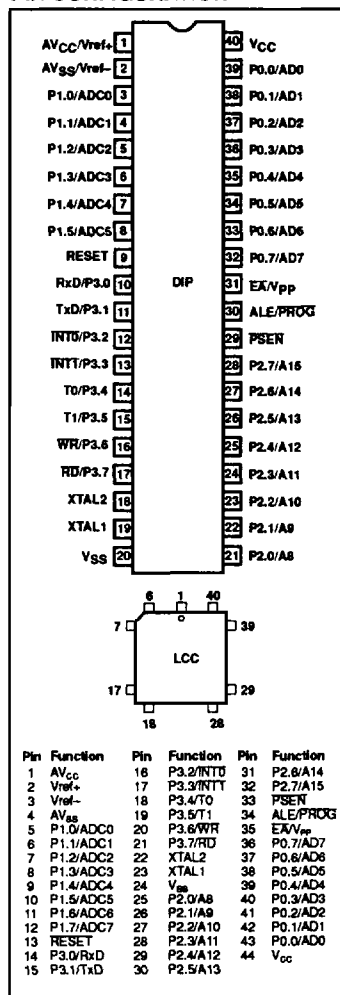
The 8XC550 contains a 4k x 8 EPROM (87C550)/ROM (83C550)/ROMless (80C550 has no program memory on-chip), a 128 x 8 RAM, 8 channels of 8-bit A/D, four 8-bit ports (port 1 is input only), a watchdog timer, two 16-bit counter/timers, a seven-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and an on-chip oscillator and clock circuits.

In addition, the 8XC550 has two software selectable modes of power reduction – idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

- 80C51 based architecture
 - 4k x 8 EPROM (87C550)/ROM (83C550)
 - 128 x 8 RAM
 - 8 channels of 8-bit A/D
 - Two 16-bit counter/timers
 - Watchdog timer
 - Full duplex serial channel
 - Boolean processor
- Memory addressing capability
 - 64k ROM and 64k RAM
- Power control modes:
 - Idle mode
 - Power-down mode
- CMOS and TTL compatible
- Three speed ranges at $V_{CC} = 5V \pm 10\%$
 - 3.5 to 12MHz
 - 3.5 to 16MHz
- Four package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATION



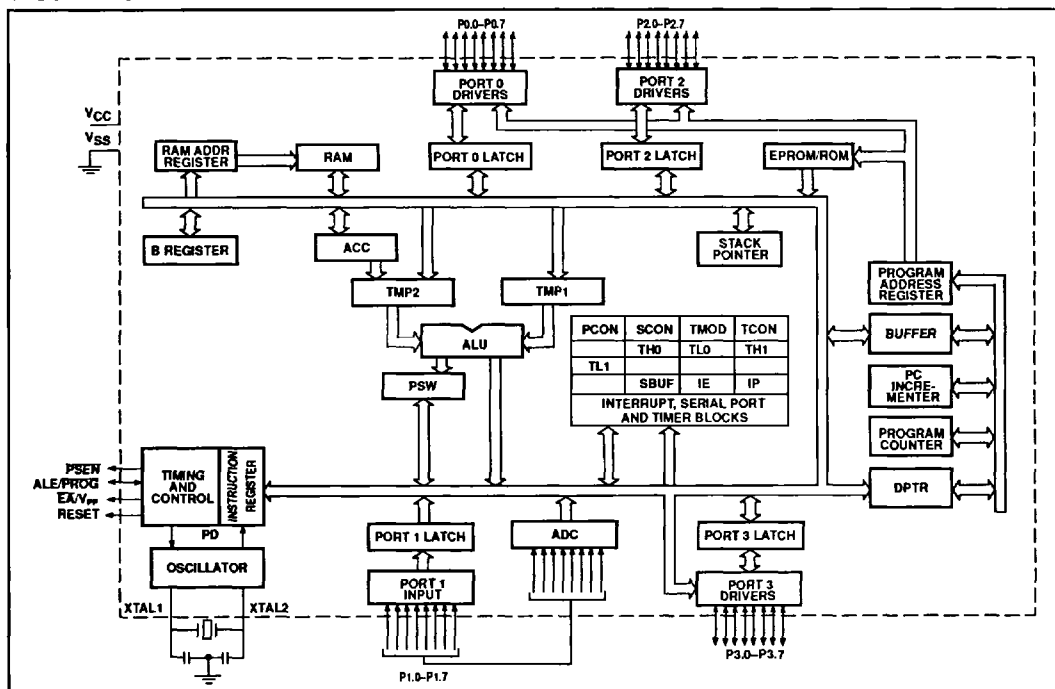
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PART NUMBER SELECTION

ROMless	ROM	EPROM	TEMPERATURE AND PACKAGE	FREQUENCY
P80C550BBF	P83C550BBF	P87C550BBF	0 to +70°C, ceramic DIP	3.5 to 12MHz
P80C550EBF	P83C550EBF	P87C550EBF	0 to +70°C, ceramic DIP	3.5 to 16MHz
P80C550BBK	P83C550BBK	P87C550BBK	0 to +70°C, ceramic LCC	3.5 to 12MHz
P80C550EBK	P83C550EBK	P87C550EBK	0 to +70°C, ceramic LCC	0.5 to 16MHz
P80C550BBP	P83C550BBP	P87C550BBP	0 to +70°C, plastic DIP	3.5 to 12MHz
P80C550EBP	P83C550EBP	P87C550EBP	0 to +70°C, plastic DIP	3.5 to 16MHz
P80C550BBA	P83C550BBA	P87C550BBA	0 to +70°C, plastic LCC	3.5 to 12MHz
P80C550EBA	P83C550EBA	P87C550EBA	0 to +70°C, plastic LCC	3.5 to 16MHz
P80C550BFP	P83C550BFP	P87C550BFP	-40 to +85°C, plastic DIP	3.5 to 12MHz
P80C550EFP	P83C550EFP	P87C550EFP	-40 to +85°C, plastic DIP	3.5 to 16MHz
P80C550BFA	P83C550BFA	P87C550BFA	-40 to +85°C, plastic LCC	3.5 to 12MHz
P80C550EFA	P83C550EFA	P87C550EFA	-40 to +85°C, plastic LCC	3.5 to 16MHz
P80C550BFF	P83C550BFF	P87C550BFF	-40 to +85°C, ceramic DIP	3.5 to 12MHz
P80C550EFF	P83C550EFF	P87C550EFF	-40 to +85°C, ceramic LCC	3.5 to 12MHz
P80C550BFK	P83C550BFK	P87C550BFK	-40 to +85°C, ceramic LCC	3.5 to 16MHz
P80C550EFK	P83C550EFK	P87C550EFK	-40 to +85°C, ceramic DIP	3.5 to 16MHz

BLOCK DIAGRAM



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PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	LCC		
V _{SS}	20	24	I	Ground: 0V reference.
V _{CC}	40	44	I	Power Supply: This is the power supply voltage for normal, idle, and power-down operation.
AV _{CC}	1	1	I	Analog Power Supply: Analog supply voltage.
AV _{SS}	2	4	I	Analog Ground: Analog 0V reference.
V _{ref+} V _{ref-}		2 3	I	V_{ref}: A/D converter reference level inputs. Note that these references are combined with AV _{CC} and AV _{SS} in the 40-pin DIP package.
P0.0–P0.7	39–32	43–36	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the S87C550. External pull-ups are required during program verification.
P1.0–P1.7	3–8	5–12	I	Port 1: Port 1 is an 8-bit input only port (6-bit in the DIP package; bits P1.6 and P1.7 are not implemented). Port 1 digital input can be read out any time.
ADC0–ADC7	3–8	5–12		ADCx: Inputs to the analog multiplexer input of the 8-bit A/D. There are only six A/D inputs in the DIP package.
P2.0–P2.7	21–28	25–32	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	10–17	14–21	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 3 also serves the special features of the SC80C51 family, as listed below: RxD (P3.0): Serial input port TxD (P3.1): Serial output port INT0 (P3.2): External interrupt INT1 (P3.3): External interrupt T0 (P3.4): Timer 0 external input T1 (P3.5): Timer 1 external input WR (P3.6): External data memory write strobe RD (P3.7): External data memory read strobe
RST	9	13	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V _{SS} permits a power-on reset using only an external capacitor to V _{CC} .
ALE/PROG	30	34	I/O	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming.
PSEN	29	33	O	Program Store Enable: The read strobe to external program memory. When the device is executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.
E _A /V _{PP}	31	35	I	External Access Enable/Programming Supply Voltage: E _A must be externally held low to enable the device to fetch code from external program memory locations 0000H to 1FFFFH. If E _A is held high, the device executes from internal program memory unless the program counter contains an address greater than 1FFFFH. For the 80C550 ROMless part, E _A must be held low for the part to operate properly. This pin also receives the 12.75V programming supply voltage (V _{PP}) during EPROM programming.
XTAL1	19	23	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	22	O	Crystal 2: Output from the inverting oscillator amplifier.

CMOS single-chip 8-bit microcontroller**80C550/83C550/87C550****Table 1. Interrupt Priorities**

Priority	Source	Vector Address	Function
Highest	INT0	0003H	External interrupt 0
	T0	000BH	Timer flag 0
	INT1	0013H	External interrupt 1
	T1	001BH	Timer flag 1
	SIO	0023H	Serial port interrupt
	ADC	002BH	A/D conversion complete
Lowest	WD	0033H	Watchdog timer

INTERRUPTS

The interrupt structure is a seven source, two level interrupt system similar to that of the 80C51. The interrupt sources are listed in Table 1 in order of polling sequence priority (highest to lowest). Note that the watchdog timer function is available only if the watchdog timer function is disabled and the watchdog timer is used as a general purpose timer.

Interrupt Control Registers

The interrupt enable and the interrupt priority registers have been modified to take into account the different interrupt sources of the 8XC550. In all other respects, their operation is identical to that of the 80C51. Setting a bit in the IE register enables the interrupt; clearing the bit disables the interrupt. All bits are cleared by reset. See Figure 1 for interrupt register formats.

SERIAL COMMUNICATIONS

The serial port operation is identical to that of the 80C51. In order to conserve power, another bit (SIDL) has been added to the PCON register that idles the serial port when it is not being used. This bit is cleared by reset. See Figure 2.

A/D CONVERTER

The analog input circuitry consists of an 8-input analog multiplexer and an analog-to-digital converter with 8-bit resolution. In the LCC package, the analog reference voltage and analog power supplies are connected via separate input pins; in the DIP package, Vref+ is combined with AV_{CC} and Vref- is combined with AV_{SS}. The analog inputs are alternate functions to port 1, which is an input only port. Digital input to port 1 can be read any time during an A/D conversion. Care should be exercised in mixing analog and digital signals on port 1, because cross talk from the digital input signals can degrade the A/D conversion accuracy of the analog input. An A/D conversion requires 40 machine cycles.

The A/D converter is controlled by the ADCON special function register. The input channel to be converted is selected by the analog multiplexer by setting ADCON register bits, ADDR2-ADDR0 (see Figure 3). These bits can only be changed when ADCI and ADCS are both low.

The completion of the 8-bit ADC conversion is flagged by ADCI in the ADCON register and the result is stored in the special function

register ADAT. The functions of the ADCI and ADCS are:

ADCI	ADCS	Operation
0	0	ADC not busy. A conversion can be started.
0	1	ADC busy. Start of a new conversion is blocked.
1	0	Conversion completed. start of new conversion is blocked.
1	1	Not possible.

An ADC conversion in progress is unaffected by a software ADC start. The result of a completed conversion remains unaffected provided ADCI remains at a logic 1. While ADCS is a logic 1 or ADCI is a logic 1, a new ADC START will be blocked and consequently lost. An A/D conversion in progress will be aborted when the idle or power-down mode is entered. The result of a completed conversion (ADCI = logic 1) remains unaffected when entering the idle mode, but will be lost if power-down mode is entered.

MSB								INTERRUPT ENABLE REGISTER (IE)								LSB							
EA		EWD		EAD		ES		ET1		EX1		ET0		EX0									

BIT		SYMBOL		FUNCTION	
IE.7		EA		GLOBAL INTERRUPT DISABLE WHEN EA = 0	
IE.6		EWD		WATCHDOG TIMER OVERFLOW	
IE.5		EAD		A/D CONVERSION COMPLETE	
IE.4		ES		SIO INTERRUPT	
IE.3		ET1		TIER 1 OVERFLOW	
IE.2		EX1		EXTERNAL INTERRUPT 1	
IE.1		ET0		TIMER 0 OVERFLOW	
IE.0		EX0		EXTERNAL INTERRUPT 0	

NOTE:
The interrupt priority register function is identical to that of the 80C51. A '1' sets that interrupt to the high priority level and a '0' sets the interrupt to the low priority level.

MSB								INTERRUPT PRIORITY REGISTER (IP)								LSB							
X		PWD		PAD		PS		PT1		PX1		PT0		PX0									

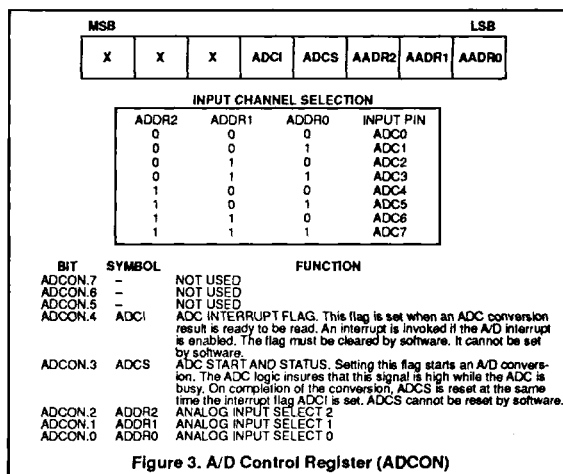
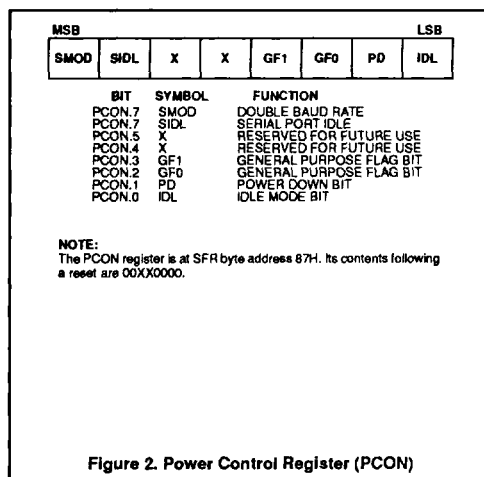
BIT		SYMBOL		FUNCTION	
IP.6		PWD		WATCHDOG TIMER	
IP.5		PAD		A/D CONVERTER	
IP.4		PS		SIO INTERRUPT	
IP.3		PT1		T1 INTERRUPT	
IP.2		PX1		INT1 INTERRUPT	
IP.1		PT0		T0 INTERRUPT	
IP.0		PX0		INT0 INTERRUPT	

Figure 1. Interrupt Registers

Figure 1. Interrupt Registers

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WATCHDOG TIMER

The watchdog timer is not directly loadable by the user. Instead, the value to be loaded into the main timer is held in an autoloader register or is part of the mask ROM programming. In order to cause the main timer to be loaded with the appropriate value, a special sequence of software action must take place. This operation is referred to as feeding the watchdog timer.

To feed the watchdog, two instructions must be sequentially executed successfully. No intervening instruction fetches are allowed, so interrupts should be disabled before feeding the watchdog. The instructions should move A5H to the WFEED1 register and then 5AH to the WFEED2 register. If WFEED1 is correctly loaded and WFEED2 is not correctly loaded, then an immediate underflow will occur.

The watchdog timer subsystem has two modes of operation. Its principal function is a watchdog timer. In this mode it protects the system from incorrect code execution by causing a system reset when the watchdog timer underflows as a result of a failure of software to feed the timer prior to the timer reaching its terminal count. If the user does not employ the watchdog function, the watchdog subsystem can be used as a timer. In this mode, reaching the terminal count sets a flag which can be used to generate an interrupt. In most other respects, the timer mode possesses the characteristics of the watchdog mode. This is done to protect the integrity of the watchdog function.

The watchdog timer subsystem consists of a prescaler and a main counter. The prescaler

has 8 selectable taps off the final stages and the output of a selected tap provides the clock to the main counter. The main counter is the section that is loaded as a result of the software feeding the watchdog and it is the section that causes the system reset (watchdog mode) or time-out flag to be set (timer mode) if allowed to reach its terminal count.

Programming the Watchdog Timer

Both the EPROM and ROM devices have a set of SFRs for holding the watchdog autoloader values and the control bits. The watchdog time-out flag is present in the watchdog control register and operates the same in all versions. In the EPROM device, the watchdog parameters (autoloader value and control) are always taken from the SFRs. In the ROM device, the watchdog parameters can be mask programmed or taken from the SFRs. The selection to take the watchdog parameters from the SFRs or from the mask programmed values is controlled by EA (external access). When EA is high (internal ROM access), the watchdog parameters are taken from the mask programmed values. If the watchdog is masked programmed to the timer mode, then the autoloader values and the pre-scaler taps are taken from the SFRs. When EA is low (external access), the watchdog parameters are taken from the SFRs. The user should be able to leave code in his program which initializes the watchdog SFRs even though he has migrated to the mask ROM part. This allows no code changes from EPROM prototyping to ROM coded production parts.

Watchdog Detailed Operation

EPROM Device (and ROMless Operation: EA = 0)

In the ROMless operation (ROM part, EA = 0) and in the EPROM device, the watchdog operates in the following manner.

Whether the watchdog is in the watchdog or timer mode, when external RESET is applied, the following takes place:

- Watchdog mode bit set to timer mode.
- Watchdog run control bit set to OFF.
- Autoloader register set to FF (max count).
- Watchdog time-out flag cleared.
- Prescaler is cleared.
- Prescaler tap set to the highest divide.
- Autoloader takes place.

The watchdog can be fed even though it is in the timer mode.

Note that the operational concept is for the watchdog mode of operation, when coming out of a hardware reset, the software should load the autoloader registers, set the mode to watchdog, and then feed the watchdog (cause an autoloader). The watchdog will now be starting at a known point.

If the watchdog is in the watchdog mode and running and happens to underflow at the time the external RESET is applied, the watchdog time-out flag will be cleared.

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When the watchdog is in the watchdog mode and the watchdog underflows, the following action takes place:

- Autoload takes place.
- Watchdog time-out flag is set
- Timer mode interrupt flag unchanged.
- Mode bit unchanged.
- Watchdog run bit unchanged.
- Autoload register unchanged.
- Prescaler tap unchanged.
- All other device action same as external reset.

Note that if the watchdog underflows, the program counter will start from 00H as in the case of an external reset. The watchdog time-out flag can be examined to determine if the watchdog has caused the reset condition. The watchdog time-out flag bit can be cleared by software.

When the watchdog is in the timer mode and the timer software underflows, the following action takes place:

- Autoload takes place.
- Watchdog time-out flag is set
- Mode bit unchanged.
- Watchdog run bit unchanged.
- Autoload register unchanged.
- Prescaler tap unchanged.

The timer mode interrupt flag is cleared when the interrupt routine is invoked. This bit can also be cleared directly by software without a software feed operation.

Mask ROM Device (EA = 1)

In the mask ROM device, the watchdog mode bit (WDMOD) is mask programmed and the bit in the watchdog command register is read only and reflects the mask programmed selection. If the mask programmed mode bit selects the timer mode, then the watchdog run bit (WDRUN) operates as described under EPROM Device. If the mask programmed bit selects the watchdog mode, then the watchdog run bit has no effect on the timer operation.

Watchdog Function

The watchdog consists of a programmable prescaler and the main timer. The prescaler derives its clock from the on-chip oscillator.

The prescaler consists of a divide by 12 followed by a 13 stage counter with taps from stage 6 through stage 13. The tap selection is programmable. The watchdog main counter is a down counter clocked (decremented) each time the programmable prescaler underflows. The watchdog generates an underflow signal (and is autoloading) when the watchdog is at count 0 and the clock to decrement the watchdog occurs. The watchdog is 8 bits long and the autoload value can range from 0 to FFH. (The autoload value of 0 is permissible since the prescaler is cleared upon autoload).

This leads to the following user design equations. Definitions: t_{OSC} is the oscillator period, N is the selected prescaler tap value, W is the main counter autoload value, t_{MIN} is the minimum watchdog time-out value (when the autoload value is 0), t_{MAX} is the maximum time-out value (when the autoload value is FFH), t_D is the design time-out value.

$$t_{MIN} = t_{OSC} \times 12 \times 64$$

$$t_{MAX} = t_{MIN} \times 128 \times 256$$

$$t_D = t_{MIN} \times 2^{PRESALER} \times W$$

(where prescaler = 0, 1, 2, 3, 4, 5, 6, or 7)

Note that the design procedure is anticipated to be as follows. A t_{MAX} will be chosen either from equipment or operation considerations and will most likely be the next convenient value higher than t_D . (If the watchdog were inadvertently to start from FFH, an overflow would be guaranteed, barring other anomalies, to occur within t_{MAX}). Then the value for the prescaler would be chosen from:

$$prescaler = \log_2 (t_{MAX} / (t_{OSC} \times 12 \times 256)) - 6$$

This then also fixes t_{MIN} . An autoload value would then be chosen from:

$$W = t_D / t_{MIN} - 1$$

The software must be written so that a feed operation takes place every t_D seconds from the last feed operation. Some tradeoffs may need to be made. It is not advisable to include feed operations in minor loops or in subroutines unless the feed operation is a specific subroutine.

Watchdog Control Register (WDCON) (Bit Addressable) Address C0

The following bits of this register are read only in the ROM part when EA is high: WDMOD, PRE0, PRE1, and PRE2. That is, the register will reflect the mask programmed

values. In the ROM part with EA high, these bits are taken from mask coded bits and are not readable by the program. WDRUN is read only in the ROM part when EA is high and MDMOD is in the watchdog mode. When WDMOD is in the timer mode, WDRUN functions normally (see Figure 4).

The parameters written into WDMOD, PRE0, PRE1, and PRE2 by the program are not applied directly to the watchdog timer subsystem. The watchdog timer subsystem is directly controlled by a second register which stores these bits. The transfer of these bits from the user register (WDMOD) to the second control register takes place when the watchdog is fed. This prevents random code execution from directly foiling the watchdog function. This does not affect the operation where these bits are taken from mask coded values.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol, page 1.

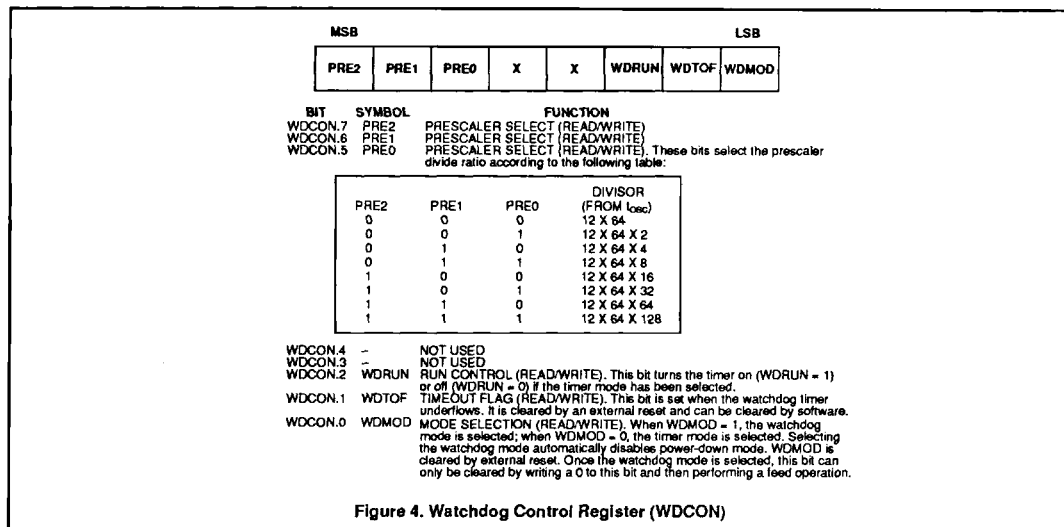
To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

IDLE MODE

In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. An A/D conversion in progress will be aborted when idle mode is entered. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

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**Programmable Idle Modes**

The programmable idle modes have been dispersed throughout the functional blocks. Each block has its own ability to be disabled. For example, if timer 0 is not commanded to be running ($TR = 0$), then the clock to the timer is disabled resulting in an idle mode power saving. An additional idle control bit has been added to the serial communications port.

A/D Operation in Idle Mode

When in the idle mode, the A/D converter will be disabled. However, the current through the V_{ref} pins will be present and will not be reduced internally in either the idle or the power-down modes. It is the responsibility of the user to disconnect V_{ref} to reduce power supply current.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-

down is the last instruction executed. The power-down mode can be terminated by a Reset in the same way as in the 80C51 or in addition by one of two external interrupts, $INT0$ or $INT1$. A termination with an external interrupt does not affect the internal data memory and does not affect the special function registers. This makes it possible to exit power-down without changing the port output levels. To terminate the power-down mode with an external interrupt, $INT0$ or $INT1$ must be switched to level-sensitive and must be enabled. The external interrupt input signal $INT0$ and $INT1$ must be kept low until the oscillator has restarted and stabilized. An instruction following the instruction that puts the device in the power-down mode will be executed. A reset generated by the watchdog timer terminates the power-down mode in the same way as an external Reset, and only the contents of the on-chip RAM are preserved.

The control bits for the reduced power modes are in the special function register PCON.

DESIGN CONSIDERATIONS

At power-on, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.

When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when idle is terminated by reset, the instruction following the one that invokes idle should not be one that writes to a port pin or to external memory. Table 2 shows the state of I/O ports during low current operating modes.

Table 2. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

CMOS single-chip 8-bit microcontroller**80C550/83C550/87C550****Encryption Table**

The encryption table is a feature of the 83C550 and 87C550 that protects the code from being easily read by anyone other than the programmer. The encryption table is 32 bytes of code that are exclusive NORed with the program code data as it is read out. The first byte is XNORed with the first location read, the second with the second read, etc.

After the encryption table has been programmed, the user has to know its contents in order to correctly decode the program code data. The encryption table itself cannot be read out.

For the EPROM (87C550) part, the encryption table is programmed in the same manner as the program memory, but using the "Pgm Encryption Table" levels specified in Table 4. After the encryption table is programmed,

verification cycles will produce only encrypted information.

For the ROM part (83C550) the encryption table information is submitted with the ROM code as shown in Table 3.

Security Bits

There are two security bits on the 83C550 and 87C550 that, when set, prevent the program data memory from being read out or programmed further.

After the first security bit is programmed, the external MOV C instruction is disabled, and for the 87C550, further programming of the code memory or the encryption table is disabled. The other security bit can of course still be programmed. With only security bit one programmed, the memory can still be read out for program verification. After the second security bit is programmed, it is no

longer possible to read out (verify) the program memory.

To program the security bits for the 87C550, repeat the programming sequence using the "Pgm Lock Bit" levels specified in Table 4. For the masked ROM 83C550 the security bit information is submitted with the ROM code as shown in Table 3.

ROM Code Submission

When submitting a ROM code for the 83C550, the following must be specified:

1. The 4k byte user ROM program.
2. The 32 byte ROM encryption key.
3. The ROM security bits.
4. The watchdog timer parameters.

This information can be submitted in an EPROM (2764) or hex file with the format specified in Table 3.

Table 3. ROM Code Submittal Requirements

ADDRESS	CONTENT	BIT(s)	COMMENT
0000H to 0FFFH	Data	7:0	User ROM data
1000H to 101FH	Key	7:0	ROM encryption key; FFH = no encryption
1020H	Security	0	ROM security bit 1
1020H	Security	1	ROM security bit 2 0 = enable security feature 1 = disable security feature
1020H	Security	2	ROM security bit 3
1030H	WMOD	0	Watchdog mode bit; 00H = timer mode 01H = watchdog mode
1031H	PRE2:0	2:0	Watchdog prescaler selection; 00H = divide by 12 x 64 07H = divide by 12 x 64 x 128 (see specification)
1032H	WD	7:0	Watchdog autoloading value (see specification)

CMOS single-chip 8-bit microcontroller**80C550/83C550/87C550****Electrical Deviations from Commercial Specifications for Extended Temperature Range**

DC and AC parameters not included here are the same as in the commercial temperature range table.

DC ELECTRICAL CHARACTERISTICS $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$ (87C550), $V_{CC} = 5\text{V} \pm 20\%$ (80/83C550), $V_{SS} = 0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
V_{IL}	Input low voltage, except EA		-0.5	$0.2V_{CC}-0.15$	V
V_{IL1}	Input low voltage to EA		0	$0.2V_{CC}-0.35$	V
V_{IH}	Input high voltage, except XTAL1, RST		$0.2V_{CC}+1$	$V_{CC}+0.5$	V
V_{IH1}	Input high voltage to XTAL1, RST		$0.7V_{CC}+0.1$	$V_{CC}+0.5$	V
I_{IL}	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.45\text{V}$		-75	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3	$V_{IN} = 2.0\text{V}$		-750	μA
I_{CC}	Power supply current: Active mode Idle mode Power down mode	$V_{CC} = 4.5-5.5\text{V}$, Frequency range = 3.5 to 12MHz		35 6 50	mA mA μA

ADC DC ELECTRICAL CHARACTERISTICS $AV_{CC} = 5\text{V} \pm 10\%$, $AV_{SS} = 0\text{V}$, $t_{AMB} = -40^{\circ}\text{C}$ to 85°C , unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
AV_{CC}	Analog supply	$AV_{CC} = V_{CC} \pm 0.2$	4.5	5.5	V
V_{ref+}	Analog reference			$AV_{CC} + 0.2$	V
AI_{CC}	Analog operating supply current	See note 1		6.0	mA
AV_{IN}	Analog input voltage		$AV_{SS} - 0.2$	$AV_{CC} + 0.2$	V
A_{IC}	Analog input capacitance			15	pF
t_{ADS}	Sampling time			$8t_{CY}$	
t_{ADC}	Conversion time			$40t_{CY}$	
	Differential nonlinearity	See note 1		± 1	LSB
	Integral nonlinearity	See note 1		± 1	LSB
QSe	Offset error	See note 1		± 10	mV
Ge	Gain error	See note 1		0.4	%
M_{CTC}	Channel-to-channel matching			± 1	LSB
Ct	Crosstalk	0 - 100kHz		-60	dB

NOTES:

- Conditions: $V_{ref+} = 4.99712\text{V}$, $V_{ref-} = 0\text{V}$.
- The resistor ladder network is not disconnected in the power-down or idle modes. Thus to conserve power, the user must remove AV_{CC} and AV_{ref} .
- If the A/D function is not required, or if the A/D function is only needed periodically, AV_{CC} can be removed without affecting the operation of the digital circuitry. Contents of ADCON and ADAT are not guaranteed to be valid. Digital inputs function normally. No digital outputs are present.

CMOS single-chip 8-bit microcontroller**80C550/83C550/87C550****ABSOLUTE MAXIMUM RATINGS^{1, 2, 3}**

PARAMETER	RATING	UNIT
Operating temperature under bias	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Voltage on $\overline{EA}/V_{PP}$ pin to V_{SS} (87C550 only)	0 to +13.0	V
Voltage on any other pin to V_{SS}	-0.5 to +6.5	V
Input, output current on any two I/O pins	±10	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

DC ELECTRICAL CHARACTERISTICS
 $T_A = 0^\circ\text{C to } +70^\circ\text{C or } -40^\circ\text{C to } +85^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$ (87C550), $V_{CC} = 5\text{V} \pm 20\%$ (80/83C550), $V_{SS} = 0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYPICAL ¹	MAX	
V_{IL}	Input low voltage, except $\overline{EA}$ ⁷		-0.5		$0.2V_{CC}-0.1$	V
V_{IL1}	Input low voltage to $\overline{EA}$ ⁷		0		$0.2V_{CC}-0.3$	V
V_{IH}	Input high voltage, except XTAL1, RST ⁷		$0.2V_{CC}+0.9$		$V_{CC}+0.5$	V
V_{IH1}	Input high voltage, XTAL1, RST ⁷		$0.7V_{CC}$		$V_{CC}+0.5$	V
V_{OL}	Output low voltage, ports 2, 3	$I_{OL} = 1.6\text{mA}$ ²			0.45	V
V_{OL1}	Output low voltage, port 0, ALE, PSEN	$I_{OL} = 3.2\text{mA}$ ²			0.45	V
V_{OH}	Output high voltage, ports 2, 3, ALE, PSEN ³	$I_{OH} = -60\mu\text{A}$	2.4			V
		$I_{OH} = -25\mu\text{A}$	$0.75V_{CC}$			V
		$I_{OH} = -10\mu\text{A}$	$0.9V_{CC}$			V
V_{OH1}	Output high voltage (port 0 in external bus mode)	$I_{OH} = -800\mu\text{A}$	2.4			V
		$I_{OH} = -300\mu\text{A}$	$0.75V_{CC}$			V
		$I_{OH} = -80\mu\text{A}$	$0.9V_{CC}$			V
I_{IL}	Logical 0 input current, ports 1, 2, 3 ⁷	$V_{IN} = 0.45\text{V}$			-50	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3 ⁷	See note 4			-650	μA
I_{L1}	Input leakage current, port 0	$V_{IN} = V_{IL}$ or V_{IH}			±10	μA
I_{CC}	Power supply current: ⁷ Active mode @ 12MHz ⁵ Idle mode @ 12MHz Power down mode	See note 6		11.5	25	mA
				1.3	4	mA
				3	50	μA
R_{RST}	Internal reset pull-down resistor		50		300	kohm
C_{IO}	Pin capacitance				10	pF

NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
- Pins of ports 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
- I_{CCMAX} at other frequencies is given by: Active mode; $I_{CCMAX} = 0.94 \times \text{FREQ} + 13.71$; Idle mode; $I_{CCMAX} = 0.14 \times \text{FREQ} + 2.31$, where FREQ is the external oscillator frequency in MHz. I_{CCMAX} is given in mA. See Figure 12.
- See Figures 13 through 16 for I_{CC} test conditions.
- These values apply only to $T_A = 0^\circ\text{C to } +70^\circ\text{C}$. For $T_A = -40^\circ\text{C to } +85^\circ\text{C}$. See table on previous page.

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AC ELECTRICAL CHARACTERISTICS

 $T_A = 0^\circ\text{C to } +70^\circ\text{C or } -40^\circ\text{C to } +85^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$ (87C550), $V_{CC} = 5\text{V} \pm 20\%$ (80/83C550), $V_{SS} = 0\text{V}^{1,2}$

SYMBOL	FIGURE	PARAMETER	12MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	5	Oscillator frequency: Speed Versions S8XC550 -1, 2 S8XC550 -4, 5			3.5 3.5	12 16	MHz MHz
t_{HLL}	5	ALE pulse width	127		$2t_{CLCL}-40$		ns
t_{AVLL}	5	Address valid to ALE low	28		$t_{CLCL}-55$		ns
t_{LLAX}	5	Address hold after ALE low	48		$t_{CLCL}-35$		ns
t_{LLIV}	5	ALE low to valid instruction in		234		$4t_{CLCL}-100$	ns
t_{LLPL}	5	ALE low to PSEN low	43		$t_{CLCL}-40$		ns
t_{PLPH}	5	PSEN pulse width	205		$3t_{CLCL}-45$		ns
t_{PLIV}	5	PSEN low to valid instruction in		145		$3t_{CLCL}-105$	ns
t_{PIX}	5	Input instruction hold after PSEN	0		0		ns
t_{PIXZ}	5	Input instruction float after PSEN		59		$t_{CLCL}-25$	ns
t_{AVIV}	5	Address to valid instruction in		312		$5t_{CLCL}-105$	ns
t_{PLAZ}	5	PSEN low to address float		10		10	ns
Data Memory							
t_{RLRH}	6, 7	RD pulse width	400		$6t_{CLCL}-100$		ns
t_{WLWH}	6, 7	WR pulse width	400		$6t_{CLCL}-100$		ns
t_{RLDV}	6, 7	RD low to valid data in		252		$5t_{CLCL}-165$	ns
t_{AHDX}	6, 7	Data hold after RD	0		0		ns
t_{RHDX}	6, 7	Data float after RD		97		$2t_{CLCL}-70$	ns
t_{LDDV}	6, 7	ALE low to valid data in		517		$8t_{CLCL}-150$	ns
t_{AVDV}	6, 7	Address to valid data in		585		$9t_{CLCL}-165$	ns
t_{LLWL}	6, 7	ALE low to RD or WR low	200	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	6, 7	Address valid to WR low or RD low	203		$4t_{CLCL}-130$		ns
t_{QVWX}	6, 7	Data valid to WR transition	23		$t_{CLCL}-60$		ns
t_{WHQX}	6, 7	Data hold after WR	33		$t_{CLCL}-50$		ns
t_{RLAZ}	6, 7	RD low to address float		0		0	ns
t_{WHLH}	6, 7	RD or WR high to ALE high	43	123	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
External Clock							
t_{CHCX}	9	High time	20		20		ns
t_{CLCX}	9	Low time	20		20		ns
t_{CLCH}	9	Rise time		20		20	ns
t_{CHCL}	9	Fall time		20		20	ns
Shift Register							
t_{XLXL}	8	Serial port clock cycle time	1.0		$12t_{CLCL}$		μs
t_{QVXH}	8	Output data setup to clock rising edge	700		$10t_{CLCL}-133$		ns
t_{XHDX}	8	Output data hold after clock rising edge	50		$2t_{CLCL}-117$		ns
t_{XHDX}	8	Input data hold after clock rising edge	0		0		ns
t_{XHDX}	8	Clock rising edge to input data valid		700		$10t_{CLCL}-133$	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.

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EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A - Address

C - Clock

D - Input data

H - Logic level high

I - Instruction (program memory contents)

L - Logic level low, or ALE

P - PSEN

Q - Output data

R - RD signal

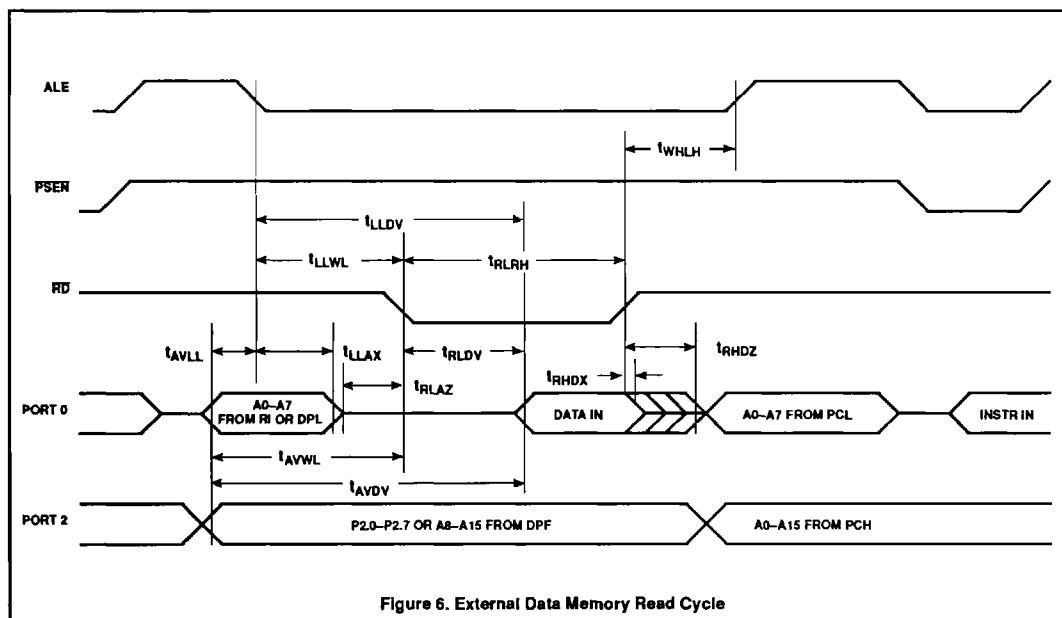
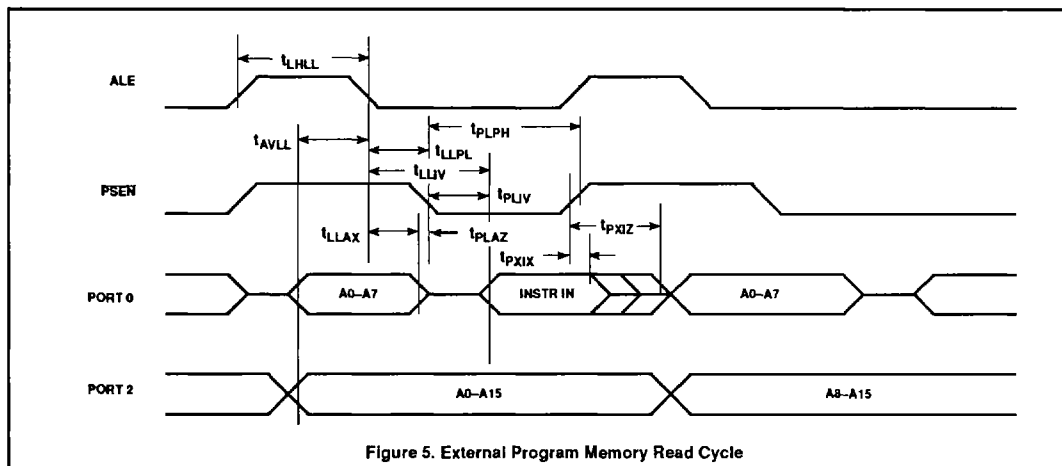
t - Time

V - Valid

W - WR signal

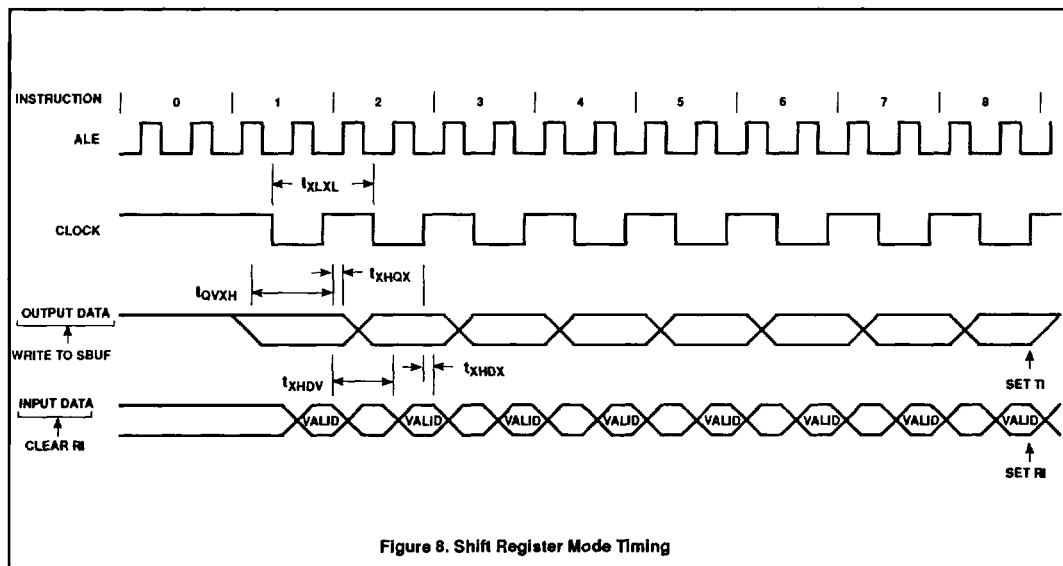
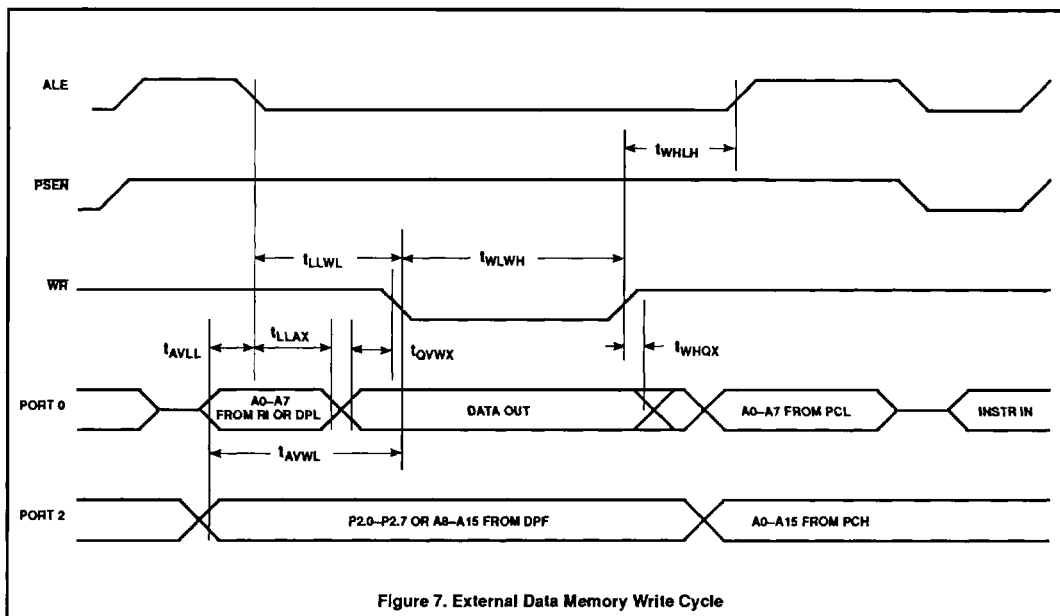
X - No longer a valid logic level

Z - Float

Examples: t_{AVLL} = Time for address valid to ALE low. t_{LLPL} = Time for ALE low to PSEN low.

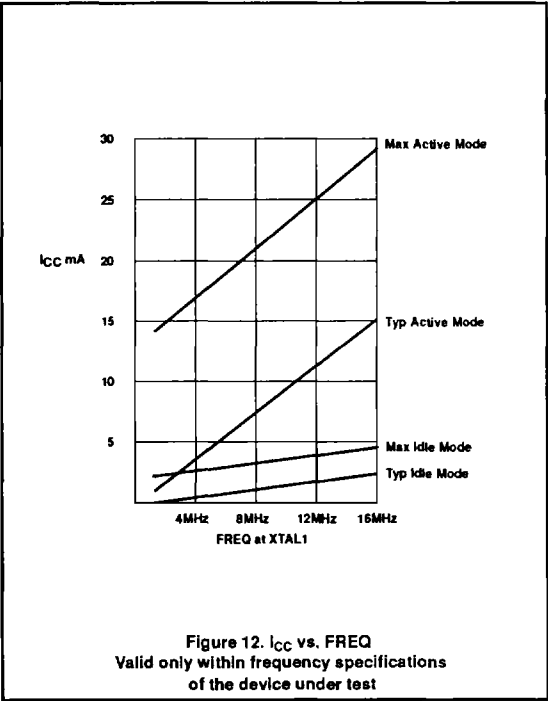
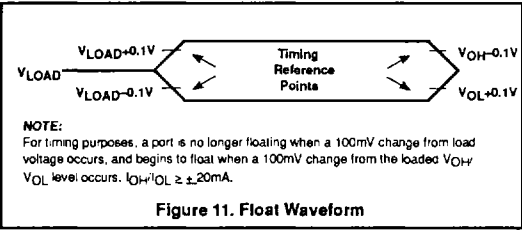
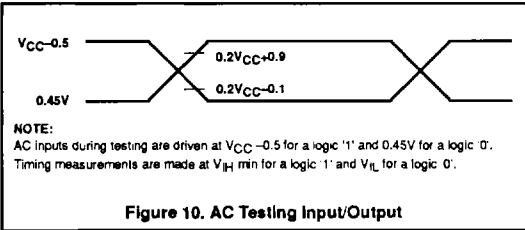
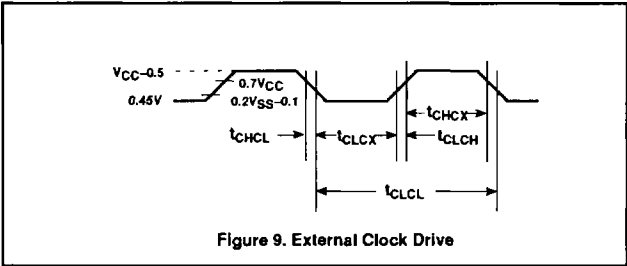
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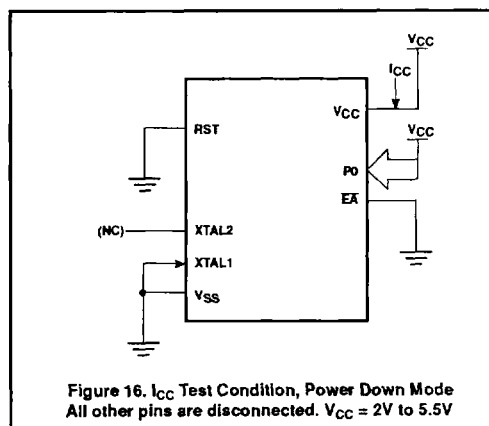
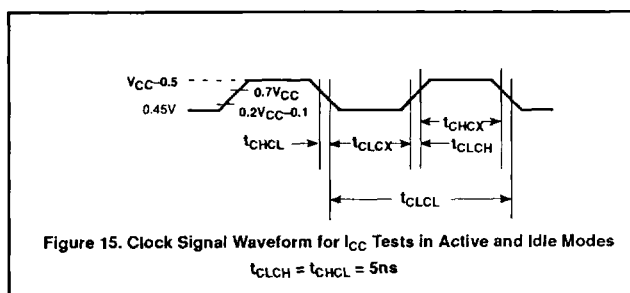
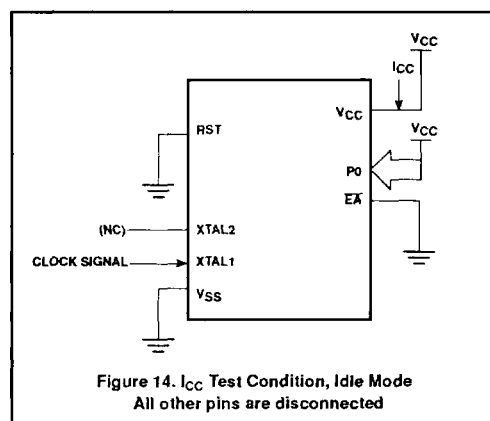
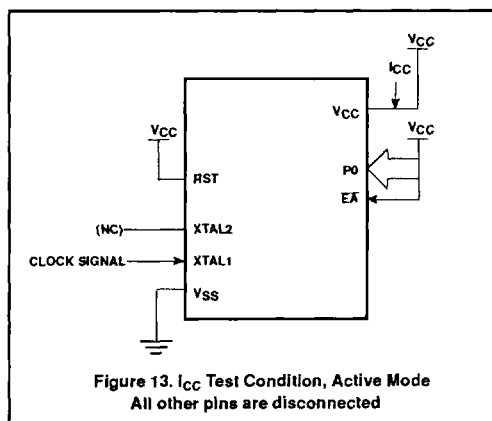
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EPROM CHARACTERISTICS

The 87C550 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/PROG pulses.

The 87C550 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an S87C550 manufactured by Philips.

Table 4 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the lock bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 17 and 18. Figure 19 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 17. Note that the 87C550 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 2 and 3, as shown in Figure 17. The code byte to be programmed into that location is applied to port 0. RST, PSEN and pins of ports 1 and 2 specified in Table 4 are held at the 'Program Code Data' levels indicated in Table 4. The ALE/PROG is pulsed low 25 times as shown in Figure 18.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the lock bits, repeat the 25 pulse programming sequence using the 'Pgm Lock Bit' levels. After one lock bit is programmed, further programming of the code memory and encryption table is disabled. However, the other lock bit can still be programmed.

Note that the $E\bar{A}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If security bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 2 and 3 as shown in Figure 19. The other pins are held at the 'Verify Code Data' levels indicated in Table 4. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P1.0 and P1.1 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips

(031H) = 96H indicates S87C550

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 4, and which satisfies the timing specifications, is suitable.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345-5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-sec/cm². Exposing the EPROM to an ultraviolet lamp of 12,000uW/cm² rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Table 4. EPROM Programming Modes

MODE	RST	PSEN	ALE/PROG	$E\bar{A}/V_{PP}$	P2.7	P2.6	P1.0	P1.1
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	V_{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	V_{PP}	1	0	1	0
Pgm security bit 1	1	0	0*	V_{PP}	1	1	1	1
Pgm security bit 2	1	0	0*	V_{PP}	1	1	0	0

NOTES:

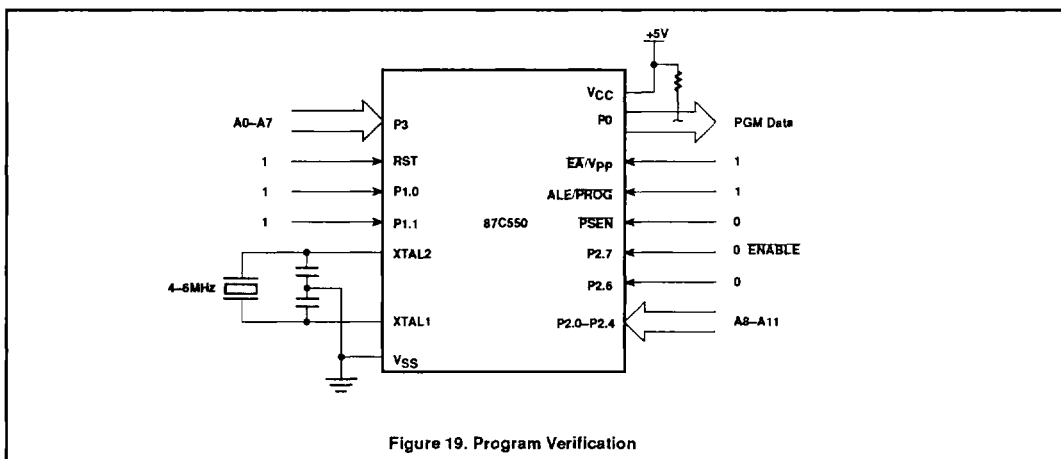
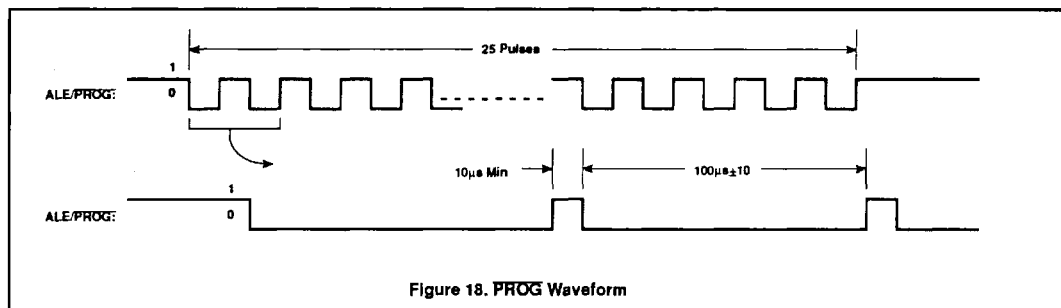
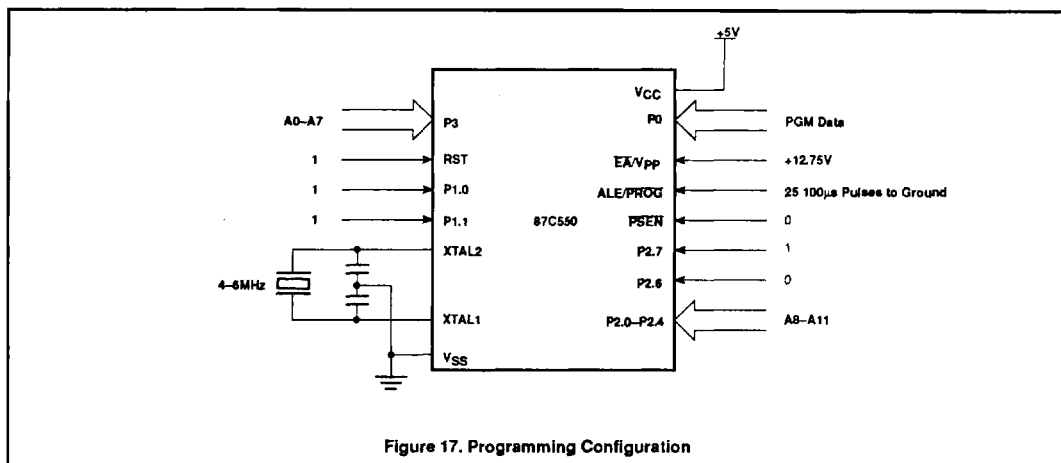
1. '0' = Valid low for that pin, '1' = valid high for that pin.
2. $V_{PP} = 12.75V \pm 0.25V$.
3. $V_{CC} = 5V \pm 10\%$ during programming and verification.

*ALE/PROG receives 25 programming pulses while V_{PP} is held at 12.75V. Each programming pulse is low for 100 μ s ($\pm 10\mu$ s) and high for a minimum of 10 μ s.

™Trademark phrase of Intel Corporation.

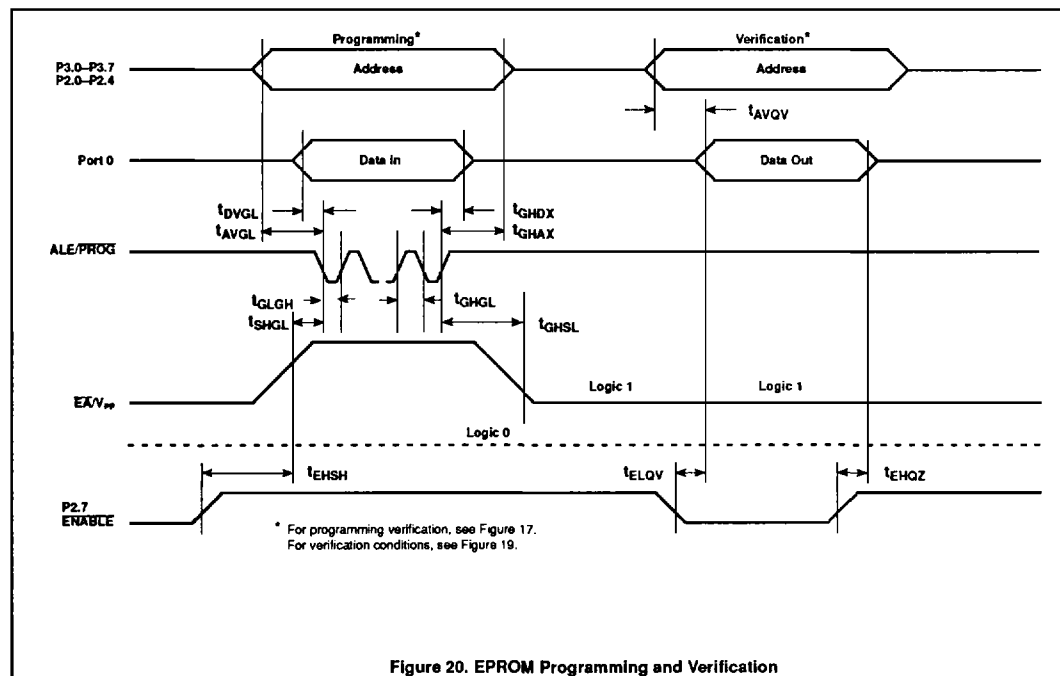
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CMOS single-chip 8-bit microcontroller**80C550/83C550/87C550****EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS** $T_A = 21^\circ\text{C}$ to $+27^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$ (See Figure 20)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to PROG low	$48t_{CLCL}$		
t_{GHAX}	Address hold after PROG	$48t_{CLCL}$		
t_{DVGL}	Data setup to PROG low	$48t_{CLCL}$		
t_{GHDX}	Data hold after PROG	$48t_{CLCL}$		
t_{EHS}	P2.7 (ENABLE) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to PROG low	10		μs
t_{GHSL}	V_{PP} hold after PROG	10		μs
t_{GLGH}	PROG width	90	110	μs
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELOZ}	ENABLE low to data valid		$48t_{CLCL}$	
t_{EHQZ}	Data float after ENABLE	0	$48t_{CLCL}$	
t_{GHGL}	PROG high to PROG low	10		μs

**Figure 20. EPROM Programming and Verification**