PRELIMINARY | COM'L: -7/10/12/15 IND: -10/12/15/20

AMD

The MACH5-256

MACH5-256/68-7/10/12/15/20 MACH5-256/104-7/10/12/15/20 MACH5-256/120-7/10/12/15/20 MACH5-256/160-7/10/12/15/20

Fifth Generation MACH® Architecture

DISTINCTIVE CHARACTERISTICS

- **Fifth generation MACH architecture**
  - 100% routable
  - Pin-out retention
  - Four power/speed options per block for maximum performance and lowest power
  - Advanced synchronous and asynchronous clocking, including dual-edge clocking
  - Asynchronous product- or sum-term set or reset
  - Functions of up to 32 product terms
  - Fixed, predictable delays
- **Fast**
  - 7.5 ns pin-to-pin delays
  - 125 MHz counter frequencies
- **High density**
  - 256 macrocells
  - 16 "32V16" PAL® blocks
  - 32 output enables
  - 100-, 144-, 160-, and 208-pin package options
- **System design considerations**
  - PCI compliant (-7, -10, -12 speed grades)
  - JTAG (IEEE 1149.1) boundary scan testing
  - In-system programmable
  - 5-V devices will not overdrive 3-V inputs (safe for mixed voltage)
  - Safe for board hot socketing
  - Bus-Friendly™ I/Os
  - Individual Output slew rate control
  - Programmable security fuse
- **Leading-edge 0.5-µm (L_{eff}) EECMOS process technology**
- **Supported by AMD software**
  - DSL design entry ports to universal tools
  - Low-cost entry-level tool
  - Windows GUI interface
  - Auto device selection
  - Multiple device partitioning
- **Extensive universal tool support**
  - Aldec
  - Cadence
  - Mentor Graphics
  - MicroSim
  - MINC
  - Synario
  - Synopsys/Logic Modeling
  - Viewlogic
- **Third-party programming support**

GENERAL DESCRIPTION

The MACH5-256 (M5-256) is a member of AMD's MACH 5 family and offers the innovations of the family's fifth generation complex programmable logic device (CPLD) architecture. The M5-256 features the family's unprecedented combination of high speed (7.5-ns pin-to-pin delays and counter speeds up to 125 MHz), density (10,000 PLD gates), and predictable timing. The M5-256's system performance capabilities—such as full compliance with the *PCI Local Bus Specification* for the -7/-10/-12 speed grades, JTAG boundary scan testing, in-system programming, advanced power management, and 3.3-V friendly I/Os—will meet designers' critical design requirements today and tomorrow. The M5-256 is fabricated with AMD's leading-edge 0.5-µm EECMOS process in AMD's state-of-the-art, ISO 9000 qualified manufacturing facilities, assuring high quality and availability.

All devices are available with pin-to-pin delays as fast as 7.5 ns and possess the density required for full system logic integration. The MACH 5 family's unique hierarchical architecture is ideal for PAL device integration and a wide range of other applications including high-speed computing, low-power applications, communications, and embedded control.

Several features have been incorporated to accommodate changing designs and fixed pinout. The routing resources include a logic switch matrix which reassigns logic to macrocells. Often designers may need to incorporate additional logic in their designs without moving to a larger package. The MACH 5 Macrocell/Package

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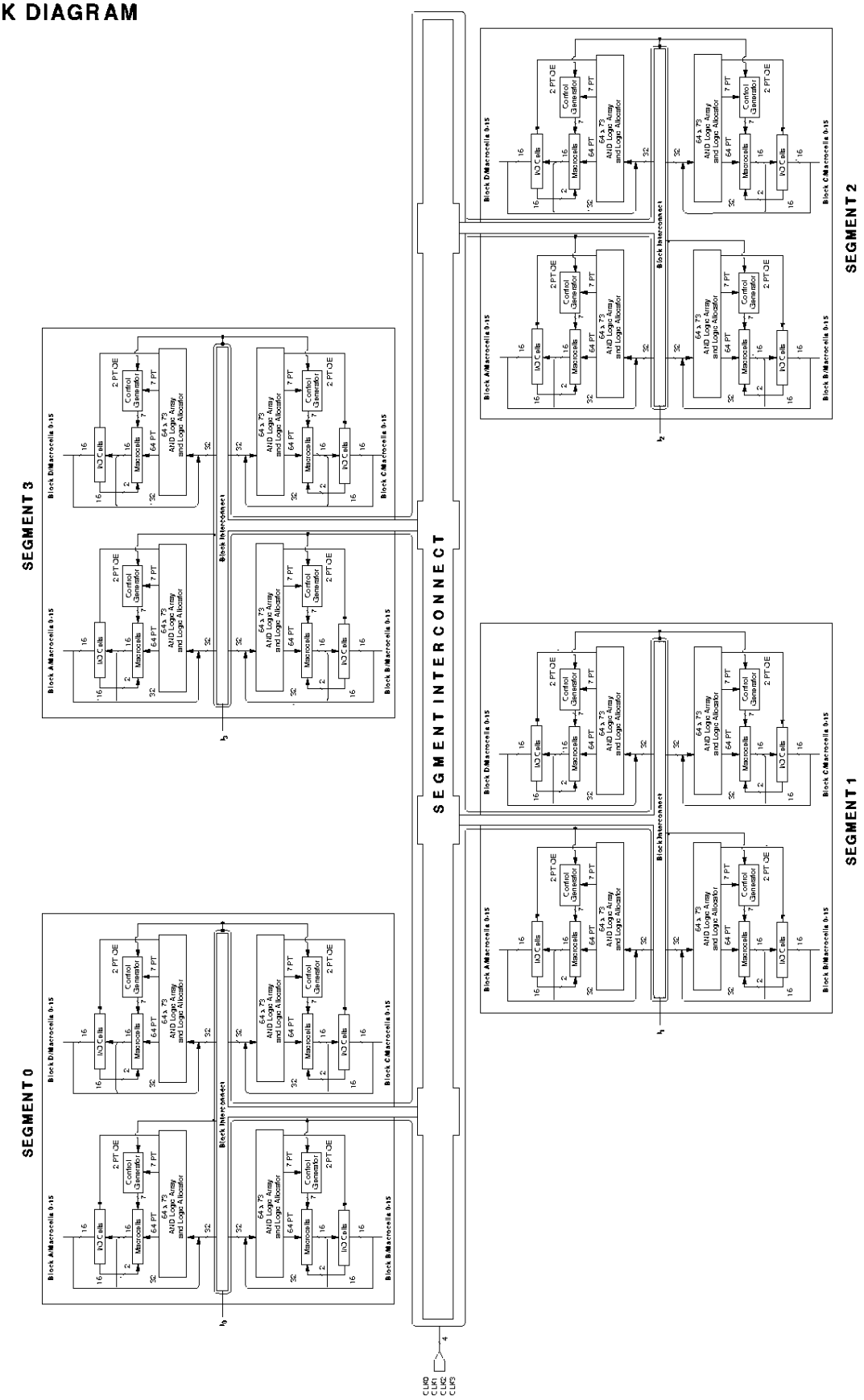
options are designed for such an occurrence. Any two MACH 5 logic densities in the same package have the same pinout to eliminate wasted logic and to provide a migration path when more logic is required.

MACH designs can be implemented using industry-standard, universal design tools. AMD and universal fitter company, MINC, Inc., have developed a strategic partnership that ensures timely universal software support for the MACH 5. MINC develops back-end PLD software for nearly every major industry-standard PLD and board-level design tool. This back-end software fits a design into a device and creates a JEDEC file. Schematic capture, boolean, state machine, VHDL, and Verilog design entry and simulation are features of the front-end tool. MINC produces the back-end for PC tools such as MicroSim's Design Center, Synario Design Automation's Synario, and others. MINC also supplies the back-end for workstation tools from Cadence, Mentor Graphics, Synopsys, and Viewlogic. Thus, the AMD-MINC partnership provides timely, accurate, and quality support for MACH devices in almost every design environment. Please see AMD's Universal Tools brochure for more information.

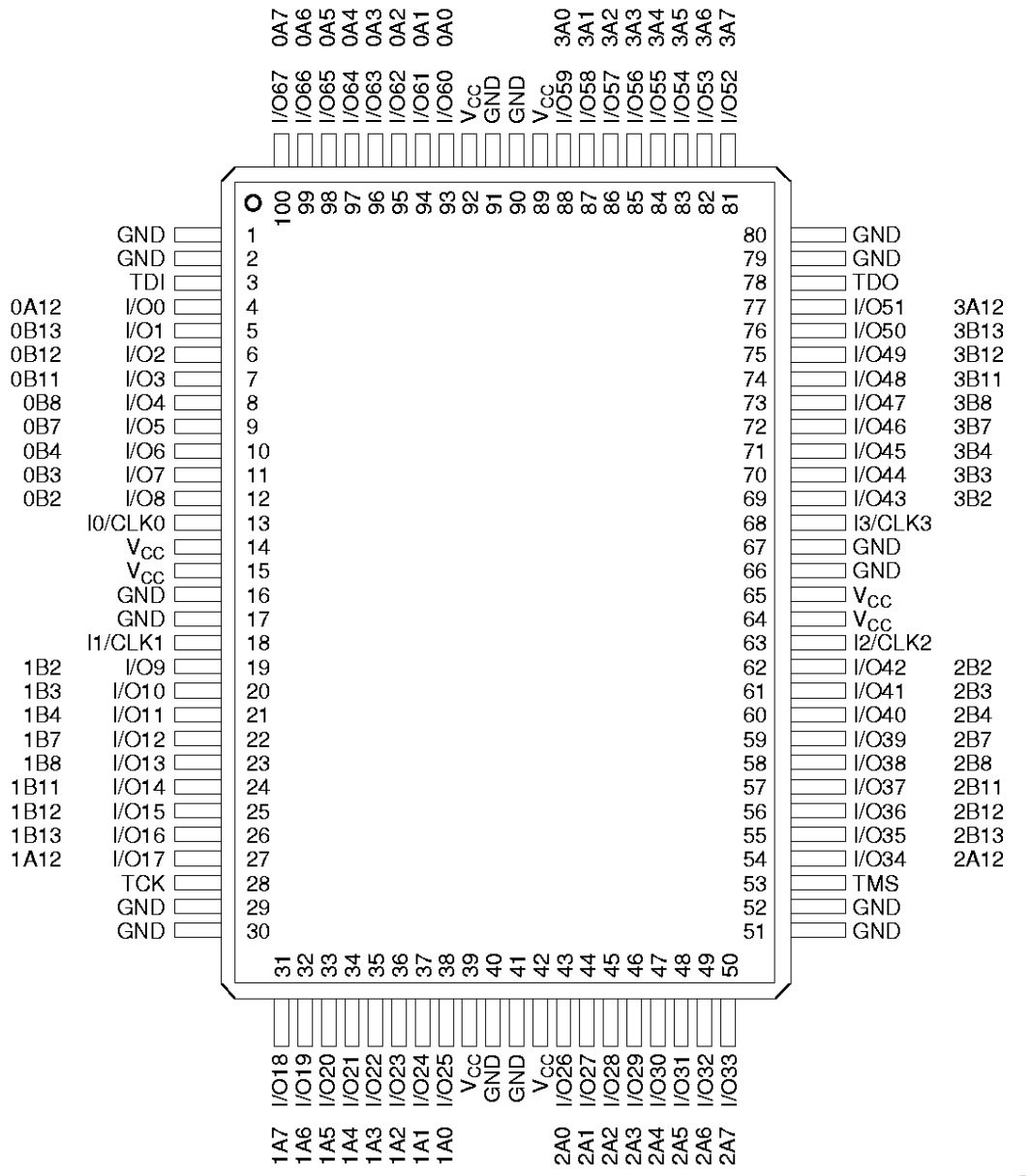
BLOCK DIAGRAM



20796C-1

CONNECTION DIAGRAMS

Top View

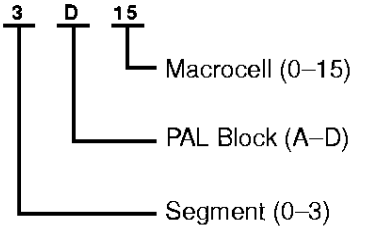


20796C-2

100 PQFP

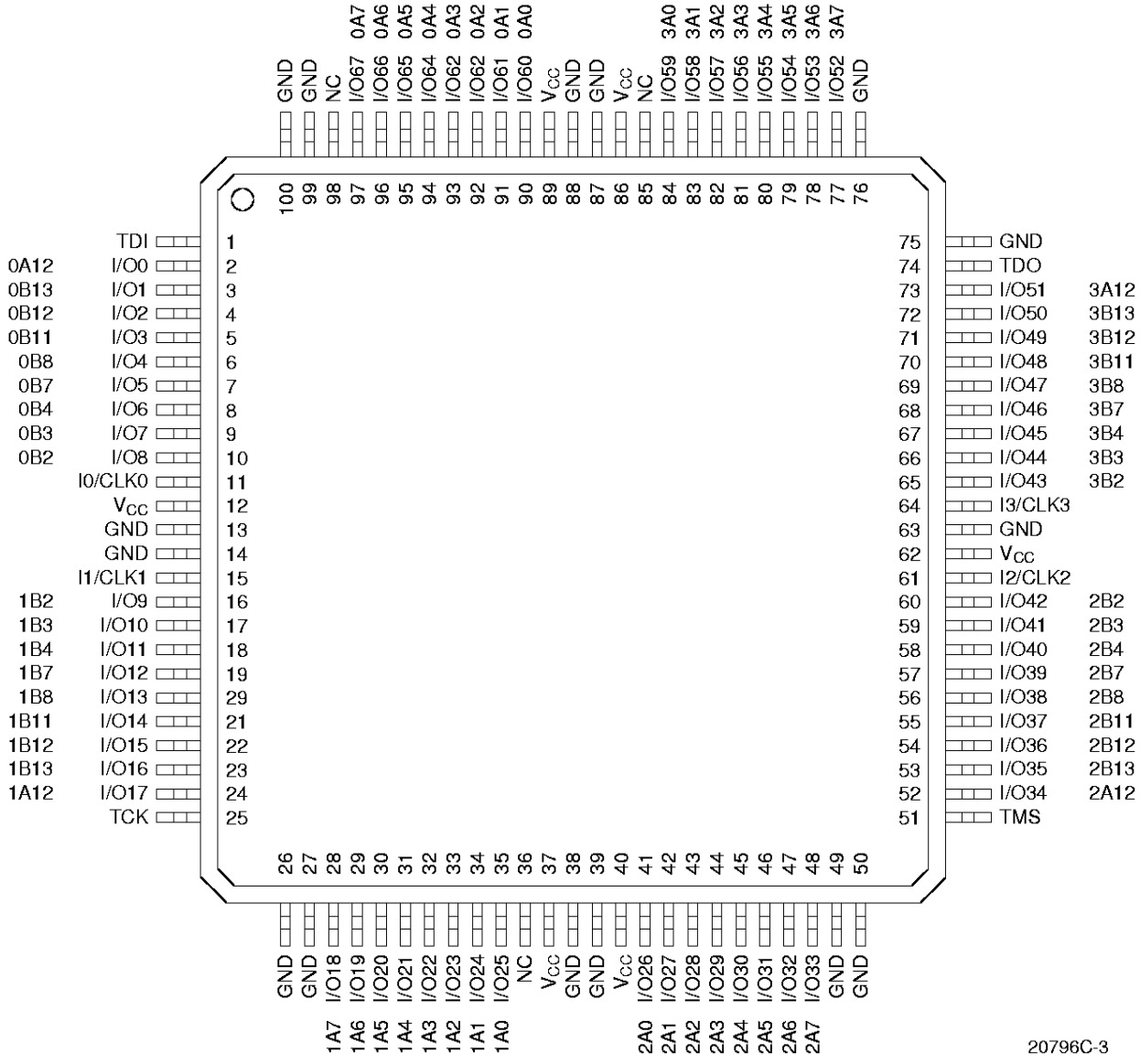
PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
V_{CC} = Supply Voltage



CONNECTION DIAGRAMS (continued)

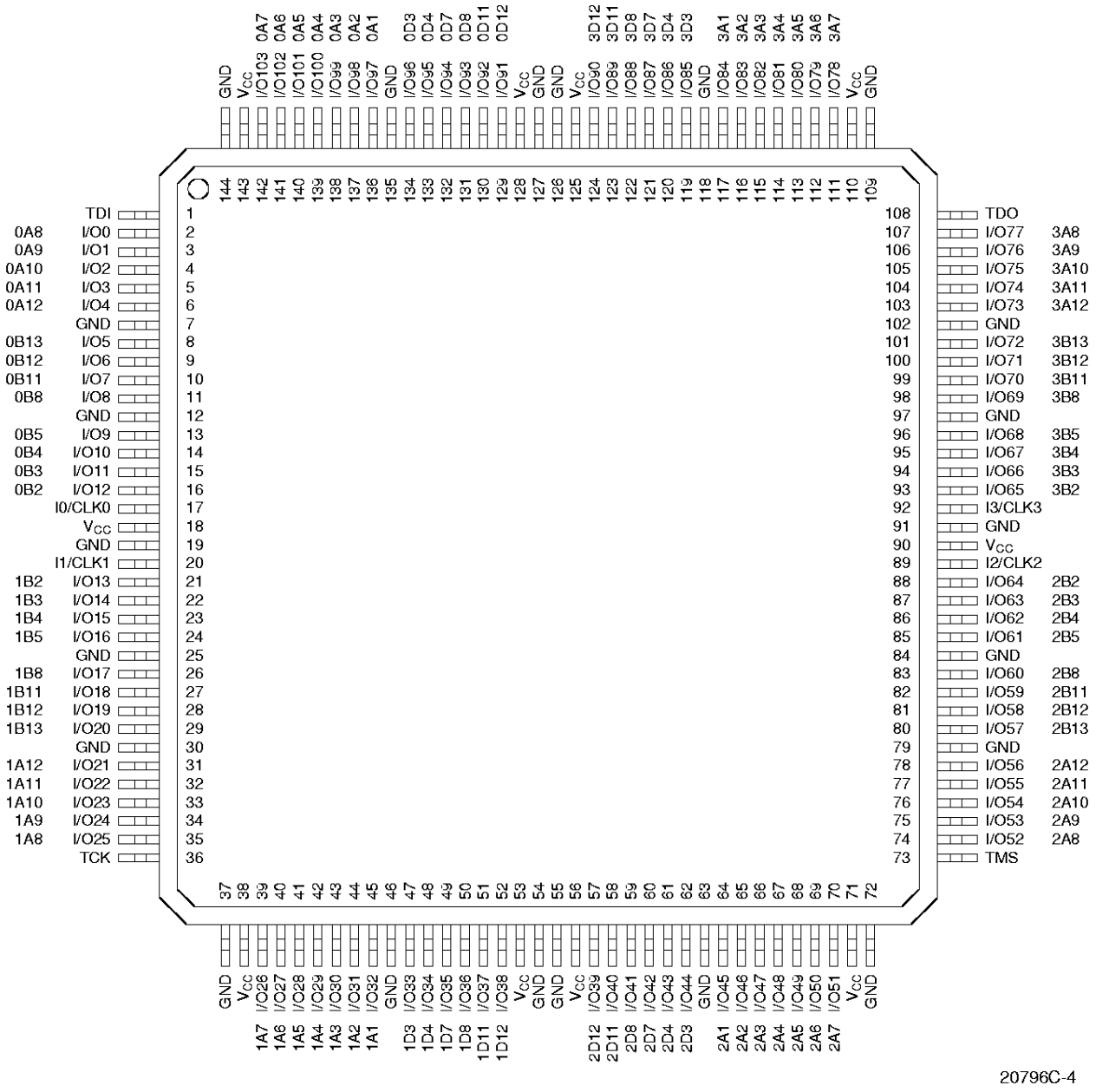
Top View



100 TQFP

CONNECTION DIAGRAMS (continued)

Top View

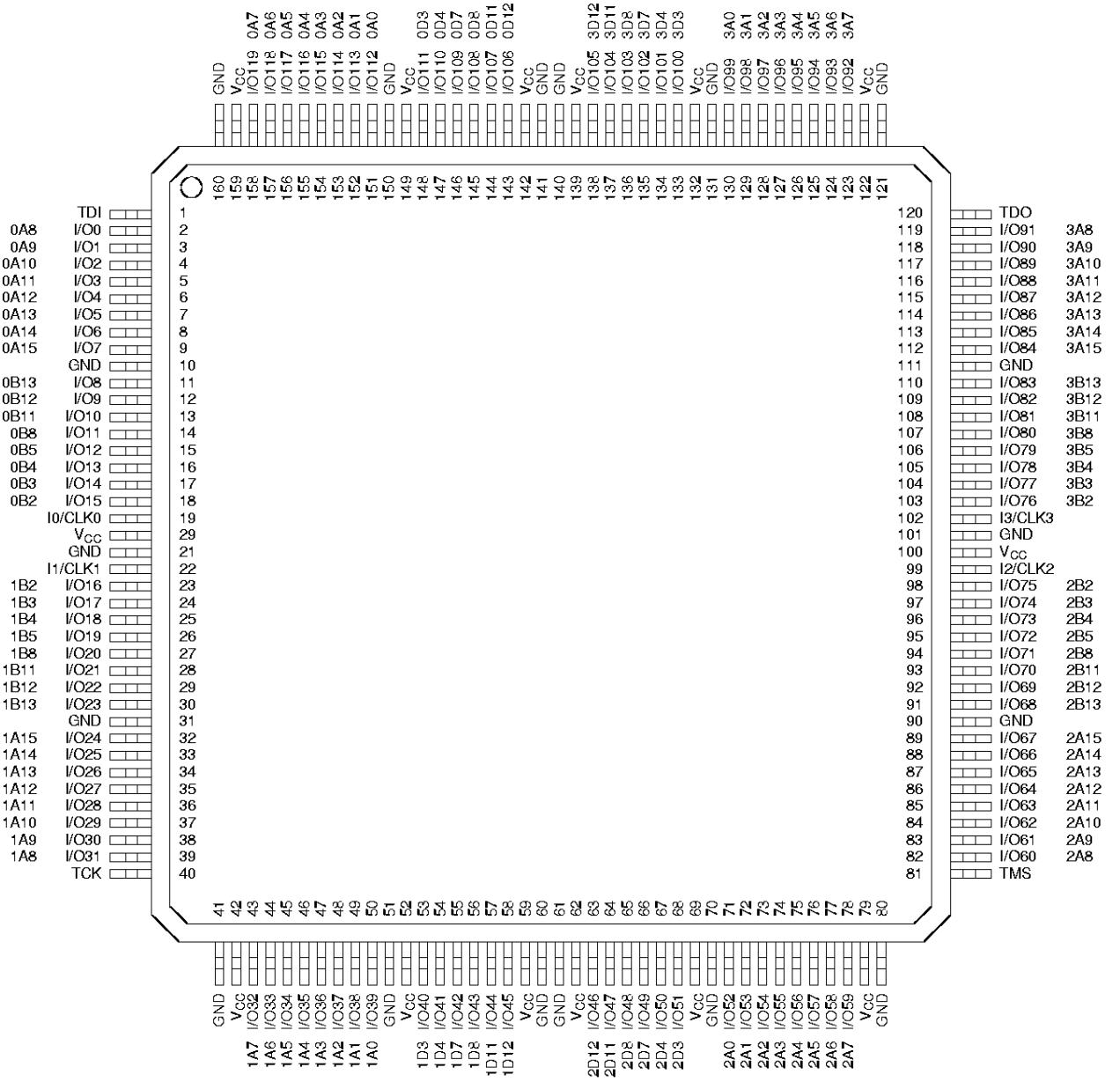


20796C-4

144 PQFP

CONNECTION DIAGRAMS (continued)

Top View

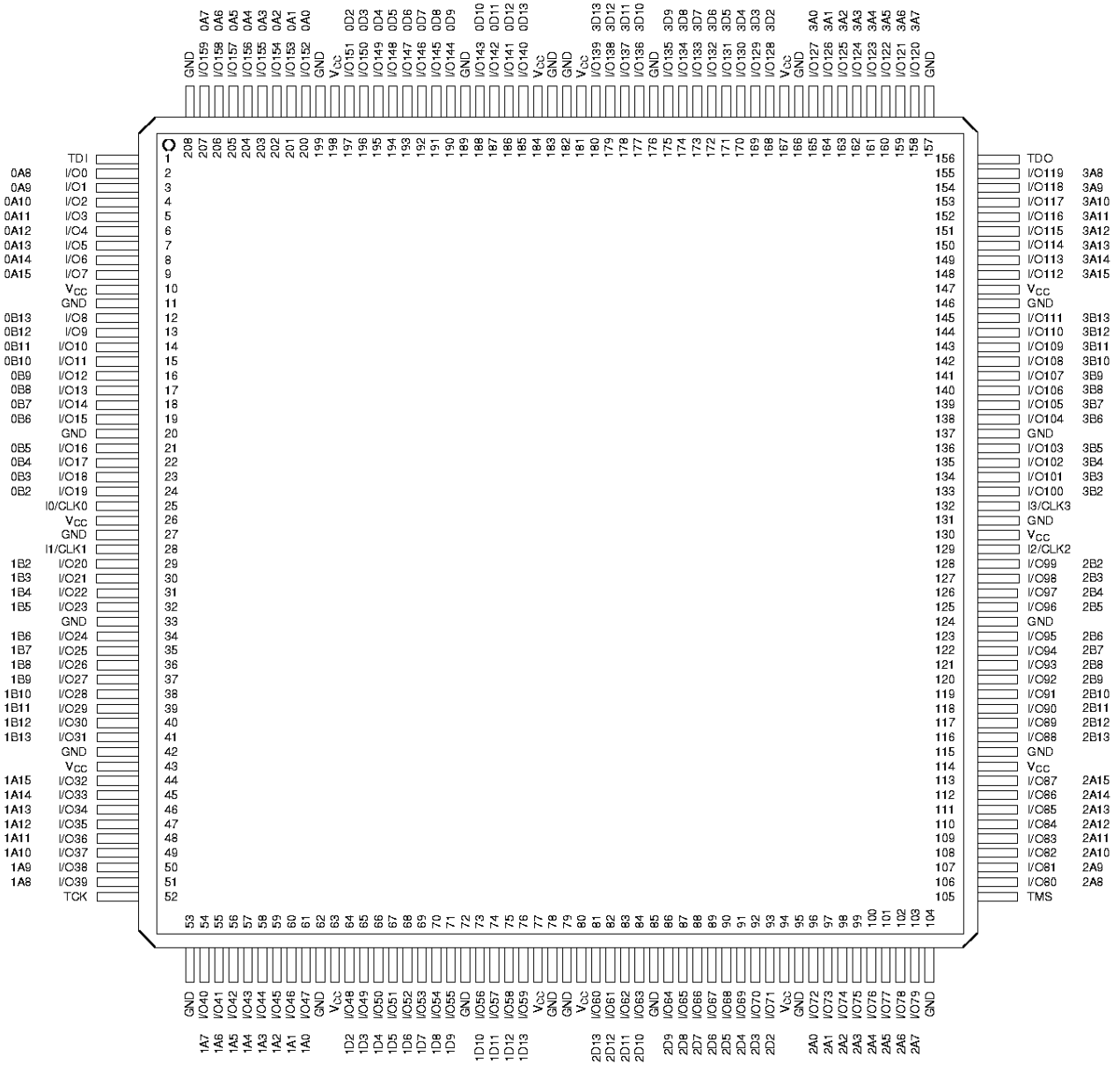


20796C-5

160 PQFP

CONNECTION DIAGRAMS (continued)

Top View



20796C-6

208 PQFP

PIN-OUT TABLE

Listed By Pin Number

PACKAGE PIN	100 TQFP SEG/BLK/MC	100 PQFP SEG/BLK/MC	144 PQFP SEG/BLK/MC	160 PQFP SEG/BLK/MC	208 PQFP SEG/BLK/MC
1	TDI	GND	TDI	TDI	TDI
2	0A12	GND	0A8	0A8	0A8
3	0B13	TDI	0A9	0A9	0A9
4	0B12	0A12	0A10	0A10	0A10
5	0B11	0B13	0A11	0A11	0A11
6	0B8	0B12	0A12	0A12	0A12
7	0B7	0B11	GND	0A13	0A13
8	0B4	0B8	0B13	0A14	0A14
9	0B3	0B7	0B12	0A15	0A15
10	0B2	0B4	0B11	GND	VCC
11	CLOCK0	0B3	0B8	0B13	GND
12	VCC	0B2	GND	0B12	0B13
13	GND	CLOCK0	0B5	0B11	0B12
14	GND	VCC	0B4	0B8	0B11
15	CLOCK1	VCC	0B3	0B5	0B10
16	1B2	GND	0B2	0B4	0B9
17	1B3	GND	CLOCK0	0B3	0B8
18	1B4	CLOCK1	VCC	0B2	0B7
19	1B7	1B2	GND	CLOCK0	0B6
20	1B8	1B3	CLOCK1	VCC	GND
21	1B11	1B4	1B2	GND	0B5
22	1B12	1B7	1B3	CLOCK1	0B4
23	1B13	1B8	1B4	1B2	0B3
24	1A12	1B11	1B5	1B3	0B2
25	TCK	1B12	GND	1B4	CLOCK0
26	GND	1B13	1B8	1B5	VCC
27	GND	1A12	1B11	1B8	GND
28	1A7	TCK	1B12	1B11	CLOCK1
29	1A6	GND	1B13	1B12	1B2
30	1A5	GND	GND	1B13	1B3
31	1A4	1A7	1A12	GND	1B4
32	1A3	1A6	1A11	1A15	1B5
33	1A2	1A5	1A10	1A14	GND
34	1A1	1A4	1A9	1A13	1B6
35	1A0	1A3	1A8	1A12	1B7
36	NC	1A2	TCK	1A11	1B8
37	VCC	1A1	GND	1A10	1B9
38	GND	1A0	VCC	1A9	1B10
39	GND	VCC	1A7	1A8	1B11
40	VCC	GND	1A6	TCK	1B12
41	2A0	GND	1A5	GND	1B13
42	2A1	VCC	1A4	VCC	GND
43	2A2	2A0	1A3	1A7	VCC
44	2A3	2A1	1A2	1A6	1A15
45	2A4	2A2	1A1	1A5	1A14
46	2A5	2A3	GND	1A4	1A13
47	2A6	2A4	1D3	1A3	1A12
48	2A7	2A5	1D4	1A2	1A11

PIN-OUT TABLE

Listed By Pin Number (continued)

PACKAGE PIN	100 TQFP SEG/BLK/MC	100 PQFP SEG/BLK/MC	144 PQFP SEG/BLK/MC	160 PQFP SEG/BLK/MC	208 PQFP SEG/BLK/MC
49	GND	2A6	1D7	1A1	1A10
50	GND	2A7	1D8	1A0	1A9
51	TMS	GND	1D11	GND	1A8
52	2A12	GND	1D12	VCC	TCK
53	2B13	TMS	VCC	1D3	GND
54	2B12	2A12	GND	1D4	1A7
55	2B11	2B13	GND	1D7	1A6
56	2B8	2B12	VCC	1D8	1A5
57	2B7	2B11	2D12	1D11	1A4
58	2B4	2B8	2D11	1D12	1A3
59	2B3	2B7	2D8	VCC	1A2
60	2B2	2B4	2D7	GND	1A1
61	CLOCK2	2B3	2D4	GND	1A0
62	VCC	2B2	2D3	VCC	GND
63	GND	CLOCK2	GND	2D12	VCC
64	CLOCK3	VCC	2A1	2D11	1D2
65	3B2	VCC	2A2	2D8	1D3
66	3B3	GND	2A3	2D7	1D4
67	3B4	GND	2A4	2D4	1D5
68	3B7	CLOCK3	2A5	2D3	1D6
69	3B8	3B2	2A6	VCC	1D7
70	3B11	3B3	2A7	GND	1D8
71	3B12	3B4	VCC	2A0	1D9
72	3B13	3B7	GND	2A1	GND
73	3A12	3B8	TMS	2A2	1D10
74	TDO	3B11	2A8	2A3	1D11
75	GND	3B12	2A9	2A4	1D12
76	GND	3B13	2A10	2A5	1D13
77	3A7	3A12	2A11	2A6	VCC
78	3A6	TDO	2A12	2A7	GND
79	3A5	GND	GND	VCC	GND
80	3A4	GND	2B13	GND	VCC
81	3A3	3A7	2B12	TMS	2D13
82	3A2	3A6	2B11	2A8	2D12
83	3A1	3A5	2B8	2A9	2D11
84	3A0	3A4	GND	2A10	2D10
85	NC	3A3	2B5	2A11	GND
86	VCC	3A2	2B4	2A12	2D9
87	GND	3A1	2B3	2A13	2D8
88	GND	3A0	2B2	2A14	2D7
89	VCC	VCC	CLOCK2	2A15	2D6
90	0A0	GND	VCC	GND	2D5
91	0A1	GND	GND	2B13	2D4
92	0A2	VCC	CLOCK3	2B12	2D3
93	0A3	0A0	3B2	2B11	2D2
94	0A4	0A1	3B3	2B8	VCC
95	0A5	0A2	3B4	2B5	GND
96	0A6	0A3	3B5	2B4	2A0

PIN-OUT TABLE

Listed By Pin Number (continued)

PACKAGE PIN	100 TQFP SEG/BLK/MC	100 PQFP SEG/BLK/MC	144 PQFP SEG/BLK/MC	160 PQFP SEG/BLK/MC	208 PQFP SEG/BLK/MC
97	0A7	0A4	GND	2B3	2A1
98	NC	0A5	3B8	2B2	2A2
99	GND	0A6	3B11	CLOCK2	2A3
100	GND	0A7	3B12	VCC	2A4
101			3B13	GND	2A5
102			GND	CLOCK3	2A6
103			3A12	3B2	2A7
104			3A11	3B3	GND
105			3A10	3B4	TMS
106			3A9	3B5	2A8
107			3A8	3B8	2A9
108			TDO	3B11	2A10
109			GND	3B12	2A11
110			VCC	3B13	2A12
111			3A7	GND	2A13
112			3A6	3A15	2A14
113			3A5	3A14	2A15
114			3A4	3A13	VCC
115			3A3	3A12	GND
116			3A2	3A11	2B13
117			3A1	3A10	2B12
118			GND	3A9	2B11
119			3D3	3A8	2B10
120			3D4	TDO	2B9
121			3D7	GND	2B8
122			3D8	VCC	2B7
123			3D11	3A7	2B6
124			3D12	3A6	GND
125			VCC	3A5	2B5
126			GND	3A4	2B4
127			GND	3A3	2B3
128			VCC	3A2	2B2
129			0D12	3A1	CLOCK2
130			0D11	3A0	VCC
131			0D8	GND	GND
132			0D7	VCC	CLOCK3
133			0D4	3D3	3B2
134			0D3	3D4	3B3
135			GND	3D7	3B4
136			0A1	3D8	3B5
137			0A2	3D11	GND
138			0A3	3D12	3B6
139			0A4	VCC	3B7
140			0A5	GND	3B8
141			0A6	GND	3B9
142			0A7	VCC	3B10
143			VCC	0D12	3B11
144			GND	0D11	3B12

PIN-OUT TABLE

Listed By Pin Number (continued)

PACKAGE PIN	100 TQFP SEG/BLK/MC	100 PQFP SEG/BLK/MC	144 PQFP SEG/BLK/MC	160 PQFP SEG/BLK/MC	208 PQFP SEG/BLK/MC
145				0D8	3B13
146				0D7	GND
147				0D4	VCC
148				0D3	3A15
149				VCC	3A14
150				GND	3A13
151				0A0	3A12
152				0A1	3A11
153				0A2	3A10
154				0A3	3A9
155				0A4	3A8
156				0A5	TDO
157				0A6	GND
158				0A7	3A7
159				VCC	3A6
160				GND	3A5
161					3A4
162					3A3
163					3A2
164					3A1
165					3A0
166					GND
167					VCC
168					3D2
169					3D3
170					3D4
171					3D5
172					3D6
173					3D7
174					3D8
175					3D9
176					GND
177					3D10
178					3D11
179					3D12
180					3D13
181					VCC
182					GND
183					GND
184					VCC
185					0D13
186					0D12
187					0D11
188					0D10
189					GND
190					0D9
191					0D8
192					0D7

PIN-OUT TABLE

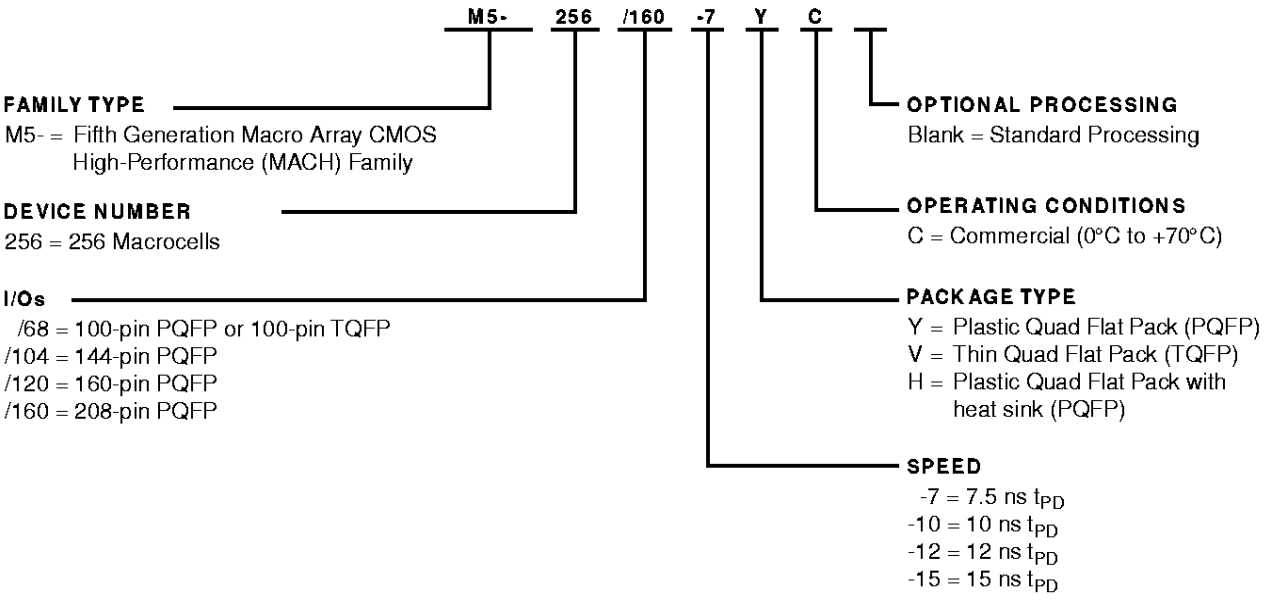
Listed By Pin Number (continued)

PACKAGE PIN	100 TQFP SEG/BLK/MC	100 PQFP SEG/BLK/MC	144 PQFP SEG/BLK/MC	160 PQFP SEG/BLK/MC	208 PQFP SEG/BLK/MC
193					0D6
194					0D5
195					0D4
196					0D3
197					0D2
198					VCC
199					GND
200					0A0
201					0A1
202					0A2
203					0A3
204					0A4
205					0A5
206					0A6
207					0A7
208					GND

ORDERING INFORMATION

MACH 5 COM -7.5, -10, -12, -15

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
M5-256/68	-7, -10, -12, -15	YC, VC
M5-256/104		YC
M5-256/120		YC
M5-256/160		HC

Device Marking

Actual device marking differs from the ordering part number (OPN). "MACH 5" is marked on a device wherever "M5-" is used in the OPN.

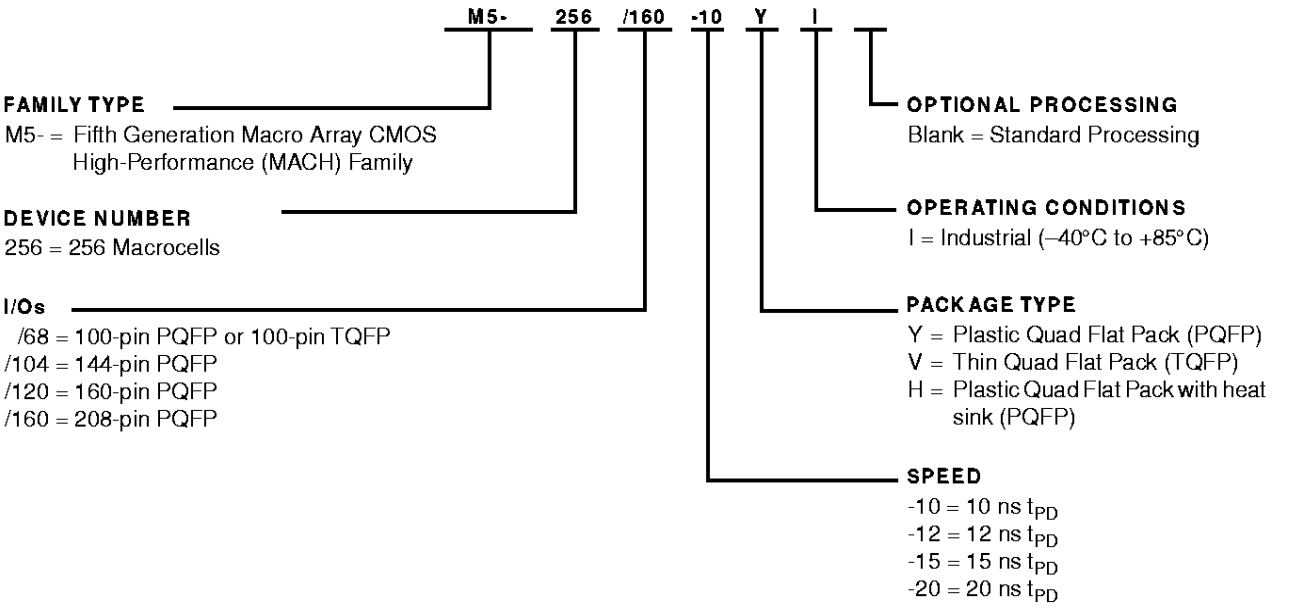
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

MACH 5 IND -10, -12, -15, -20

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
M5-256/68	-10, -12, -15, -20	YI, VI
M5-256/104		YI
M5-256/120		YI
M5-256/160		HI

Device Marking

Actual device marking differs from the ordering part number (OPN). "MACH 5" is marked on a device wherever "M5-" is used in the OPN.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The Fifth Generation MACH Architecture yields the highest speeds at the highest CPLD densities. Excellent routing resources ensure pinout retention as well as high utilization. The MACH 5 architecture consists of PAL blocks connected by two levels of interconnect. Each group of four PAL blocks is given its own routing resources, called **block interconnect**. Together, the four PAL blocks and their block interconnect are called a **segment**. The second level of interconnect, the **segment interconnect**, ties all of the segments together (see Figure 1). The only logic difference between any two MACH 5 devices is the number of segments, so once a designer is familiar with one device, consistent performance can be expected across the entire family. All devices have four pin clocks available which can also be used as logic inputs. If these pins are used as logic inputs, they are fed directly to the block interconnect of specific segments. For the M5-256, I0 is connected to the block interconnect of segment 0, I1 to the block interconnect of segment 1, I2 to the block interconnect of segment 2, and I3 to the block interconnect of segment 3.

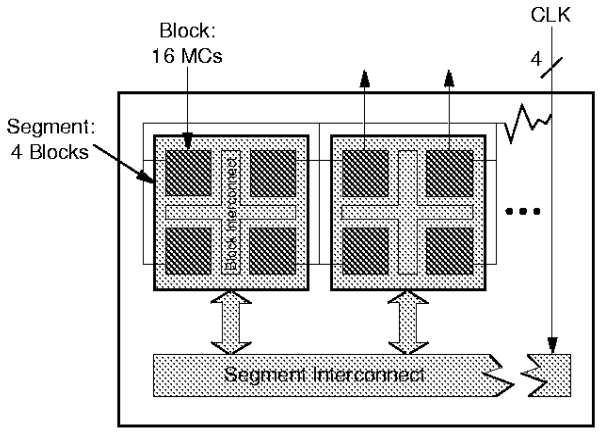


Figure 1. MACH 5 Block Diagram with Segment Numbers

Enhanced PAL Block

The MACH 5 PAL blocks consist of the elements listed below. While each PAL block resembles an independent PAL device, it has superior control and logic generation capabilities.

- Macrocell
- Logic array
- Logic allocator
- I/O cell
- Register control generator
- Output enable generator

The I/Os associated with each PAL block (Figure 2) have a path directly back to that PAL block called **local feedback**. When the I/O is used in another PAL block, the **interconnect feeder** assigns a **block interconnect** line to that signal. The interconnect feeder acts as an input switch matrix. The block and segment interconnect provide connections between any two signals in a device. The **block feeder** assigns block interconnect lines and local feedback lines to the PAL block inputs. Two inputs per PAL block can also be fed directly to a macrocell for registered input applications.

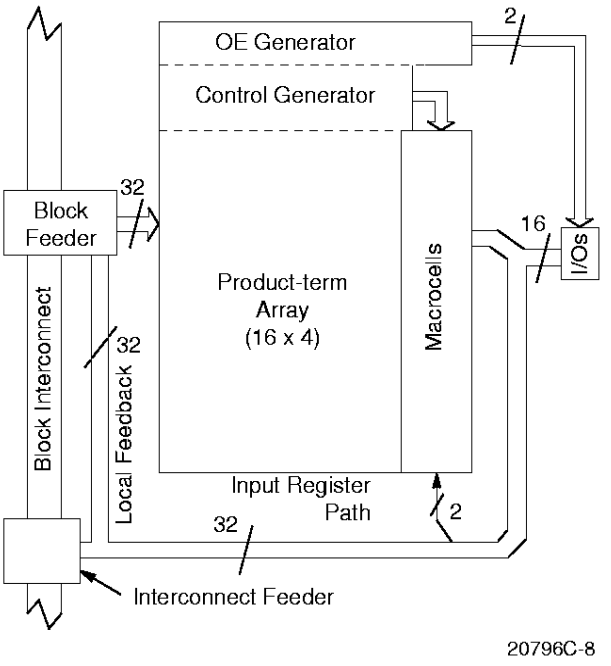


Figure 2. PAL Block Structure

Logic Array and Allocator

The product-term array has the familiar sum-of-products architecture used in PAL devices. The logic allocator assigns product terms to macrocells. Up to eight clusters of four product terms can be steered to one macrocell, and product terms can be steered in a basic cluster of three or four product terms. If three product terms are steered away, one can be left for separate logic generation. The logic allocator acts as an output logic switch matrix: as a design changes, the **logic allocator** will reassign logic to macrocells to retain pinout. If not used in a cluster, the extra product term can be XORed with the basic cluster for functions such as data comparison. If the basic cluster of three product terms is steered away, the product term remaining can still be used for logic generation. The XOR gate available to each macrocell can be used for logic and/or for polarity control. The product term clusters available to each macrocell within a PAL block are shown in Table 1.

Rather than an output switch matrix which reassigns macrocells to pins to retain pinout, the wide logic allocator produces the same result by reassigning logic to macrocells. In addition, large equations (up to 32 product terms) can be implemented in a MACH 5 device with only one pass through the logic array.

Table 1. Product Term Steering Options for PT Clusters and Macrocells

Macrocell	Available Clusters
MC0	C0, C1, C2, C3, C4
MC1	C0, C1, C2, C3, C4, C5
MC2	C0, C1, C2, C3, C4, C5, C6
MC3	C0, C1, C2, C3, C4, C5, C6, C7
MC4	C0, C1, C2, C3, C4, C5, C6, C7
MC5	C1, C2, C3, C4, C5, C6, C7, C8
MC6	C2, C3, C4, C5, C6, C7, C8, C9
MC7	C3, C4, C5, C6, C7, C8, C9, C10
MC8	C5, C6, C7, C8, C9, C10, C11, C12
MC9	C6, C7, C8, C9, C10, C11, C12, C13
MC10	C7, C8, C9, C10, C11, C12, C13, C14
MC11	C8, C9, C10, C11, C12, C13, C14, C15
MC12	C8, C9, C10, C11, C12, C13, C14, C15
MC13	C9, C10, C11, C12, C13, C14, C15
MC14	C10,C11, C12, C13, C14, C15
MC15	C11, C12, C13, C14, C15

Macrocells

The macrocells for MACH 5 consist of a storage element, a control (clock and set or reset or latch enable) bus, and routing resources. The macrocell (Figure 3) and can be configured for combinatorial, registered or latched operation. The D-type flip-flops can be configured as T-type, J-K, or S-R operation through the use of the XOR gate associated with each macrocell.

Control Generator

The control generator provides four configurable clock lines and three configurable set/reset lines to each macrocell in a PAL block. Any of the four clock lines and any of the three set/reset lines can be independently selected by any flip-flop within a block. The clock lines (Figure 4) provide global (pin) clocks, product term clocks, sum term clocks, and latch enables. Positive or negative edge clocking is available as well as advanced clocking features such as **complementary** and **biphase** clocking. Complementary clocking provides two clock lines exactly 180 degrees out of phase, and is useful in applications such as fast data paths. A biphase clock line clocks flip-flops on both the positive and negative edges of the clock. The configuration options for the four clock lines per PAL block are as follows:

Clock Line 0 Options

- Global clock (0, 1, 2, or 3) with clock enable, clocked on the positive or negative edge of the clock
- Product-term clock (A*B*C)
- Sum-term clock (A+B+C)

Clock Line 1 Options

- Global clock (0, 1, 2, or 3) with positive edge clock enable
- Global clock (0, 1, 2, or 3) with negative edge clock enable
- Global clock (0, 1, 2, or 3) with positive and negative edge clock enable (biphase)

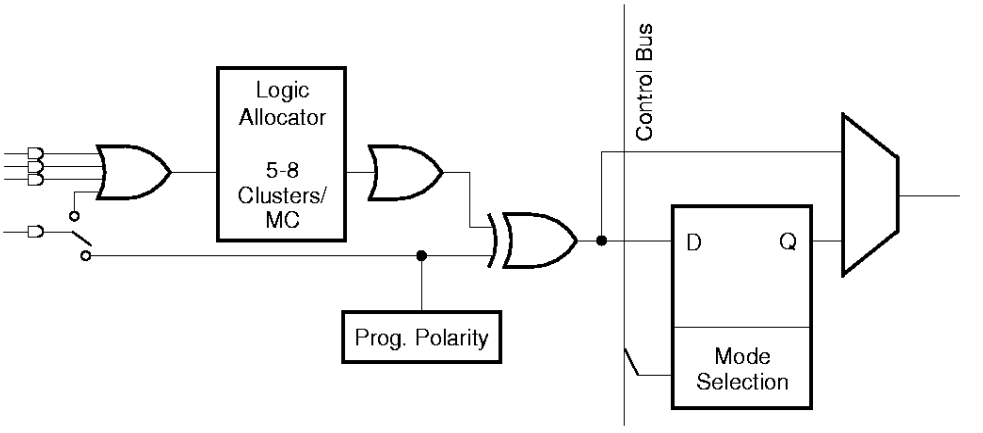


Figure 3. Macrocell Diagram

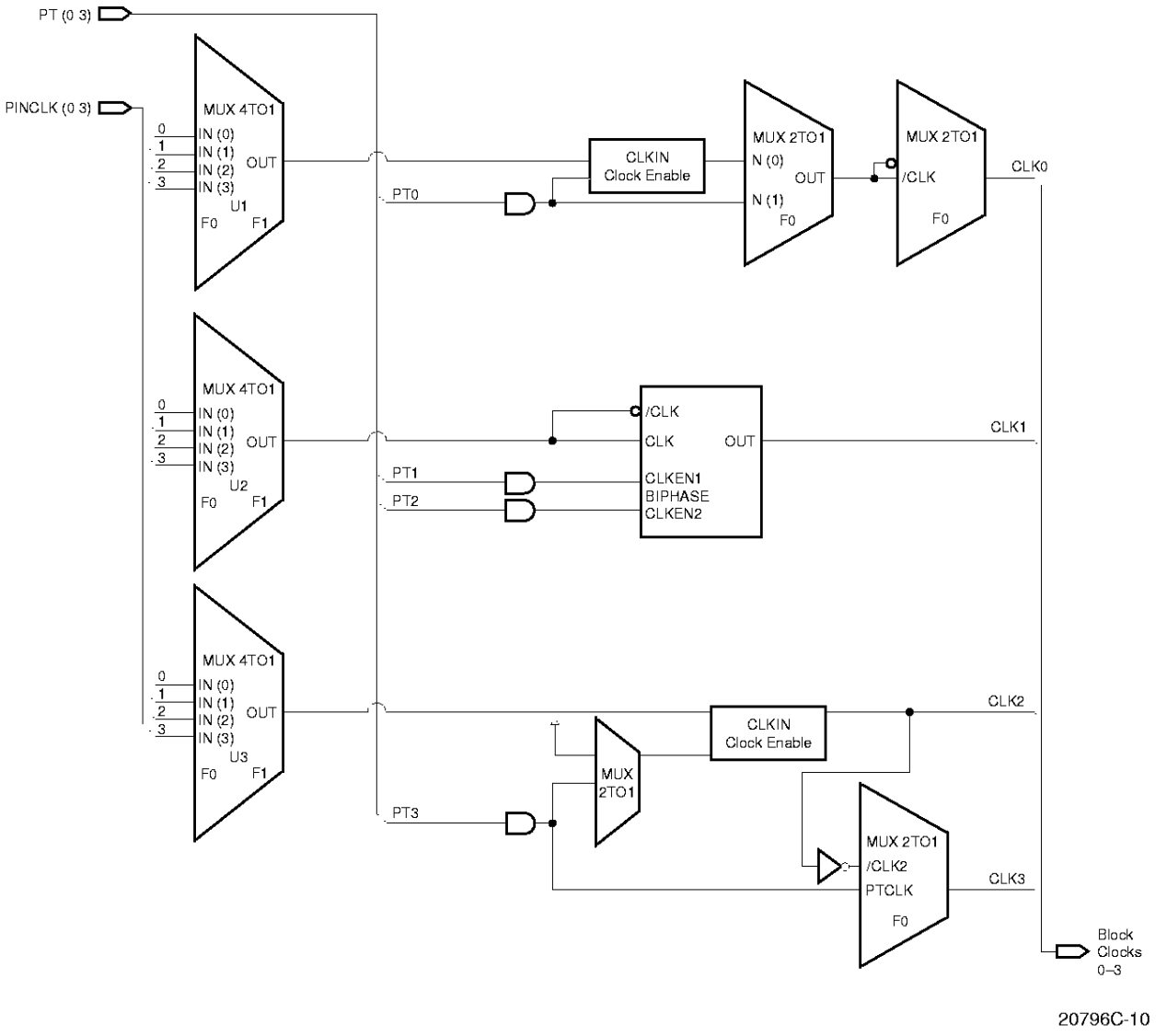


Figure 4. Clock Generator

Clock Line 2 Options

- Global clock (0, 1, 2, or 3) with clock enable

Clock Line 3 Options

- Complement of clock line 2 (same clock enable)
- Product-term clock (if clock line 2 does not use clock enable

Three of the four global clocks are available within any given PAL block. There are two product-term clocks and one sum-term clock available per PAL block.

The set/reset generation portion of the control generator (Figure 5) creates three set/reset lines for the PAL block. Each macrocell can choose one of these three lines or choose no set/reset at all. All three lines can be configured for product term set/reset and two of the three lines can be configured as sum term set/reset and one of the lines can be configured as product-term or sum-term latch enable. While the set/reset signals are generated in the control generator, whether that signal sets or resets a flip-flop is determined within the individual macrocell. The same signal can set one flip-flop and reset another. PT2 or /PT2 can also be used as a latch enable for macrocells configured as latches.

OE Generator

There is one output enable (OE) generator per PAL block that generates two product-term driven output enables. Each I/O cell is simply an output buffer. Each macrocell within the PAL block can choose to be permanently enabled, permanently disabled, or choose one of the two product term output enables per PAL block (Figure 6).

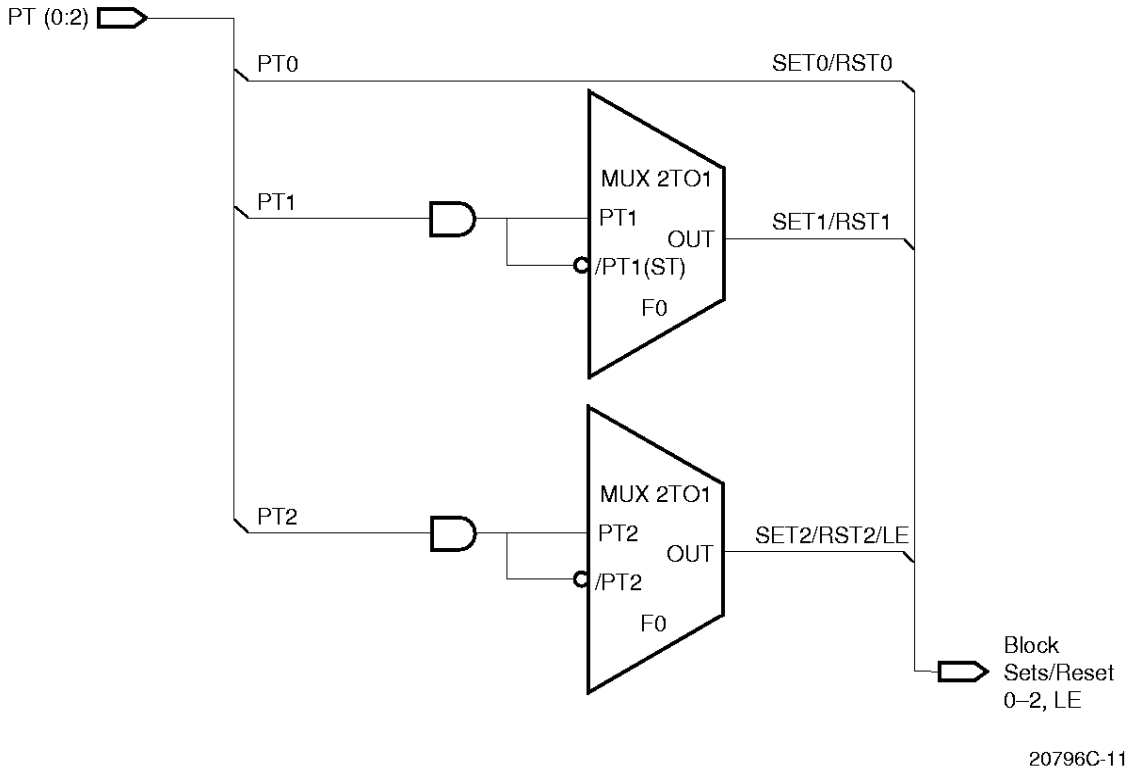


Figure 5. Set/Reset Generator

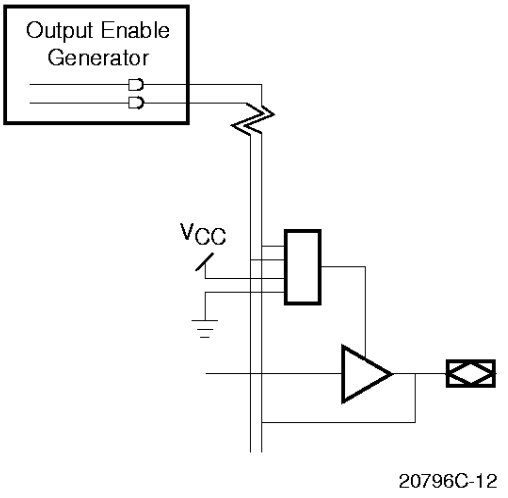


Figure 6. Output Enable Generator and I/O Cell

MACH 5 TIMING

MACH 5 timing can be modeled on any AMD approved software tool or it can be estimated using the model shown in Figure 7. Device timing will depend on the level of interconnect used and the power level chosen for a particular path. These are the path and power factors. The pin-to-pin delays can be calculated by following one path from input/feedback to output. For example, t_{PD} is the pin-to-pin delay for a signal within a PAL block. $t_{PD}+t_{BLK}$ is the pin-to-pin delay for a signal that uses the block interconnect and stays within a segment. $t_{PD}+t_{SEG}$ is the pin-to-pin delay for a signal that uses both the block and segment interconnect. Power level timing is calculated in the same manner. If a signal uses block interconnect and is placed in a low-power block, then the pin-to-pin delay will be $t_{PD}+t_{BLK}+t_{PL3}$.

SAFE FOR MIXED VOLTAGE DESIGNS

The M5-256 is safe for mixed voltage designs. The 5-V device outputs will not drive above 3.3 volts. Also, a MACH 5 device requires only one supply voltage: 5-V for M5 devices. Both the 3.3-V and 5-V versions have the same performance and have only trivial power differences.

BOARD HOT SOCKETING

MACH 5 is ideal for PC add-on cards and other applications in which voltage may be applied to device inputs before V_{CC}. MACH 5 inputs are designed to accept up to 5.5 V on inputs when the supply voltage is at zero without latch-up and without any reliability concerns. During power-up and power-down, all of the I/O are tri-stated so that they will not interfere with other devices, and there is no I/O leakage during power down, so a MACH 5 device can safely be connected to an active bus. These devices are designed to be safe for board hot insertion.

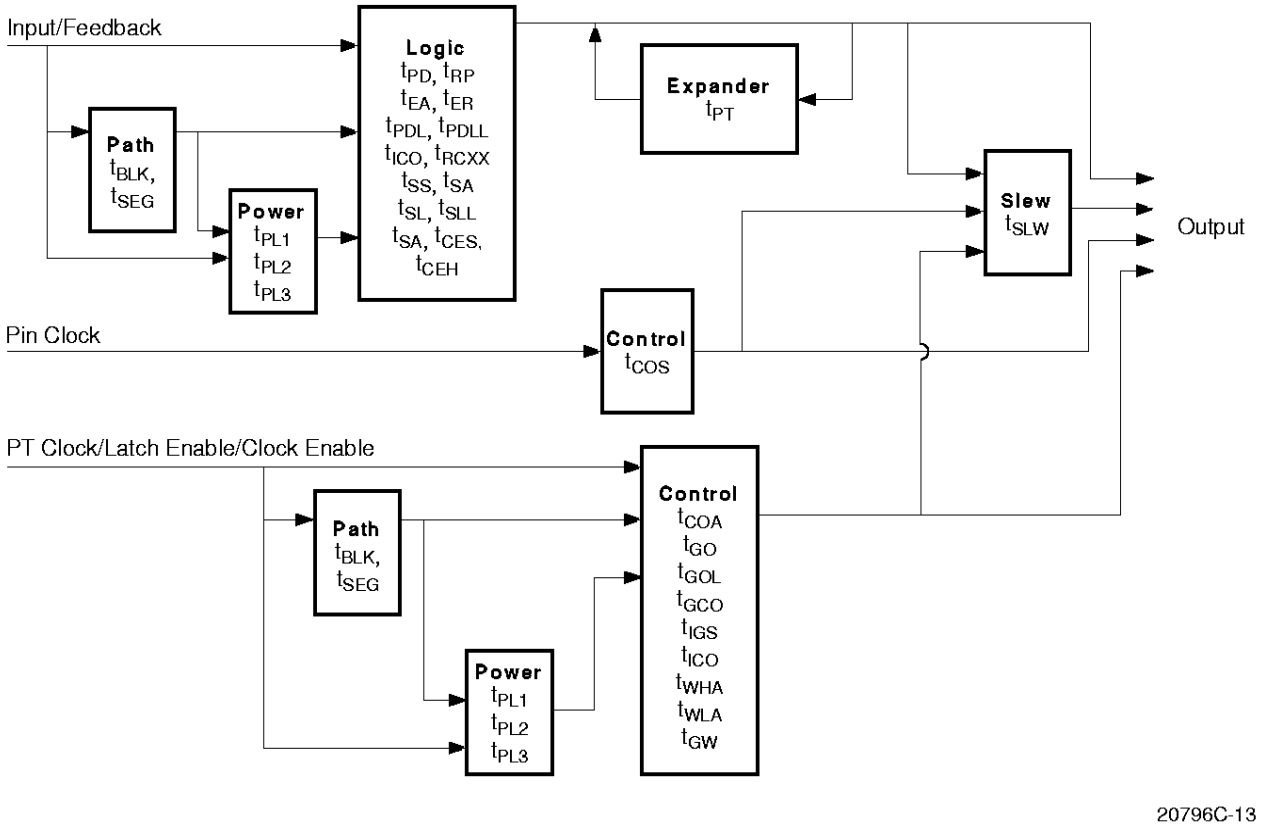


Figure 7. MACH 5 Timing Factors

PCI COMPLIANCE

MACH 5 family members in the -7/-10/-12 speeds are fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group (SIG). MACH 5 devices provide the speed, drive, density and I/Os for the most complex PCI designs. For more information on using MACH for PCI designs please see the application note *PCI Interface Using AMD PLDs.*

MULTIPLE I/O AND DENSITY OPTIONS

As logic needs change during the design process, the MACH 5 family offers six macrocell densities and seven I/O options to optimize cost and functionality concerns.

The MACH 5 family also offers the ability to fit a working design on a member device into another device with the same number of I/Os but a different macrocell density. With proper considerations during design, this feature will allow pins to be fixed in the same locations and require no board reconfiguration.

JTAG, IN-SYSTEM PROGRAMMING

All MACH 5 devices are in-system programmable and are compliant to the JTAG standard, IEEE 1149.1, developed for checking circuit board connectivity. MACH in-system programming is implemented as an extension of this standard which uses manufacturer defined instructions and registers for program and verify. In-system programming eases prototyping and reduces manufacturing steps. MACH 5 devices can be programmed across the commercial temperature range. Minimum programming time is typically less than 5 seconds. For more information on the benefits of in-system programming, please see the application note *Introduction to JTAG and 5-V Programming* included in the 1995 MACH data book. AMD's MACHpro® software serializes JEDEC files and downloads them to the target board through the PC parallel port. MACH 5 devices can be programmed in any JTAG chain.

POWER MANAGEMENT

There are 4 power/speed options in each MACH 5 PAL block. The speed and power tradeoff can be tailored for each design. In large designs, there may be several different speed requirements for different portions of a design. In a computing design, a state machine controller may require the fastest speed available, while the data path portion may run at the slower speed of the bus.

Power level and resulting speed for the 7.5 ns devices

High Speed/High Power	100% power	7.5 ns
Medium High Speed/Medium High Power	67% power	11.5 ns
Medium Low Speed/Medium Low Power	40% power	16.5 ns
Low Speed/Low Power	20% power	25 ns

PROGRAMMABLE SLEW-RATE

Each MACH 5 I/O has an individual programmable slew-rate control bit. Each output can be configured for the highest speed (3 V/ns) or for the lowest noise (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections and less noise. For designs with short traces or well terminated lines, the fast-slew rate can be used to achieve the highest speed. The slew-rate is adjusted independent of power.

POWER UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic and clock must be inactive until the reset delay time has elapsed.

SECURITY

A programmable security bit is provided to prevent unauthorized copying of array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern, securing proprietary designs from competitors. The security bit can only be erased in conjunction with the array during an erase cycle.

QUALITY AND TESTABILITY

MACH 5 devices are electrically erasable which allows for full AC and DC verification of every device. In addition this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

TECHNOLOGY

The MACH 5 devices are fabricated on AMD's own state-of-the-art 0.5 micron (L_{eff}) EECMOS technology. This advanced technology allows MACH 5 to offer both the highest performance CPLDs and the lowest power CPLDs in the industry. The floating gate cells rely on Fowler-Nordheim tunneling to charge the gates, and have a proven record of endurance and reliability.

The substrate of these devices is grounded to provide substrate clamp diodes on every input which makes inputs more immune to noisy input signals.

BUS-FRIENDLY I/O STRUCTURE

All of the MACH 5 devices have a Bus-Friendly input structure which weakly holds an input at its last driven state. While it is good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from threshold where noise can cause high-frequency switching. For more information on Bus-Friendly inputs, please see the AMD application note *Evolution of Bus-Friendly Inputs and I/Os.*

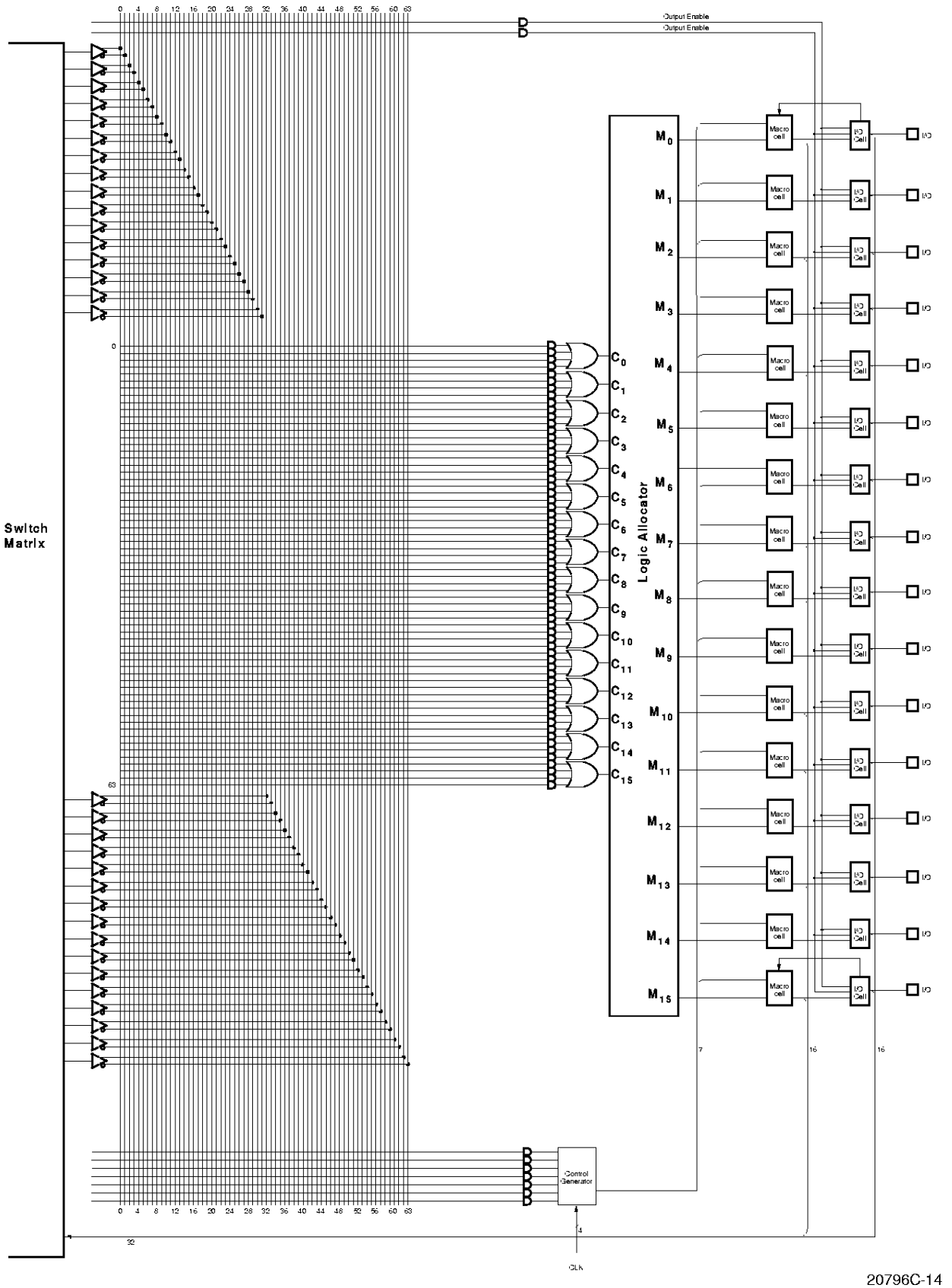


Figure 8. M5-256 PAL Block

ABSOLUTE MAXIMUM RATINGS

MACH 5 COM -7.5, -10, -12, -15

Storage Temperature . . . . . –65°C to +150°C

Supply Voltage
with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . 0.5 V to 5.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (0°C to +70°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Ambient Temperature (T_A)
Operating in Free Air. . . . . .0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

5-V DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Description	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4		3.3	V
V_{OL}	Output LOW Voltage	I_{OL} = +16 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)	–30		–160	mA
I_{CC}	Supply Current	All PAL Blocks Power Level 0 (PL0) V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f = 0 MHz, T_A = 25°C (Note 4)		350		mA
		All PAL Blocks Power Level 1 (PL1) V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f = 0 MHz, T_A = 25°C (Note 4)		220		mA
		All PAL Blocks Power Level 2 (PL2) V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f = 0 MHz, T_A = 25°C (Note 4)		125		mA
		All PAL Blocks Power Level 3 (PL3) V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f = 0 MHz, T_A = 25°C (Note 4)		55		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{ZH}.*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	I/CLK pin	V_{IN} = 2.0 V	5 V, 25°C, 1 MHz	12	pF
$C_{I/O}$	I/O pin	V_{OUT} = 2.0 V	5 V, 25°C, 1 MHz	10	pF

Note:

1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

BASIC (all signals from within PAL block except global control signals)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output or Input, I/O, or Feedback to Output through Transparent Output Latch	2	7.5	2	10	2	12	2	15	ns
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock	4		5		6		8		ns
t_{HS}	Register Data Hold Time Using a Global Clock	0		0		0		0		ns
t_{COS}	Global Clock to Output (Pin Clock)		6		7		8		10	ns
t_{WLS}	Global Clock High Width (Note 3)	3		5		6		6		ns
t_{WHS}	Global Clock Low Width (Note 3)	3		5		6		6		ns
f_{MAX}	External Feedback, PAL Block Level $1/(t_{SS} + t_{COS})$	100		83		71		55		MHz
	Internal Feedback PAL Block Level	125		100		83.3		83.3		MHz
	No Feedback PAL Block Level	166.7		100		83.3		83.3		MHz
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock, PAL Block Level	4		5		6		7		ns
t_{HA}	Output Register Data Hold Time Using a Product Term Clock	4		5		6		7		ns
t_{COA}	Product Term Clock to Output		10		12		15		17	ns
t_{WLA}	Product Term Clock Width LOW	4		5		6		7		ns
t_{WHA}	Product Term Clock Width HIGH	4		5		6		7		ns
f_{MAXA}	External Feedback, PAL Block Level $1/(t_{SA} + t_{COA})$	71		58		47.6		42		MHz
	Internal Feedback, PAL Block Level	88		72		60		52		MHz
	No Feedback, PAL Block Level	125		100		83.3		71.4		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Product Term Gate	4		5		6		7		ns
t_{HL}	Latch Data Hold Time (Using Product Term Gate)	4		5		6		7		ns
t_{GO}	Latch Gate to Output		10		11		12		13	ns
t_{GOL}	Latch Gate to Output through Transparent Latch		17		18		19		20	ns

BASIC (all signals from within PAL block except global control signals) (continued)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{GCO}	Latch Gate to Combinatorial Output		17		18		19		20	ns
t_{IGS}	Latch Gate to Output Latch Setup	10		11		12		13		ns
t_{GW}	Gate Width LOW (for LOW Transparent) or High (for HIGH Transparent)	4		5		6		7		ns
t_{BUF}	Delay Savings for Using Internal Feedback Instead of Pin Feedback (I/Os Only, No Savings for Buried)	0.5	2	0.5	2	0.5	2	0.5	2	ns

ASYNCHRONOUS SET and RESET, OUTPUT ENABLE, CLOCK ENABLE

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RP}	Asynchronous Reset or Preset to Registered or Latched Output		10		12		14		16	ns
t_{PRW}	Asynchronous Reset or Preset Width	4		5		6		7		ns
t_{PRR}	Asynchronous Reset or Preset Recovery Time	7.5		8		9		10		ns
t_{EA}	Input, I/O, or Feedback to Output Enable	2	9.5	2	10	2	12	2	15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		9.5		10		12		15	ns
t_{CES}	Setup Time from Clock Enable to Next Clock Edge	5		6		7		7		ns
t_{CEH}	Hold Time for Clock Enable After Last Enabled Clock Edge	4		5		6		6		ns

REGISTERS and LATCHES (input and output, BLOCK level)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch		9		10		12		15	ns
t_{ICO}	Input Register Clock to Combinatorial Output		13		14		16		18	ns
t_{SIRS}	Input Register Setup Time Using Global Clock	2		3		3		3		ns
t_{SIRA}	Input Register Setup Time Using Product Term Clock	0		0		0		0		ns
t_{HIRS}	Input Register Hold Time Using Global Clock	3		4		4		4		ns
t_{HIRA}	Input Register Hold Time Using Product Term Clock	6		7		7		7		ns
t_{WICW}	Input Register Clock Width Low or High	4		5		6		7		ns
f_{MAXI}	Maximum Input Register Frequency	125		100		83.3		71.4		MHz
t_{RCSS}	Register Using Global Clock to Output Register Using Global Clock Setup Time	7.5		10		12		15		ns
t_{RCSA}	Register Using Global Clock to Output Register Using Product Term Clock Setup Time	12.5		15		17		18		ns
t_{RCAS}	Register Using Product Term Clock to Output Register Using Global Clock Setup Time	12.5		15		17		18		ns
t_{RCAA}	Register Using Product Term Clock to Output Register Using Same Product Term Clock Setup Time	10		10		12		15		ns
t_{SIL}	Input Latch Setup Time	2		3		3		3		ns
t_{HIL}	Input Latch Hold Time	6		7		7		7		ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	9		10		11		12		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		12		14		16		18	ns

INTERCONNECT

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{BLK}	Interconnect delay between blocks. If a signal depends on inputs not in the same block, but in the same segment, this delay must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA},t_{SL}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}.		1.5		2.0		2.0		2.0	ns
t_{SEG}	Interconnect delay between segments. This parameter includes all block interconnect delay. If a signal depends on inputs not in the same segment, this delay must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{SL}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}.		5		6.0		6.0		6.0	ns

POWER, LOGIC, and SLEW

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PL1}	Low-power level 1 delay. If a signal is selected as low power level 1, this parameter must be added to t_{PD}, t_{SS}, t_{SA}, t_{HA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		4		4		4		4	ns
t_{PL2}	Low-power level 2 delay. If a signal is selected as low power level 2, this parameter must be added to t_{PD}, t_{SS}, t_{SA}, t_{HA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		9		9		9		9	ns
t_{PL3}	Low-power level 3 delay. If a signal is selected as low power level 3, this parameter must be added to t_{PD}, t_{SS}, t_{SA}, t_{HA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		17.5		17.5		17.5		17.5	ns
t_{PT}	Product term cluster steering delay. This delay is added for each additional cluster of product terms used beyond the first cluster, to t_{PD}, t_{SS}, t_{SA}, t_{PDL}, t_{PDLL}, t_{SLL}, t_{SL}.		0.3		0.3		0.3		0.3	ns
t_{SLW}	Slow Slew Rate delay. If slow slew rate is selected, this parameter must be added to t_{PD}, t_{COS}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{PDL}, t_{ICO}, t_{PDLL}.		2.5		2.5		2.5		2.5	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *If a signal is used as both a clock and a logic array input, then the maximum input frequency applies (Fmax/2).*

ABSOLUTE MAXIMUM RATINGS

MACH 5 IND -10, -12, -15, -20

Storage Temperature . . . . . –65°C to +150°C

Supply Voltage
with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . 0.5 V to 5.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (–40°C to +85°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Ambient Temperature (T_A)
Operating in Free Air. . . . . –40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

5-V DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Description	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4		3.3	V
V_{OL}	Output LOW Voltage	I_{OL} = +16 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)	–30		–160	mA
I_{CC}	Supply Current	All PAL Blocks Power Level 0 (PL0) V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f = 0 MHz, T_A = 25°C (Note 4)		350		mA
		All PAL Blocks Power Level 1 (PL1) V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f = 0 MHz, T_A = 25°C (Note 4)		220		mA
		All PAL Blocks Power Level 2 (PL2) V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f = 0 MHz, T_A = 25°C (Note 4)		125		mA
		All PAL Blocks Power Level 3 (PL3) V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f = 0 MHz, T_A = 25°C (Note 4)		55		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH}.*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	I/CLK pin	V_{IN} = 2.0 V	5 V, 25°C, 1 MHz	12	pF
$C_{I/O}$	I/O pin	V_{OUT} = 2.0 V	5 V, 25°C, 1 MHz	10	pF

Note:

1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

BASIC (all signals from within PAL block except global control signals)

Parameter Symbol	Parameter Description	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output or Input, I/O, or Feedback to Output through Transparent Output Latch	2	10	2	12	2	15	2	20	ns
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock	5		6		8		10		ns
t_{HS}	Register Data Hold Time Using a Global Clock	0		0		0		0		ns
t_{COS}	Global Clock to Output (Pin Clock)		7		8		10		12	ns
t_{WLS}	Global Clock High Width (Note 3)	5		6		6		7		ns
t_{WHS}	Global Clock Low Width (Note 3)	5		6		6		7		ns
f_{MAX}	External Feedback, PAL Block Level $1/(t_{SS} + t_{COS})$	83		71		55		45.5		MHz
	Internal Feedback PAL Block Level	100		83.3		83.3		71.4		MHz
	No Feedback PAL Block Level	100		83.3		83.3		71.4		MHz
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock, PAL Block Level	5		6		7		8		ns
t_{HA}	Output Register Data Hold Time Using a Product Term Clock	5		6		7		8		ns
t_{COA}	Product Term Clock to Output		12		15		17		20	ns
t_{WLA}	Product Term Clock Width LOW	5		6		7		8		ns
t_{WHA}	Product Term Clock Width HIGH	5		6		7		8		ns
f_{MAXA}	External Feedback, PAL Block Level $1/(t_{SA} + t_{COA})$	83		67		59		50		MHz
	Internal Feedback, PAL Block Level	95		83.3		71.4		62.5		MHz
	No Feedback, PAL Block Level	100		83.3		71.4		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Product Term Gate	5		6		7		8		ns
t_{HL}	Latch Data Hold Time (Using Product Term Gate)	5		6		7		8		ns
t_{GO}	Latch Gate to Output		11		12		13		14	ns
t_{GOL}	Latch (Input or Output) Gate to Output through Transparent Latch		18		19		20		21	ns

BASIC (all signals from within PAL block except global control signals) (continued)

Parameter Symbol	Parameter Description	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{GCO}	Latch Gate to Combinatorial Output		18		19		20		21	ns
t_{IGS}	Latch Gate to Output Latch Setup	11		12		13		14		ns
t_{GW}	Gate Width LOW (for LOW Transparent) or High (for HIGH Transparent)	5		6		7		8		ns
t_{BUF}	Delay Savings for Using Internal Feedback Instead of Pin Feedback (I/Os Only, No Savings for Buried)	0.5	2	0.5	2	0.5	2	0.5	2	ns

ASYNCHRONOUS SET and RESET, OUTPUT ENABLE, CLOCK ENABLE

Parameter Symbol	Parameter Description	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RP}	Asynchronous Reset or Preset to Registered or Latched Output		12		14		16		18	ns
t_{PRW}	Asynchronous Reset or Preset Width	5		6		7		8		ns
t_{PRR}	Asynchronous Reset or Preset Recovery Time	8		9		10		11		ns
t_{EA}	Input, I/O, or Feedback to Output Enable	2	10	2	12	2	15	2	20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		10		12		15		20	ns
t_{CES}	Setup Time from Clock Enable to Next Clock Edge	6		7		7		8		ns
t_{CEH}	Hold Time for Clock Enable After Last Enabled Clock Edge	5		6		6		7		ns

REGISTERS and LATCHES (input and output, BLOCK level)

Parameter Symbol	Parameter Description	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch		10		12		15		20	ns
t_{ICO}	Input Register Clock to Combinatorial Output		14		16		18		20	ns
t_{SIRS}	Input Register Setup Time Using Global Clock	3		3		3		3		ns
t_{SIRA}	Input Register Setup Time Using Product Term Clock	0		0		0		0		ns
t_{HIRS}	Input Register Hold Time Using Global Clock	4		4		4		4		ns
t_{HIRA}	Input Register Hold Time Using Product Term Clock	7		7		7		7		ns
t_{WICW}	Input Register Clock Width Low or High	5		6		7		8		ns
f_{MAXI}	Maximum Input Register Frequency	100		83.3		71.4		62.5		MHz
t_{RCSS}	Register Using Global Clock to Output Register Using Global Clock Setup Time	10		12		15		20		ns
t_{RCSA}	Register Using Global Clock to Output Register Using Product Term Clock Setup Time	15		17		18		20		ns
t_{RCAS}	Register Using Product Term Clock to Output Register Using Global Clock Setup Time	15		17		18		20		ns
t_{RCAA}	Register Using Product Term Clock to Output Register Using Same Product Term Clock Setup Time	10		12		15		20		ns
t_{SIL}	Input Latch Setup Time	3		3		3		3		ns
t_{HIL}	Input Latch Hold Time	7		7		7		7		ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	10		11		12		13		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		14		16		18		20	ns

INTERCONNECT

Parameter Symbol	Parameter Description	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{BLK}	Interconnect delay between blocks. If a signal depends on inputs not in the same block, but in the same segment, this delay must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{SL}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}.		2.0		2.0		2.0		2.0	ns
t_{SEG}	Interconnect delay between segments. This parameter includes all block interconnect delay. If a signal depends on inputs not in the same segment, this delay must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{SL}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}.		6		6		6		6	ns

POWER, LOGIC, and SLEW

Parameter Symbol	Parameter Description	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PL1}	Low-power level 1 delay. If a signal is selected as low power level 1, this parameter must be added to t_{PD}, t_{SS}, t_{SA}, t_{HA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		4		4		4		4	ns
t_{PL2}	Low-power level 2 delay. If a signal is selected as low power level 2, this parameter must be added to t_{PD}, t_{SS}, t_{SA}, t_{HA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		9		9		9		9	ns
t_{PL3}	Low-power level 3 delay. If a signal is selected as low power level 3, this parameter must be added to t_{PD}, t_{SS}, t_{SA}, t_{HA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		17.5		17.5		17.5		17.5	ns
t_{PT}	Product term cluster steering delay. This delay is added for each additional cluster of product terms used beyond the first cluster, to t_{PD}, t_{SS}, t_{SA}, t_{PDL}, t_{PDLL}, t_{SLL}, t_{SL}.		0.3		0.3		0.3		0.3	ns
t_{SLW}	Slow Slew Rate delay. If slow slew rate is selected, this parameter must be added to t_{PD}, t_{COS}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{PDL}, t_{ICO}, t_{PDLL}.		2.5		2.5		2.5		2.5	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *If a signal is used as both a clock and a logic array input, then the maximum input frequency applies (Fmax/2).*

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ					Unit
			100-Pin PQFP	100-Pin TQFP	144-Pin PQFP	160-Pin PQFP	208-Pin PQFP	
θ_{jc}	Thermal impedance, junction to case		TBD	TBD	TBD	TBD	TBD	°C/W
θ_{ja}	Thermal impedance, junction to ambient		30	30	30	30	18	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	TBD	TBD	TBD	TBD	TBD	°C/W
		400 lfpm air	TBD	TBD	TBD	TBD	TBD	°C/W
		600 lfpm air	TBD	TBD	TBD	TBD	TBD	°C/W
		800 lfpm air	TBD	TBD	TBD	TBD	TBD	°C/W

Plastic θ_{jc} Considerations

The data listed for plastic θ_{jc} are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θ_{jc} measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θ_{jc} tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment. TQFP thermal measurements are taken with components on a 6-layer printed circuit board.

DEVELOPMENT SYSTEMS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD Catalog.

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	MACHXL Software
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	AMD/MicroSim Software
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	AMD-ABEL Software Data I/O MACH Fitters
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	Contact Manufacturer
Cadence Design Systems 555 River Oaks Pkwy San Jose, CA 95134 (408) 943-1234	PLD Designer Verilog, LeapFrog, RapidSim Simulators Ver. 9602
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	ABEL™ Synario™ Software
ISDATA GmbH Daimlerstr. 51 D-76185 Karlsruhe, Germany (721) 75 10 87	LOG/iC2 LOG/iC Classic
Logic Modeling 19500 NW Gibbs Dr. P.O. Box 310 Beaverton, OR 97075 (503) 690-6900	SmartModel® Library
Mentor Graphics Corp. 8005 S.W. Boeckman Rd. Wilsonville, OR 97070-7777 (800) 547-3000 or (503) 685-7000	PLDSynthesis™ II QuickSim Simulator
MicroSim Corp. 20 Fairbanks Irvine, CA 92718 (714) 770-3022	MicroSim PLSyn® PSPICE® A/D PLogic
MINC Incorporated 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (800) 755-FPGA or (719) 590-1155	PLDesigner-XL™ Software
SUSIE-CAD 10000 Nevada Highway, Suite 201 Boulder City, NV 89005 (702) 293-2271	SUSIE™ Simulator

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS
Synopsys 700 E. Middlefield Rd. Mountain View, CA 94040	FPGA or Design Compiler (Requires MINC PLDesigner-XL™)
Teradyne EDA 321 Harrison Ave. Boston, MA 02118 (800) 777-2432 or (617) 422-2793	MultiSIM Interactive Simulator LASAR
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 442-4660 or (508) 480-0881	ViewPLD ViewSim Simulator
MANUFACTURER	**TEST GENERATION SYSTEM**
Acugen Software, Inc. 427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 891-1995	ATGEN™ Test Generation Software
iNt GmbH Busenstrasse 6 D-8033 Martinsried, Munich, Germany (87) 857-6667	PLDCheck 90

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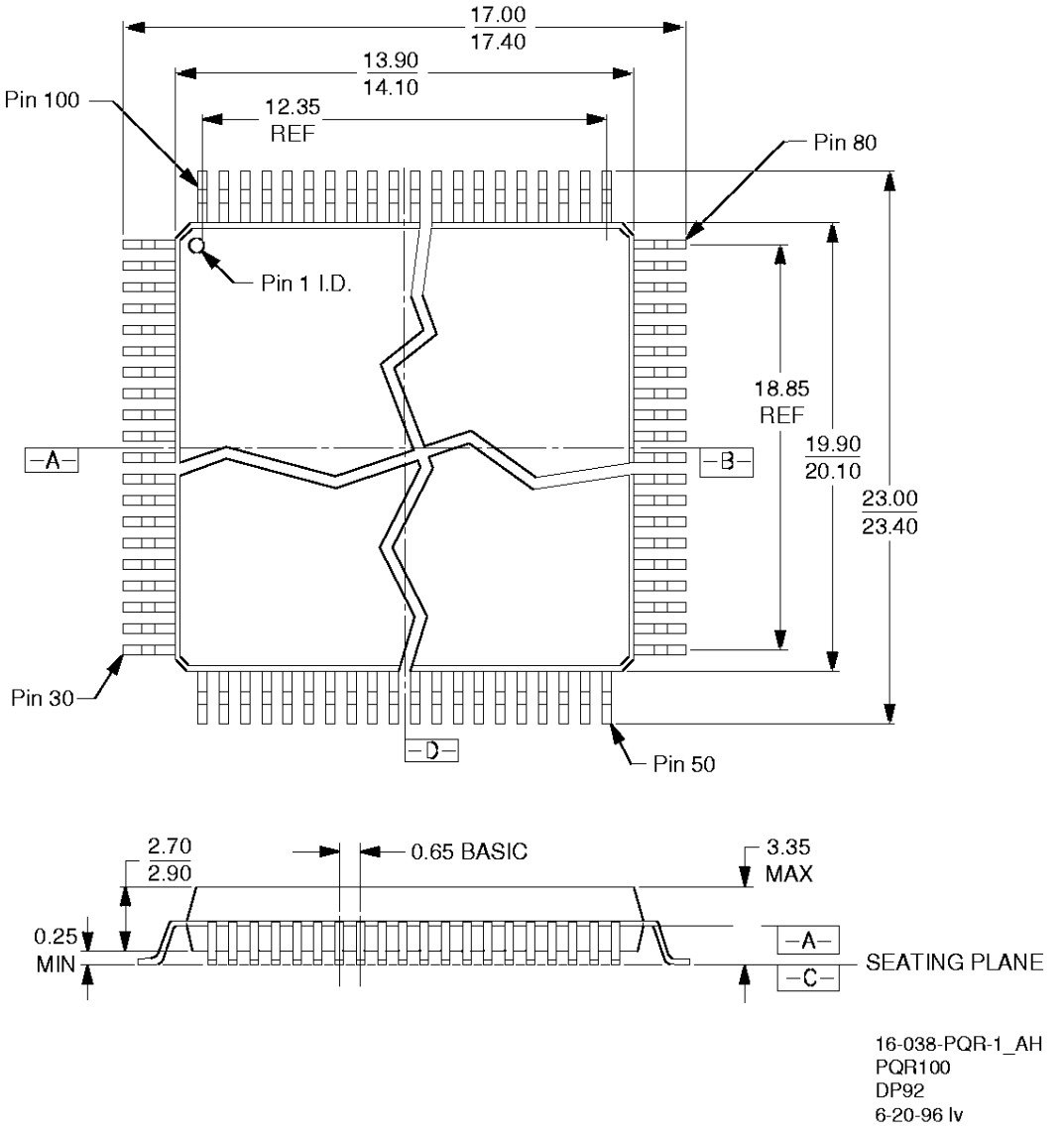
PHYSICAL DIMENSIONS

PQR100

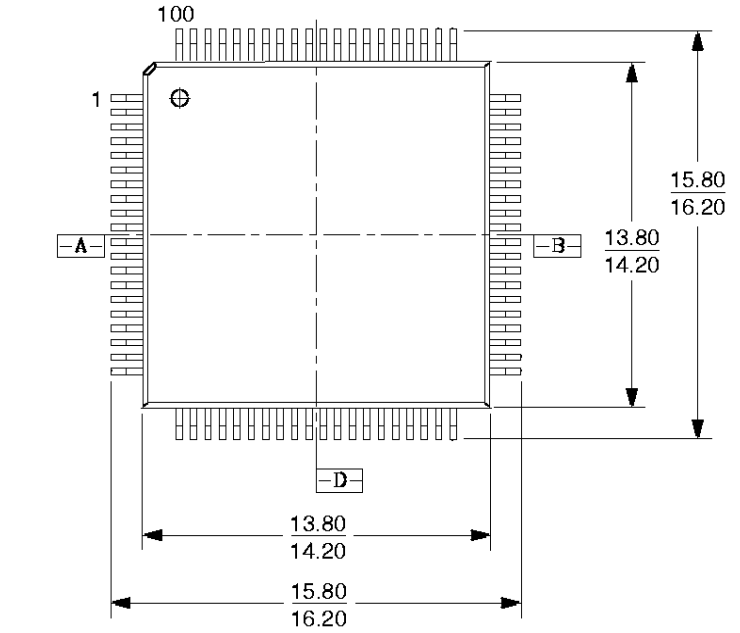
100-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)

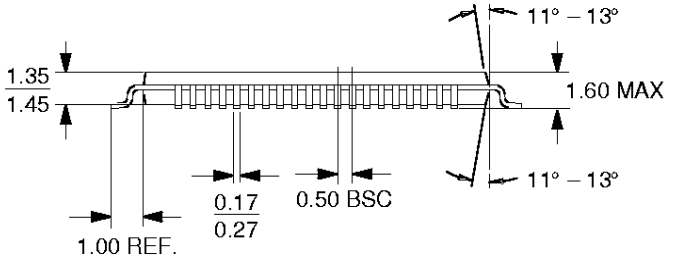


16-038-PQR-1_AH
PQR100
DP92
6-20-96 lv

PQT100

100-Pin Thin Quad Flat Pack (measured in millimeters)

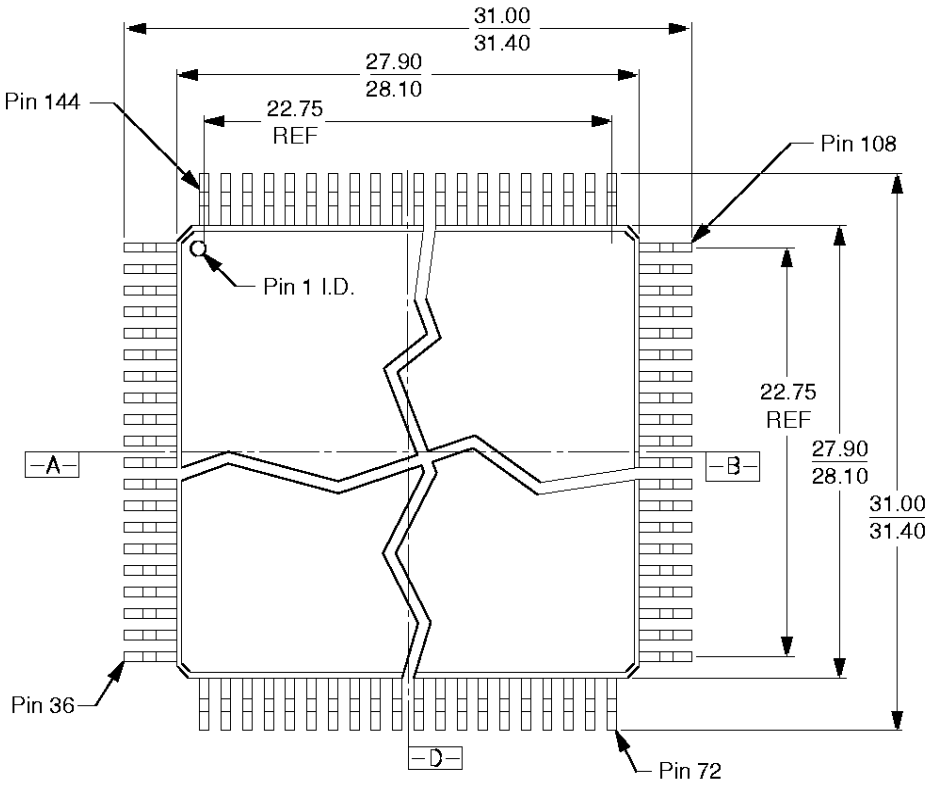


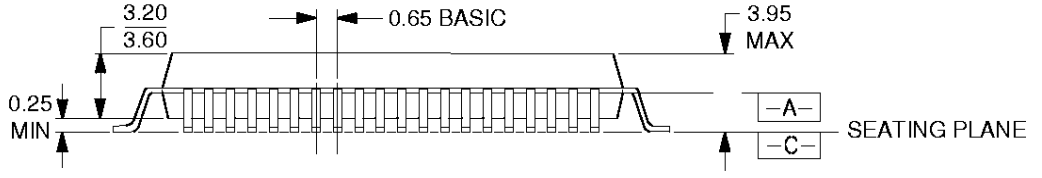


16-038-PQT-2_AI
PQT100
1.10.96 lv

PQR144

144-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)

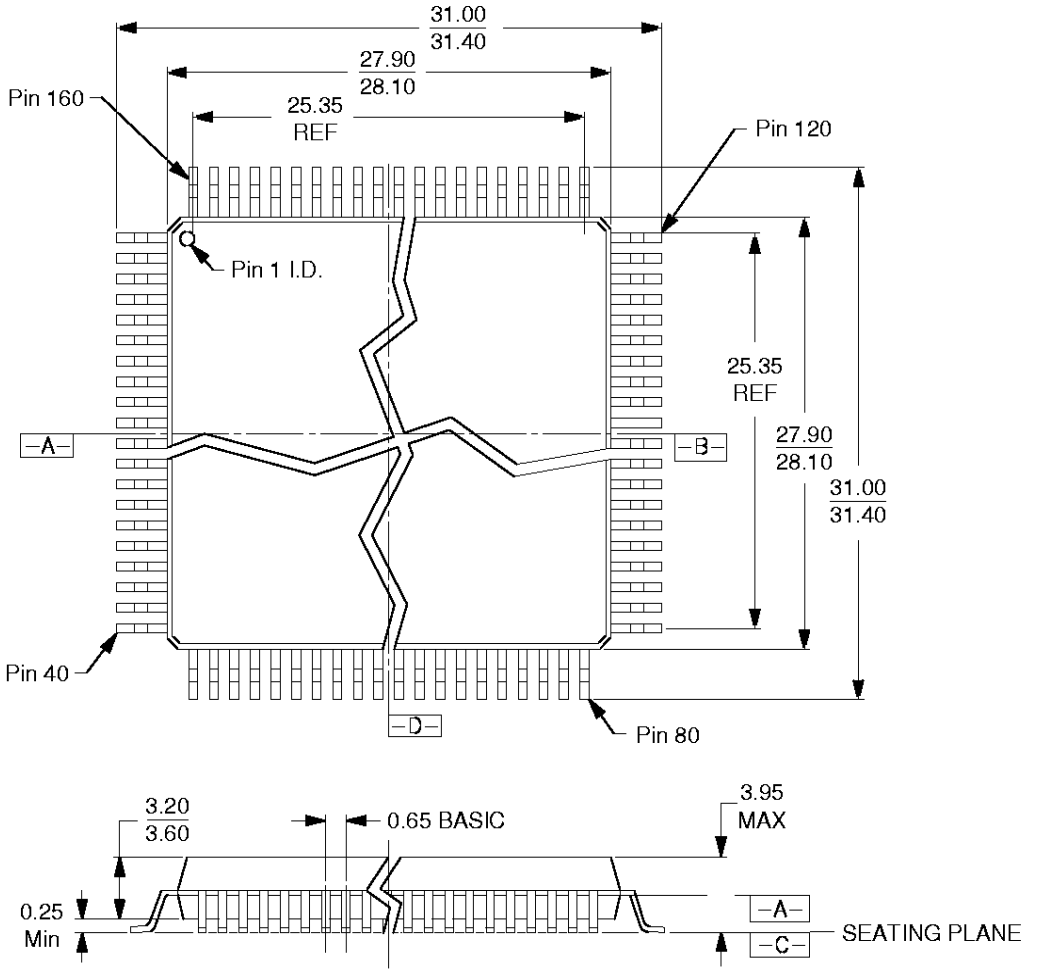




16-038-PQR-1_AH
PQR144
DP92
9-3-96 lv

PQR160

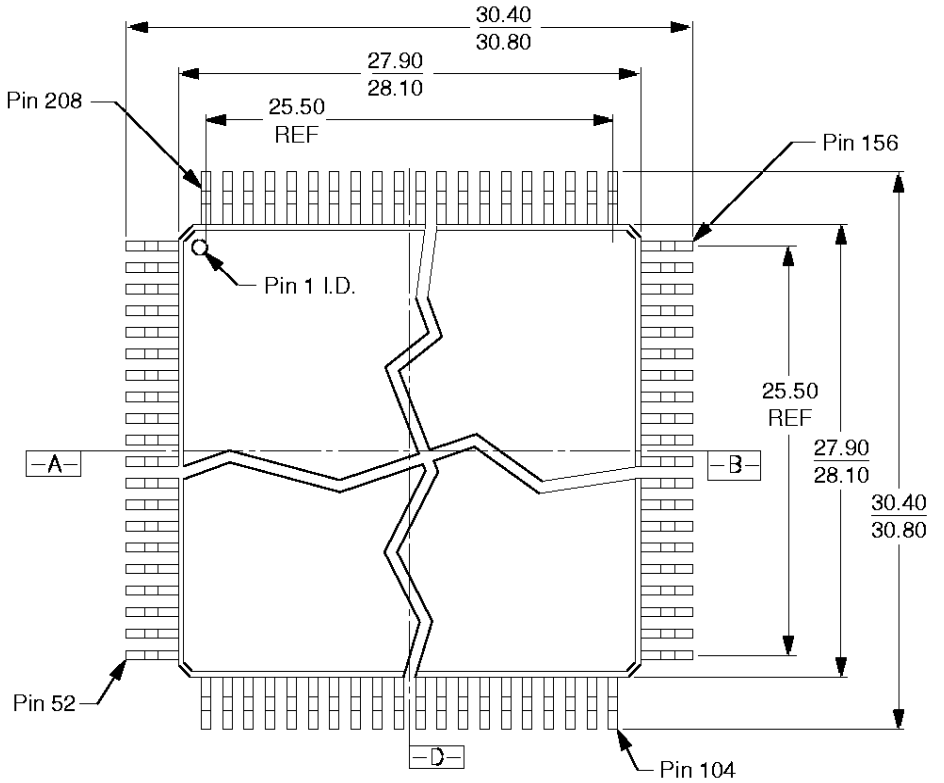
160-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)

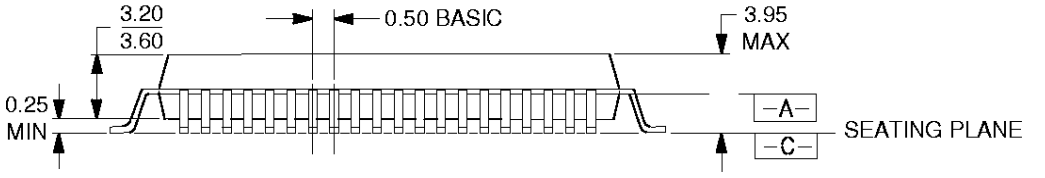


16-038-PQR-1
PQR160
12-22-95 lv

PQR208

208-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)





16-038-PQR-1_AH
PQR208
DP92
11-5-96 lv