NEC

MOS INTEGRATED CIRCUIT

μPD168117A

7-CHANNEL H-BRIDGE DRIVER WITH A MICRO STEP FUNCTION SUPPORTING PULSE INPUT

DESCRIPTION

The μPD168117A is a 7-channel H-bridge driver with a micro step function supporting pulse input that consists of a CMOS control circuit and a MOS output stage. It can reduce the current consumption and the voltage loss at the output stage compared with a conventional driver using bipolar transistors, thanks to employment of a MOS process. Moreover, at the μPD168117A, micro step control of 128 divisions can perform stepping motor drive by the pulse input, and motor can be driven by low noise and low vibration.

The package is a 64-pin FLGA that helps reduce the mounting area and height.

The μPD168117A can be used to drive two stepping motors, or two DC motors and one coil.

FEATURES

- Seven H-bridge circuits employing power MOS FET
- Low-voltage driving
  V_{DD} = 2.7 to 3.6 V
  V_M = 2.7 to 5.5 V
- Output on-state resistance: 1.0 Ω TYP., 1.5 Ω MAX. (sum of top and bottom stage, ch1 to ch4, and ch7)
  1.5 Ω TYP., 2.0 Ω MAX. (sum of top and bottom stage, ch5 and ch6)
- PWM output (ch1 to ch6), linear output (ch7)
- Output current
  <ch1 to ch6>
  DC current: 0.4 A/ch (when each channel is used independently)
  Peak current: 0.7 A/ch (when each channel is used independently)
  <ch7>
  DC current: 0.5 A/ch (when used independently)
  Peak current: 0.7 A/ch (when used independently)
- Input logic frequency: 150 kHz supported
- Under-voltage lockout circuit
  Shuts down the internal circuit at V_{DD} = 1.7 V TYP.
- Overheat protection circuit
  Operates at 150°C or more and shuts down internal circuitry.
- Mounted on 64-pin FLGA (□6 mm, 0.65 mm pitch)

ORDERING INFORMATION

Part Number	Package	Packing Type
μPD168117AFC-BA2-E1-A [Note]	64-pin plastic FLGA (6 x 6)	Embossed-type taping

Note Pb-free (This product does not contain Pb in external electrode and other parts.)

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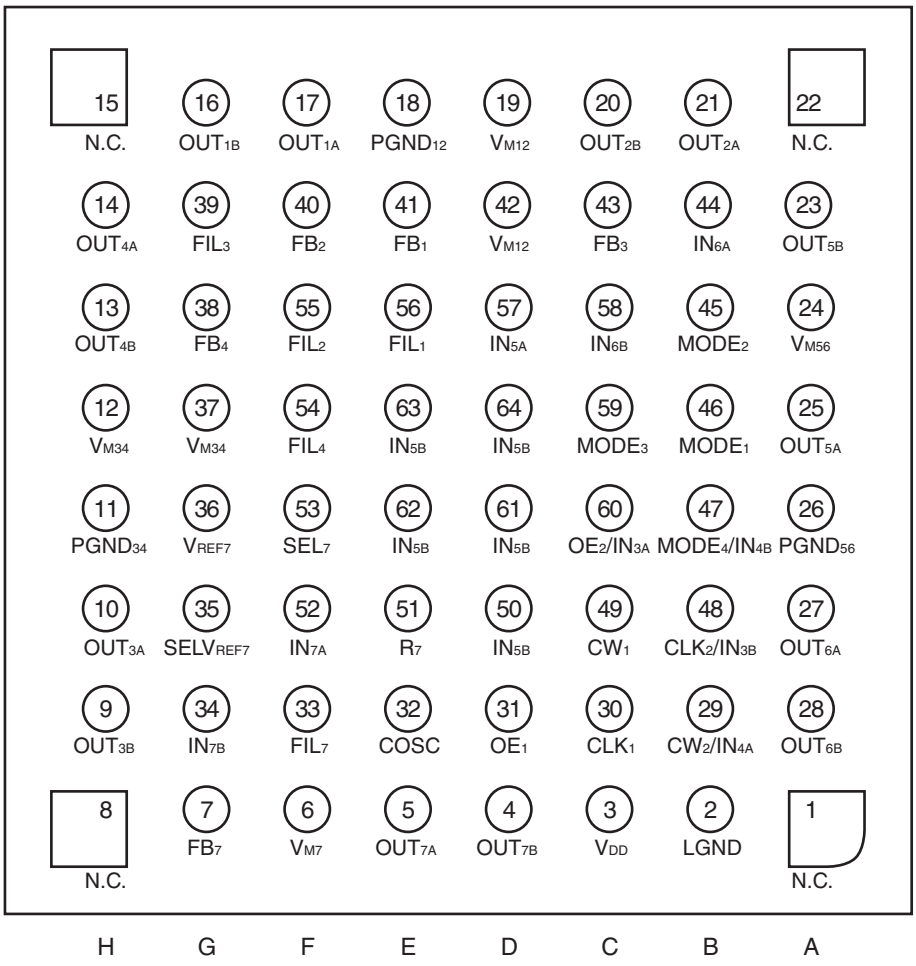
1. PIN CONFIGURATION (Bottom View)

Package: 64-pin plastic FLGA (6 x 6)



Cautions Be sure to connect all of the pins which have more than one.

2. PIN FUNCTIONS

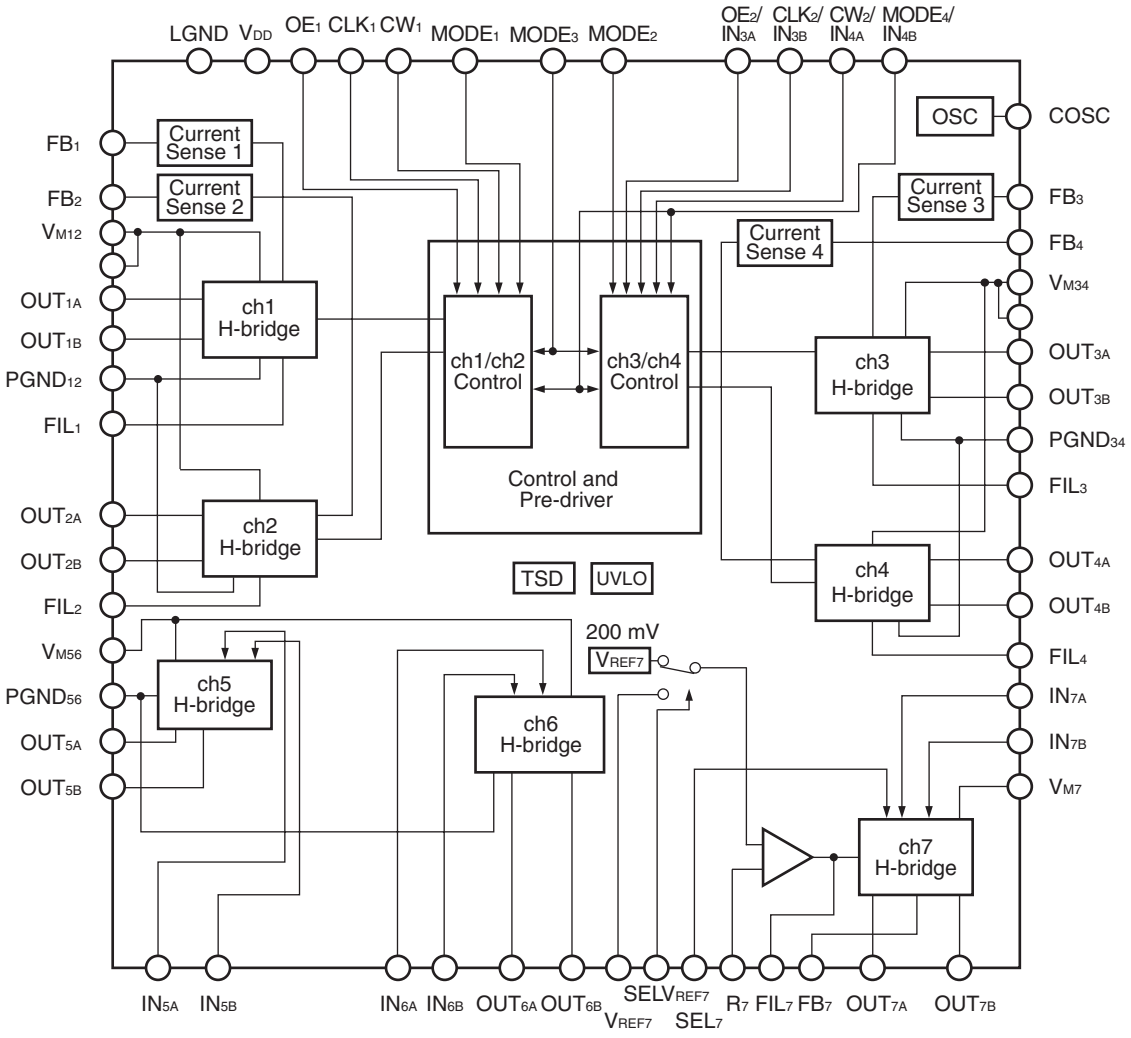
(1/2)

Pin No.		Pin Name	Function
1	A1	N.C.	–
2	B1	LGND	Logic block GND pin
3	C1	V_{DD}	Logic block power supply pin
4	D1	OUT_{7B}	H-bridge 7 output pin B
5	E1	OUT_{7A}	H-bridge 7 output pin A
6	F1	V_{M7}	H-bridge 7 power supply pin
7	G1	FB_7	Current detection resistor connection pin 7
8	H1	N.C.	–
9	H2	OUT_{3B}	H-bridge 3 output pin B
10	H3	OUT_{3A}	H-bridge 3 output pin A
11	H4	$PGND_{34}$	H-bridge 3, H-bridge 4 GND pin
12	H5	V_{M34}	H-bridge 3, H-bridge 4 power supply pin
13	H6	OUT_{4B}	H-bridge 4 output pin B
14	H7	OUT_{4A}	H-bridge 4 output pin A
15	H8	N.C.	–
16	G8	OUT_{1B}	H-bridge 1 output pin B
17	F8	OUT_{1A}	H-bridge 1 output pin A
18	E8	$PGND_{12}$	H-bridge 1, H-bridge 2 GND pin
19	D8	V_{M12}	H-bridge 1, H-bridge 2 power supply pin
20	C8	OUT_{2B}	H-bridge 2 output pin B
21	B8	OUT_{2A}	H-bridge 2 output pin A
22	A8	N.C.	–
23	A7	OUT_{5B}	H-bridge 5 output pin B
24	A6	V_{M56}	H-bridge 5, H-bridge 6 power supply pin
25	A5	OUT_{5A}	H-bridge 5 output pin A
26	A4	$PGND_{56}$	H-bridge 5, H-bridge 6 GND pin
27	A3	OUT_{6A}	H-bridge 6 output pin A
28	A2	OUT_{6B}	H-bridge 6 output pin B
29	B2	CW_2/IN_{4A}	H-bridge 3, H-bridge 4 driving direction input pin/H-bridge 4 input pin A
30	C2	CLK_1	H-bridge 1, H-bridge 2 CLK input pin
31	D2	OE_1	H-bridge 1, H-bridge 2 output enable pin
32	E2	COSC	Chopping frequency setting capacitor connection pin
33	F2	FIL_7	Amplifier operation stabilizing filter connection pin
34	G2	IN_{7B}	H-bridge 7 input pin B
35	G3	$SELV_{REF7}$	ch7 reference voltage setup selection pin
36	G4	V_{REF7}	ch7 reference voltage external input pin
37	G5	V_{M34}	H-bridge 3, H-bridge 4 power supply pin
38	G6	FB_4	Current detection resistor connection pin 4

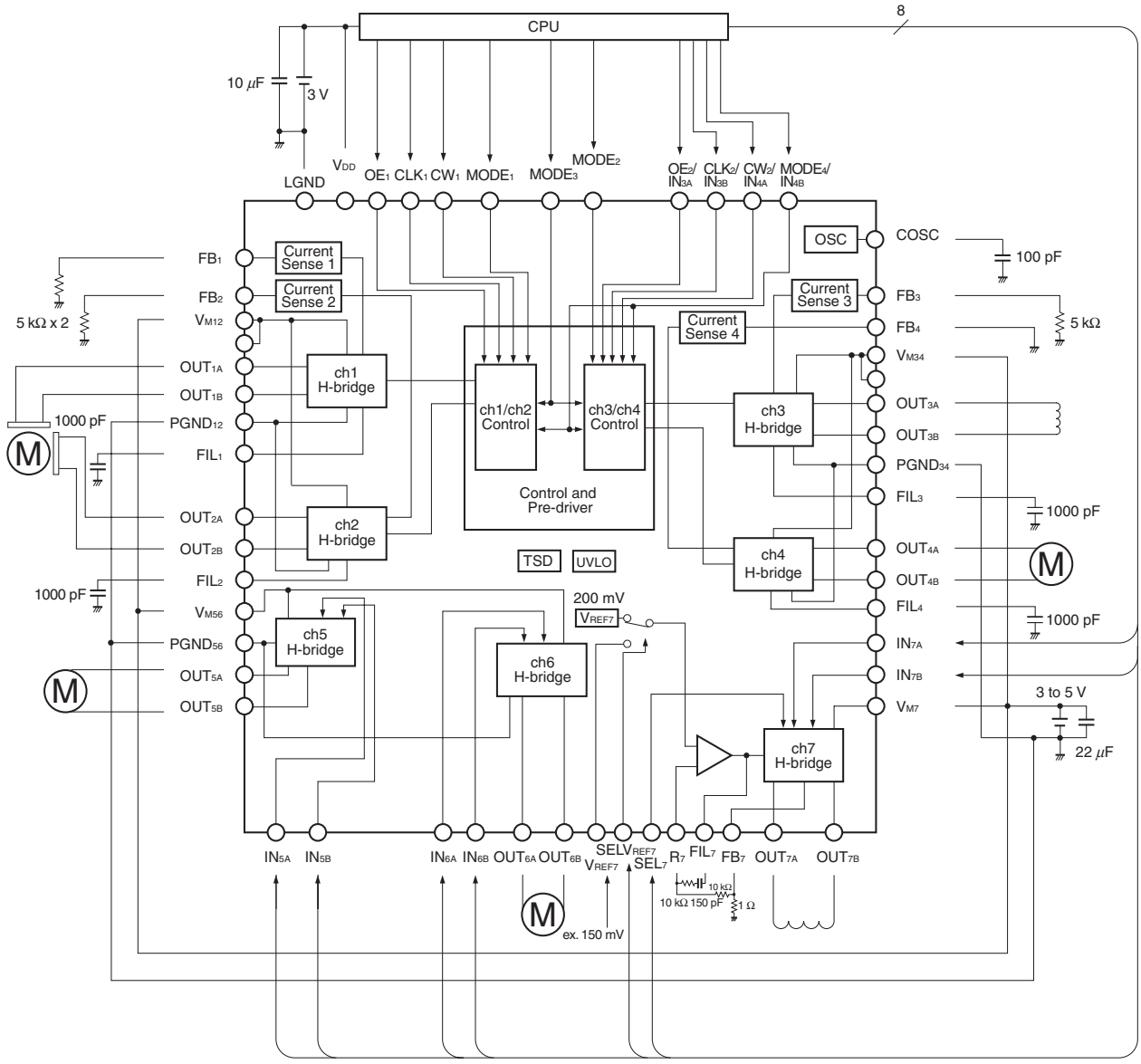
(2/2)

Pin No.		Pin Name	Function
39	G7	FIL_3	Filter capacitor connection pin 3
40	F7	FB_2	Current detection resistor connection pin 2
41	E7	FB_1	Current detection resistor connection pin 1
42	D7	V_{M12}	H-bridge 1, H-bridge 2 power supply pin
43	C7	FB_3	Current detection resistor connection pin 3
44	B7	IN_{6A}	H-bridge 6 input pin A
45	B6	$MODE_2$	Mode selection pin 2
46	B5	$MODE_1$	Mode selection pin 1
47	B4	$MODE_4/IN_{4B}$	Mode selection pin 4/H-bridge 4 input pin B
48	B3	CLK_2/IN_{3B}	H-bridge 3, H-bridge 4 CLK input pin/H-bridge 3 input pin B
49	C3	CW_1	H-bridge 1, H-bridge 2 driving direction input pin
50	D3	IN_{5B}	H-bridge 5 input pin B
51	E3	R_7	Amplifier operation stabilizing resistor connection pin
52	F3	IN_{7A}	H-bridge 7 input pin A
53	F4	SEL_7	ch7 excitation mode selection pin
54	F5	FIL_4	Filter capacitor connection pin 4
55	F6	FIL_2	Filter capacitor connection pin 2
56	E6	FIL_1	Filter capacitor connection pin 1
57	D6	IN_{5A}	H-bridge 5 input pin A
58	C6	IN_{6B}	H-bridge 6 input pin B
59	C5	$MODE_3$	Mode selection pin 3
60	C4	OE_2/IN_{3A}	H-bridge 3, H-bridge 4 output enable pin/H-bridge 3 input pin A
61	D4	IN_{5B}	H-bridge 5 input pin B
62	E4	IN_{5B}	H-bridge 5 input pin B
63	E5	IN_{5B}	H-bridge 5 input pin B
64	D5	IN_{5B}	H-bridge 5 input pin B

3. BLOCK DIAGRAM



4. STANDARD CONNECTION EXAMPLE



Cautions 1. Be sure to connect all of the pins which have more than one.

2. The constants shown in the above diagram are provided as examples only. Perform design based on thorough evaluation with the actual machine.

5. FUNCTION OPERATION TABLE

5.1 Power Save Function

This IC can be placed in the power-save mode by making $MODE_1$, $MODE_2$, $MODE_3$, and $MODE_4$ high level.

This function allows holding of the excitation position when the stepping motor mode is selected and the operation to be started from where the excitation position is held when the power-save mode is cleared. In the power-save mode, the current consumption is reduced to 20 μA TYP. because the internal circuits other than UVLO are stopped.

The operation modes of ch1 to ch4 can be set by a combination of $MODE_1$ to $MODE_4$. For the combination of the MODE pins, refer to **Table 5–1. MODE Pin Truth Table**.

Table 5–1. Mode Pin Truth Table

$MODE_1$	$MODE_2$	$MODE_3$	$MODE_4$ ($/IN_{4B}$)	Operation Mode	
				ch1, ch2	ch3, ch4
L	L	L	IN_{4B} input	2-phase excitation	General-purpose driving (current limiting)
L	L	H		1-2 phase excitation	
L	H	L		Micro step	
L	H	H	L	2-phase excitation	2-phase excitation
L	H	H	H	1-2 phase excitation	1-2 phase excitation
H	L	L	L	2-phase excitation (current limiting)	2-phase excitation (current limiting)
H	L	L	H	1-2 phase excitation (current limiting)	1-2 phase excitation (current limiting)
H	L	H	L	2-phase excitation	Micro step
H	L	H	H	1-2 phase excitation	Micro step
H	H	L	L	Micro step	2-phase excitation
H	H	L	H	Micro step	1-2 phase excitation
H	H	H	L	Micro step	Micro step
H	H	H	H	Power save mode	

Remark H: High level, L: Low level

5.2 ch1, ch2 (Dedicated to Stepping Motor)

CLK_1	CW_1	OE_1	Operation Mode
↑	L	H	Pulse progress, CW mode
↓	L	H	Pulse progress, CW mode
↑	H	H	Pulse progress, CCW mode
↓	H	H	Pulse progress, CCW mode
x	x	L	Output Hi-Z (The internal follows the above-mentioned mode of operation)

Remark x: High level or low level, Hi-Z: High impedance

5.3 ch3, ch4 (Selecting Stepping Motor, DC Motor and Coil Driving)

<Stepping motor drive mode>

CLK_2	CW_2	OE_2	Operation Mode
↑	L	H	Pulse progress, CW mode
↓	L	H	Pulse progress, CW mode
↑	H	H	Pulse progress, CCW mode
↓	H	H	Pulse progress, CCW mode
x	x	L	Output Hi-Z (The internal follows the above-mentioned mode of operation)

<General-purpose drive mode>

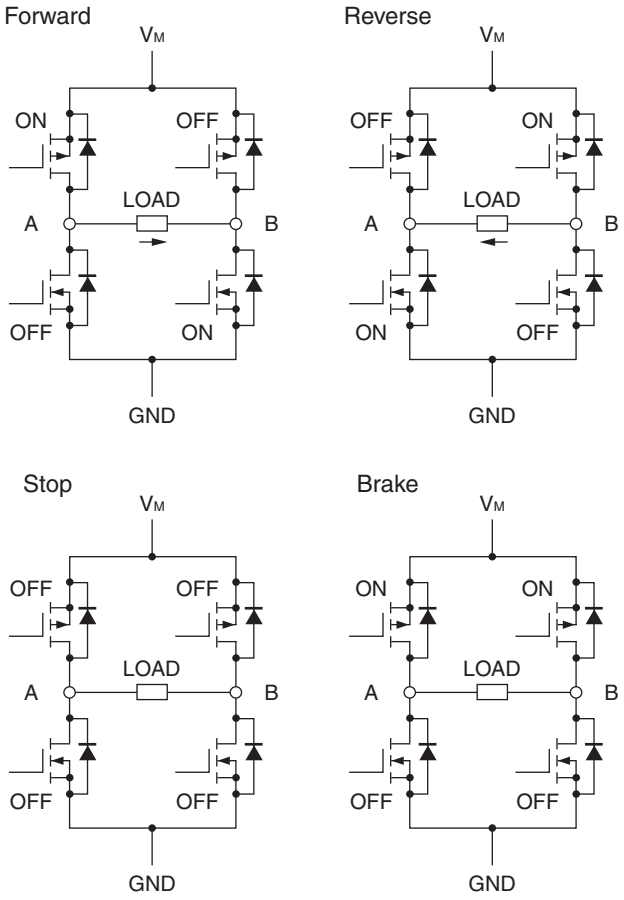
IN_{3A}/IN_{4A}	IN_{3B}/IN_{4B}	OUT_{3A}/OUT_{4A}	OUT_{3B}/OUT_{4B}	Operation Mode
L	L	Z	Z	Stop
L	H	L	H Note	Reverse
H	L	H Note	L	Forward
H	H	H	H	Brake

Note When the μPD168117A is used for constant-current driving (when a sense resistor is connected to the FB pin), chopping driving is performed.

Remark Z: Output high impedance

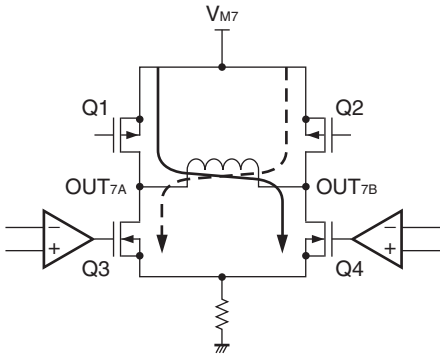
5.4 ch5, ch6

IN_{5A}/IN_{6A}	IN_{5B}/IN_{6B}	OUT_{5A}/OUT_{6A}	OUT_{5B}/OUT_{6B}	Operation Mode
L	L	Z	Z	Stop
L	H	L	H	Reverse
H	L	H	L	Forward
H	H	H	H	Brake



5.5 ch7

IN_{7A}	IN_{7B}	OUT_{7A}	OUT_{7B}	H-bridge Output State			
				Q1	Q2	Q3	Q4
L	L	Z	Z	OFF	OFF	OFF	OFF
L	H	L (linear)	H	OFF	ON	ON (linear)	OFF
H	L	H	L (linear)	ON	OFF	OFF	ON (linear)
H	H	H	H	ON	ON	OFF	OFF



5.6 SEL_7 Pin

The current that flows into ch7 can be changed by setting the SEL_7 pin.

SEL_7	Operation Mode
L	Weak excitation mode (Current 2/3 of the normal setting flows.)
H	Normal operation mode (Comparison operation with reference voltage)

5.7 Reference Voltage Settings

The external setting mode, in which the reference voltage is input to V_{REF7} externally, and the internal setting mode, in which the internal reference voltage is used, can be switched using the $SELV_{REF7}$ pin.

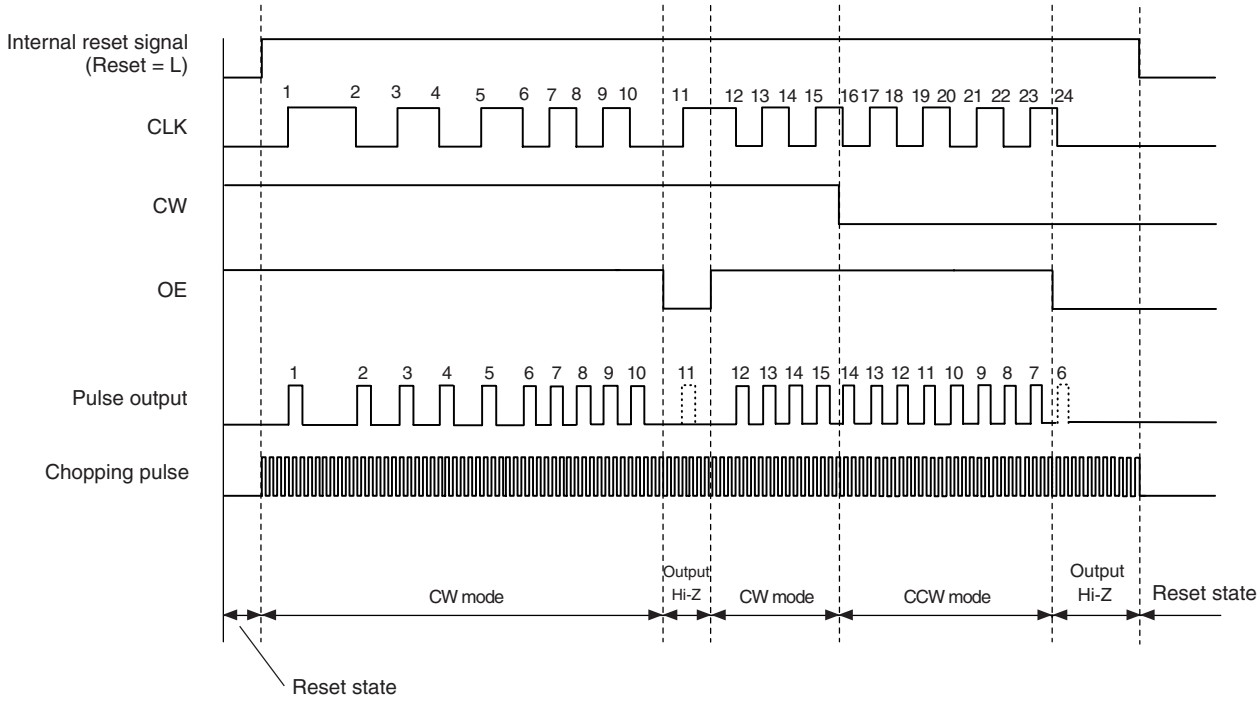
When using the external setting mode, the voltage which will become reference voltage must be applied to the V_{REF7} pin.

The functions for the SEL_7 pin will be enabled, regardless of the external/internal setting mode. The voltage (when external setting mode is set), and the 200 mV (when the internal setting mode is set) that are applied to the V_{REF7} pin are equivalent to normal operation mode (SEL_7 = H).

$SELV_{REF7}$	Operation Mode
L	External setting mode (Voltage must be applied to V_{REF7})
H	Internal setting mode (200 mV setting)

6. COMMAND INPUT TIMING CHART

Figure 6–1. In The Micro Step Mode



Remark The motor excitation output is equivalent to the pulse output. The excitation position of the motor is changed by the rising edge timing of the pulse output (equals the rising or falling edges of CLK).

7. FUNCTIONAL DEPLOYMENT

7.1 Reset Function

This whole IC can be changed into a reset state by setting all of $MODE_1$ to $MODE_4$ to H, and all of IN_{5A}, IN_{5B}, IN_{6A}, IN_{6B}, IN_{7A}, and IN_{7B} to L. In the state of reset, an output will be in Hi-Z state, and since it stops operation of an internal circuit, it can make self-consumption current below 1 μA.

Be sure to perform a reset operation.

In the reset operation, the internal circuitry is stopped whenever possible, so that the self current consumption can be reduced. When the external input signal is stopped, the current consumption can be lowered to 1 μA MAX.

Immediately after release of reset, excitation is started from the position where the current of ch1 is 100% and the current of ch2 is 0%, in the micro step drive mode and 1-2 phase excitation drive mode. In the 2-phase excitation drive mode, excitation is started from the position where the currents of ch1 and ch2 are 100%.

7.2 2-phase Excitation Drive Mode and 1-2 Phase Excitation Drive Mode

In the 2-phase excitation drive mode, current of ±100% is allowed to flow into ch1 and ch2 simultaneously. In the 1-2 phase excitation drive mode, the motor can be driven at a higher torque by allowing a current to flow so that the synthesized torque of ch1 and ch2 is the same as the torque at phase 1 position. The 2-phase excitation, 1-2 phase excitation, and micro step driving modes are selected by the $MODE_1$ to $MODE_4$ pins.

Note that 100% (= saturation drive mode) and a mode in which the current set by the sense resistor is used can be selected by the MODE pin. Current control is performed by chopping drive.

7.3 Micro Step Drive Mode of Stepping Motor

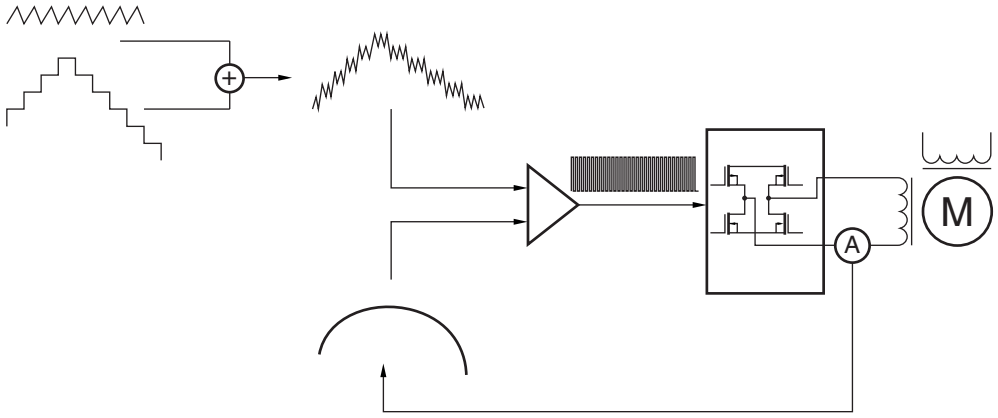
The current flowing into the H-bridge is constant by using a vector value so that one period can be stopped in 1/128 steps. This function is provided to realize high-accuracy positioning control of a stepping motor.

To realize this micro step driving, the following functions are internally realized by the driver.

- Detection of current flowing into each channel by sense resistor as voltage value
- Synthesizing half the dummy sine waveform generated by the internal D/A with PWM oscillation waveform for chopping operation
- Driver stage performing PWM drive based on result of comparing detected voltage and synthesized waveform

Because the internal dummy sine wave consists of 128 steps per period, it can be used to drive a stepping motor using 128 divisions. The micro step drive mode, 2-phase excitation drive mode, and 1-2 phase excitation drive mode can be selected by using external pins.

Figure 7–1. Concept of Micro Step Drive Operation



7.4 Input Signals (CLK, OE and CW pins, stepping motor control methods)

The motor is driven by the pulses input to the CLK_1 (CLK_2) pin. The pulses advance by one at the rising and falling edges of the CLK_1 (CLK_2) signal.

When the CLK_1 (CLK_2) pin is fixed to low levels, the internal excitation positions do not progress, regardless of the input status of the OE_1 (OE_2) pin.

Since 1 electrical angle cycle is divided by 128, it equals 1 electrical angle cycle because of the 64-clock input.

Since both edges are used for control, the pulse intervals that are output rely on the pulse duty which is input. It is suggested that pulses with a duty of 50% should be input.

The rotational direction of the motor is set by CW_1 (CW_2).

In CW mode, the current for ch2 (ch4) is output delayed by a 90º phase in relation to the current for ch1 (ch3).

In CCW mode, the current for ch2 (ch4) is output advanced by a 90º phase in relation to the current for ch1 (ch3).

7.5 Output Enable (OE) Pin

The OE_1 (OE_2) pin can be used to forcibly stop pulse output of ch1 and ch2 (or ch3 and ch4).

When OE_1 (OE_2) = L, the output is forcibly made to go into Hi-Z. Moreover, since an internal excitation position can make it go on also at OE_1 (OE_2) pin = L, an internal excitation position advances in inputting a pulse into CLK_1 (CLK_2) pin.

The internal information will be held if OE_1 (OE_2) = L and CLK_1 (CLK_2) pin are fixed to low level. Motor position information is memorized unless it is reset. In performing stepping motor control, be sure to give as OE_1 (OE_2) = H.

7.6 Current Detection Resistor Connection (FB) Pin

(1) ch1 to ch4

The current detection resistor is connected when current driving is necessary. It is used for micro step driving and solenoid driving. The peak value (at 100% current of ch1 (ch3) or ch2 (ch4)) of output current is decided by the resistance R_{FB} linked to FB_1 (FB_3) and FB_2 (FB_4). This IC contains the reference power supply V_{REF} for current value comparison (500 mV TYP.) in the internal, and performs the drive which makes the current value acquired from R_{FB} and V_{REF} an output current peak value.

The current that flows into the output is {500 mV (reference voltage) /FB pin resistance x 1000}.

Peak output current: I_{MAX} (A) ≅ V_{REF} (V) ÷ R_{FB} (Ω) x 1000

Example) Where FB = 4.7 kΩ

Output current = 500 (mV) /4.7 (kΩ) x 1000

≅ 106.4 (mA)

This means constant current driving of about 106.4 mA.

When current driving is not performed, connect the FB pin to GND.

(2) ch7

Connect the current detection circuit between the source of the driver low side and GND. Because the circuit is configured to detect current directly, connect a detection resistor of low resistance (1 Ω maximum).

The current that flows into the output is {200 mV (reference voltage) /FB_7 pin resistance} (when SEL_7 = H).

Output current: I_{MAX} (A) ≅ V_{REF} (V) ÷ R_{FB} (Ω)

Example) Where FB_7 = 0.5 Ω

Output current = 200 (mV) /0.5 (Ω)

= 400 (mA)

This means constant current driving of 400 mA.

Because only ch7 employs the linear drive mode and directly detects the output current, the current accuracy is determined only by the external resistor and the offset of the current control amplifier.

The above example shows ($SELV_{REF7}$ = H) using the internal reference voltage. When applying reference voltage externally, set $SELV_{REF7}$ to L, then apply voltage to the V_{REF7} pin. The output current can be calculated by transposing 200 mV in the computational expression.

7.7 Selecting 2-phase Excitation/Micro Step Drive Mode

The 2-phase excitation, 1-2 phase excitation, or micro step drive mode can be selected by using the $MODE_1$ to $MODE_4$ pins. Refer to **Table 5–1. Mode Pin Truth Table** for details.

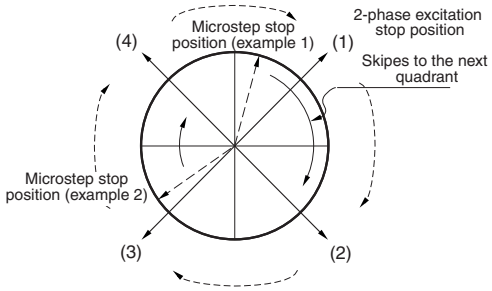
Immediately after release of reset, the IC is initialized. In the 1-2 phase excitation and micro step drive mode, excitation is started from the position where the output current of ch1 (ch3) is 100% and output current of ch2 (ch4) is 0%. In the 2-phase excitation drive mode, excitation is started from the position where the currents of both ch1 (ch3) and ch2 (ch4) are +100%.

When the mode is changed from the micro step driving to the 2-phase excitation (or 1-2 phase excitation), the position of micro step is held until CLK is input.

When the rotation direction does not change, pulse output is started by the first CLK input, the position is skipped to the 2-phase position of the next quadrant (or to the closest 1-2 phase position at the rotation direction destination), and driving is started.

When the rotation direction changes, it is skipped to 2-phase position of the next quadrant, or 1-2-phase position to the direction which changed, and a drive is started.

Figure 7–2. Concept of Change Operation, Micro Step Driving ↔ 2-phase Excitation (1-2 Phase Excitation)



7.8 Under-voltage Lockout (UVLO) Circuit

This function is to forcibly stop the operation of the IC to prevent malfunctioning if V_{DD} drops. When UVLO operates, the IC is in the reset status. If V_{DD} drops abruptly in the order of several μs, this function may not operate.

7.9 Overheat Protection (TSD) Circuit

This function is to forcibly stop the operation of the IC to protect it from destruction due to overheating if the chip temperature of the IC rises.

The overheat protection circuit operates when the chip temperature rises to 150°C or more. When overheat is detected, all the circuits are stopped. When reset state or when UVLO is detected, the overheat protection circuit does not operate.

7.10 Power Up Sequence

This IC has a circuit that prevents current from flowing into the V_M pin when V_{DD} = 0 V. Therefore, the current that flows into the V_M pin is cut off 1 μA MAX. when V_{DD} = 0 V.

8. NOTE ON CORRECT USE

8.1 Transmitting Data

Data input at reset state is ignored.

8.2 Pin Processing of Unused Circuit

The input/output pins of an unused circuit must be processed as specified below.

A V_M power supply pin is provided for each output circuit. The current consumption of the internal circuit can be reduced by dropping the V_M power of the unused circuit to GND. However, if there are multiple power supply pins, be sure to connect all of them to the same potential.

<ch1, ch2>

Lower OE_1, CLK_1, and CW_1.

Open FIL_1, FIL_2, OUT_{1A}, OUT_{1B}, OUT_{2A}, and OUT_{2B}.

Connect FB_1 and FB_2 to GND.

<ch3, ch4>

Set the general-purpose drive mode.

Lower OE_2/IN_{3A}, CLK_2/IN_{3B}, CW_2/IN_{4A}.

Higher $MODE_4/IN_{4B}$.

Open FIL_3, FIL_4, OUT_{3A}, OUT_{3B}, OUT_{4A}, and OUT_{4B}.

Connect FB_3 and FB_4 to GND.

<ch5, ch6>

Lower IN_{5A} (IN_{6A}) and IN_{5B} (IN_{6B}) .

Open OUT_{5A} (OUT_{6A}) and OUT_{5B} (OUT_{6B}) .

<ch7>

Lower SEL_7, $SELV_{REF7}$, IN_{7A}, and IN_{7B}.

Open OUT_{7A} and OUT_{7B}.

Connect V_{REF7}, FIL_7, FB_7, and R_7 to GND.

8.3 Input Pin Processing

The signal input pins for this IC are not equipped with on-chip pull down/pull up resistors. When the V_{DD} power is on, the logic for all of the input pins must be set to either H or L.

9. STEPPING MOTOR DRIVING WAVEFORM

Figure 9–1. 2-phase Excitation Output Mode

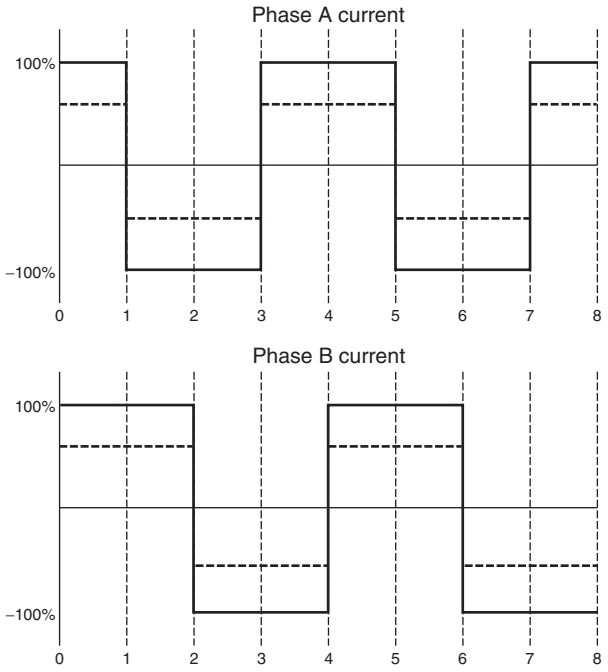
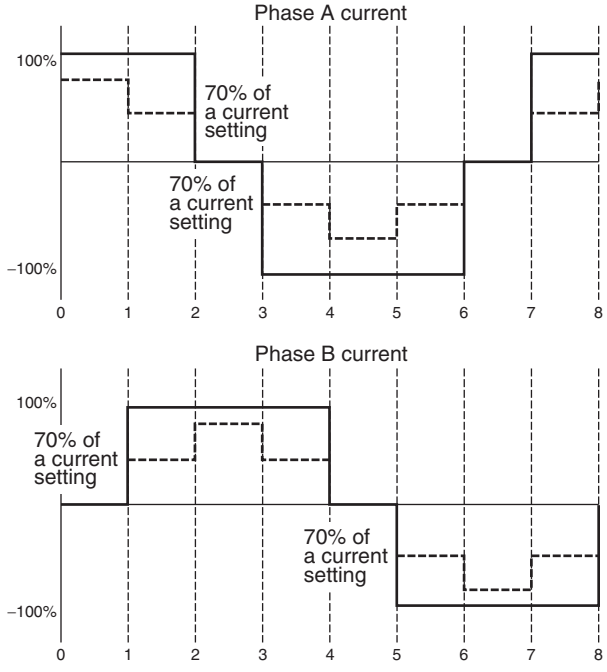
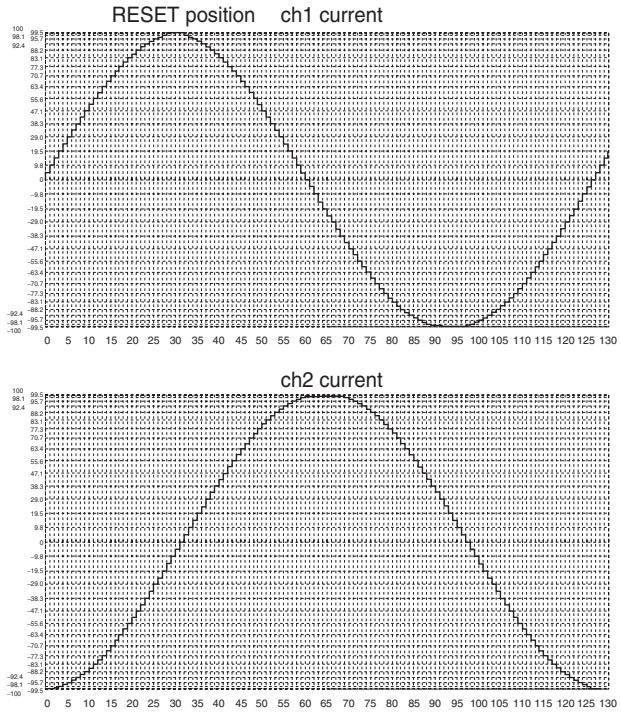


Figure 9–2. 1-2 Phase Excitation Output Mode



Remark Solid line: Output duty 100% drive, Dotted line: Current control drive (The current is in accordance with the current setting.)

Figure 9–3. Micro Step Drive Mode



Remark The horizontal axis of the above charts indicates the number of steps. The above charts show an example in the CW (forward) mode.

The current flowing into phases A and B is positive in the direction from OUT pin A to OUT pin B, and negative in the direction from OUT pin B to OUT pin A. Because the micro step drive mode is in 128 steps, it equals 1 electrical angle cycle.

10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, glass epoxy 4-layer board of 100 mm x 100 mm x 1.6 mm with copper foil area of 50%)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Control block	−0.5 to +6.0	V
	V_M	Motor block	−0.5 to +6.0	V
Input voltage	V_{IN}		−0.5 to V_{DD} +0.5	V
Output pin voltage	V_{OUT}	Motor block	6.2	V
DC output current (ch1 to 6ch)	$I_{D(DC)}$	DC (during output independent operation)	±0.4	A/ch
DC output current (ch7)	$I_{D(DC)}$	DC (during output independent operation)	±0.5	A/ch
Instantaneous output current	$I_{D(pulse)}$	PW < 10 ms, Duty Cycle ≤ 20% (during output independent operation)	±0.7	A/ch
Power consumption	P_T		1.5	W
Peak junction temperature	$T_{ch(MAX)}$		150	°C
Storage temperature	T_{stg}		−55 to +150	°C

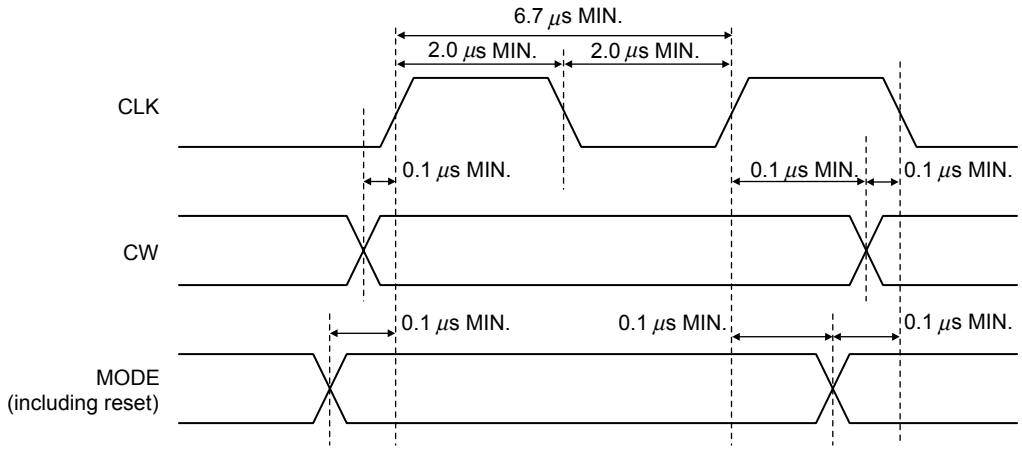
Remark The overheat protection circuit operates at T_{ch} > 150°C. When overheat is detected, all the circuits are stopped. The overheat protection circuit does not operate at reset or on detection of ULVO.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = 25°C, glass epoxy 4-layer board of 100 mm x 100 mm x 1.6 mm with copper foil area of 50%)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}	Control block	2.7		3.6	V
	V_M	Motor block	2.7		5.5	V
Input voltage	V_{IN}		0		V_{DD}	V
DC output current (ch1 to 6ch)	$I_{D(DC)}$	DC (during output independent operation)	−0.3		+0.3	A/ch
DC output current (ch7)	$I_{D(DC)}$	DC (during output independent operation)	−0.4		+0.4	A/ch
Instantaneous output current	$I_{D(pulse)}$	PW < 10 ms, Duty Cycle ≤ 20% (during output independent operation)	−0.6		+0.6	A/ch
Capacitor capacitance		COSC (during 300 kHz TYP. oscillation)		100		pF
ch7 reference voltage input range	V_{REF7}		0.1		0.7	V
Logic input frequency	f_{IN}				150	kHz
Operating temperature range	T_A		−10		75	°C

Figure 10–1. AC timing waveform



Electrical Characteristics (Unless otherwise specified, T_A = 25°C, V_{DD} = 3.0 V, V_M = 3.0 V)

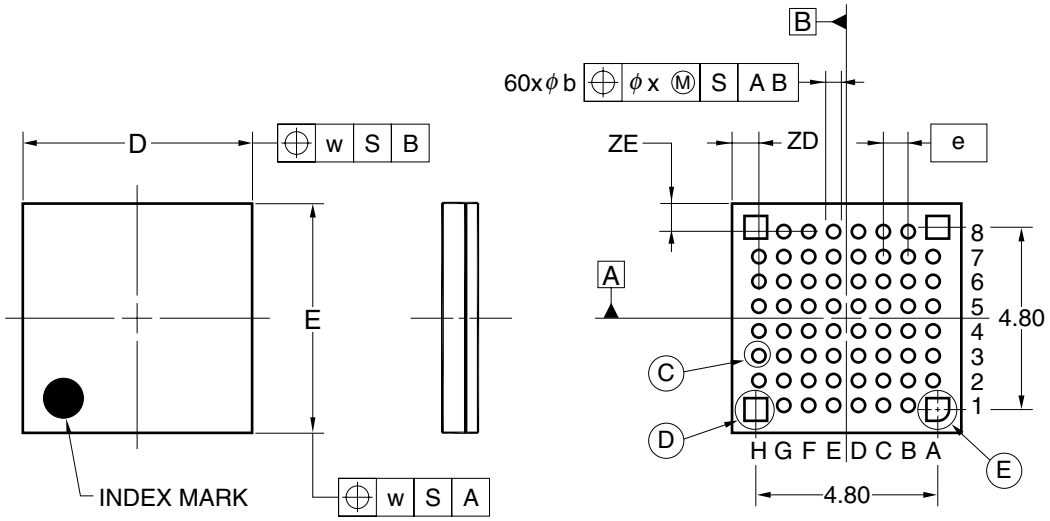
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
V_{DD} pin current in standby mode	$I_{DD(STB)}$	During reset			1.0	μA
V_{DD} pin current in during operation	$I_{DD(ACT)}$	During non-reset			5.0	mA
High-level input current	I_{IH}	$V_{IN} = V_{DD}$			1.0	μA
Low-level input current	I_{IL}	V_{IN} = 0 V	−1.0			μA
High-level input voltage	V_{IH}		0.7 x V_{DD}			V
Low-level input voltage	V_{IL}				0.3 x V_{DD}	V
COSC oscillation frequency	f_{OSC}	COSC = 150 pF		200		kHz
H-bridge on-state resistance	R_{on}	I_M = 0.3 A, sum of upper and lower stages (ch1 to ch4, and ch7)		1.0	1.5	Ω
	R_{on56}	I_M = 0.3 A, sum of upper and lower stages (ch5 and ch6)		1.5	2.0	Ω
Output leakage current [Note1]	$I_{M(off)}$	Per V_M pin, All control pin: low level			1.0	μA
Low-voltage detection voltage	V_{DDS}			1.7	2.5	V
Internal reference voltage [Note2]	V_{REF}	ch1 to ch4	450	500	550	mV
	V_{REF7}	ch7, during $SELV_{REF7}$ = H	180	200	220	mV
Current detection ratio [Note2]		I_M = 0.1 A, with sense resistor of 5 kΩ, ch1 to ch4	900	1000	1100	
Output turn-on time	t_{on}	R_L = 20 Ω, ch1 to ch6	0.02	0.35	1.0	μs
Output turn-off time	t_{off}		0.02	0.35	1.0	μs

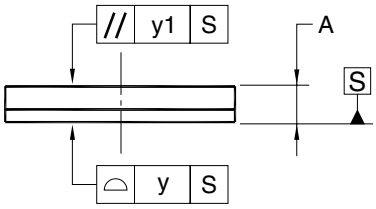
Notes 1. This IC has a circuit that prevents current from flowing into the V_M pin when V_{DD} = 0 V.

2. The accuracy of the output current for ch1 to ch4 depends upon the motor that is actually used, but the current fluctuations of the IC are determined by reference voltage and current detection ratios. Assume that the total of the reference voltage V_{REF} and current sense circuit errors are equal to ±10%.

11. PACKAGE DRAWING

64-PIN PLASTIC FLGA (6x6)





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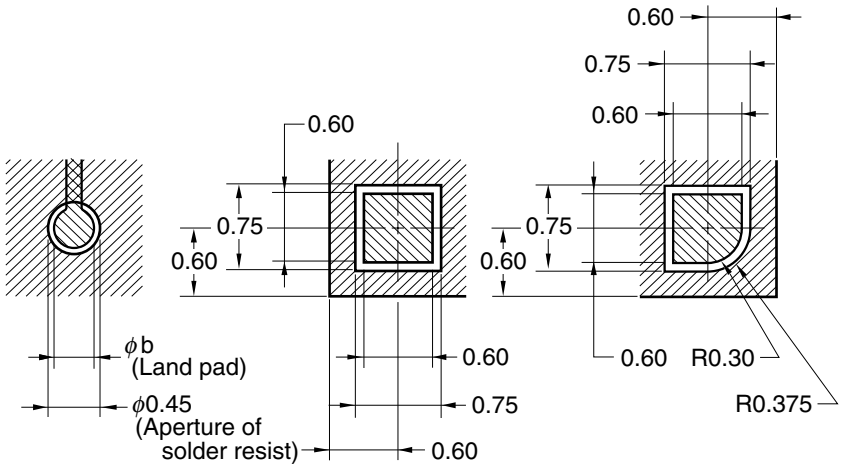

(UNIT:mm)

ITEM	DIMENSIONS
D	6.00±0.10
E	6.00±0.10
w	0.20
e	0.65
A	0.91±0.07
b	0.35±0.05
x	0.08
y	0.10
y1	0.20
ZD	0.725
ZE	0.725

P64FC-65-BA2

12. RECOMMENDED SOLDERING CONDITIONS

The μPD168117A should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Type of Surface Mount Device

μPD168117AFC-BA2-E1-A[Note1]: 64-pin plastic FLGA (6 x 6)

Process	Conditions	Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds MAX. (at 220°C or higher) , Count: Three times or less, Exposure limit: 3 days[Note2] (after that, prebake at 125°C for 10 hours) , Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended. <Precaution> Products other than in heat-resistant trays (such as those packaged in a magazine, taping, or non-thermal-resistant tray) cannot be baked in their package.	IR60-103-3

Notes 1. Pb-free (This product does not contain Pb in external electrode and other parts.)

2. After opening the dry pack, store it a 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating) .

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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