TC8540F

TENTATIVE

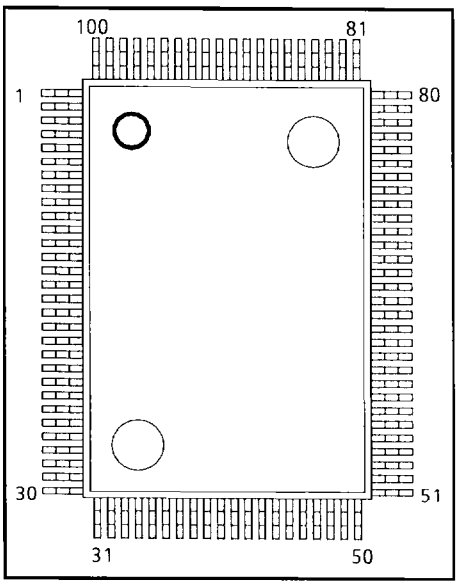
Bus Interface Adapter

1. GENERAL DESCRIPTION

The TC8540F is a bus interface adapter (BIA) for converting the system interface of the hard disk control system, which is composed of the hard disk controllers T7518, and the VFOs, TC8663AF-88, TC8563AF-89, TC8564AF, into the interface compatible with the IBM PC/XT. This BIA is composed of the host interface, the CPU interface and the HDD control section.

The host interface section functions as the interface capable of direct connection with the bus of the IBM PC/XT. Especially in the data transfer through the DMA, the transfer rate can be increased up to max. 1.25MB/S. In addition, the transfer through the I/O is also made possible.

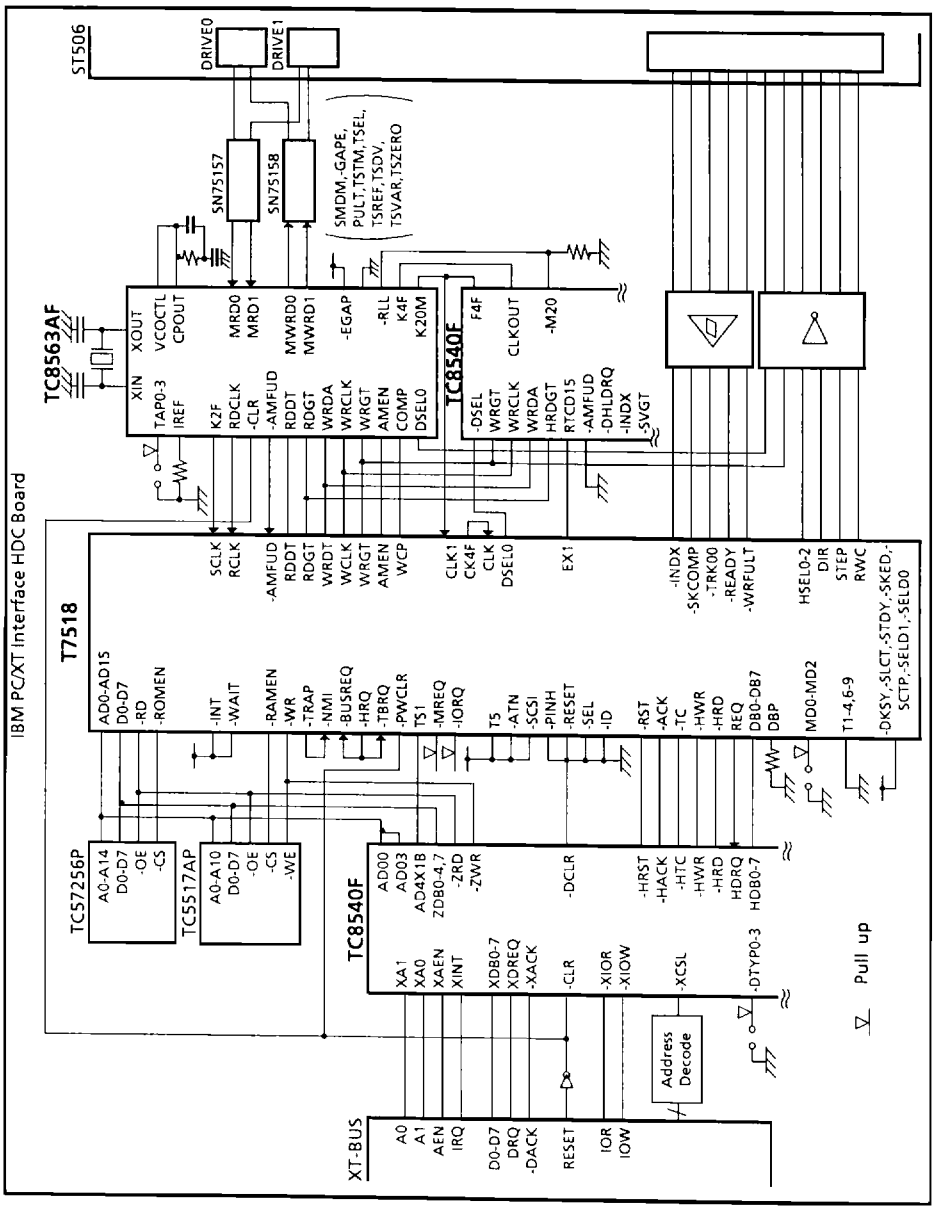
The CPU interface section provides the CPU in the hard disk controller with the extension I/O port to make the extension of the hard disk controller function possible. The HDD control section prepares the signal for drive control making possible the extension of the general-purpose characteristics of the drive to be connected.



2. FEATURES

- Si-gate high speed CMOS technology
- +5V single power supply
- 100 pin flat package
- Direct connection to IBM PC/XT compatible interface
- Direct connection to HDC T7518 buses
- DMA transfer rate 1.25MB/S

3. TYPICAL APPLIED SYSTEM CONFIGURATION



4. PIN DESCRIPTION

4.1 PIN CONFIGURATION

NO.	I/O	PIN NAME	NO.	I/O	PIN NAME	NO.	I/O	PIN NAME
1	O	-HINDX	36	I	-AMFUD	71		NC
2	O	-HSCTP	37		NC	72		NC
3	V	VDD	38	I	F4F	73	I	XA1
4	O	-HAMFD	39	I	-INDX	74	I	XA0
5	I	HRDGT	40	G	VSS	75	I	EXT31
6	O	-WTGT	41		NC	76	I	EXT11
7	I	WRDA	42	I	-SVGT	77	I	EXT01
8		NC	43	I	WRGT	78	V	VDD
9	I	WRCLK	44	O	PSAVE	79	I	-M20
10	I	-DSEL	45		NC	80	I	-DTYP0
11	I	RTCD15	46	I	-CLR	81	I	-DTYP1
12	I	-DHLDRQ	47	I	XAEN	82	I	-DTYP2
13		NC	48		NC	83	I	-DTYP3
14	I/O	HDB7	49	O	XINT	84	I/O	ZDB0
15	G	VSS	50		NC	85	I/O	ZDB1
16	I/O	HDB6	51	I/O	XDB7	86	I/O	ZDB2
17		NC	52	I/O	XDB6	87		NC
18	I/O	HDB5	53	V	VDD	88	I/O	ZDB3
19	I/O	HDB4	54	I/O	XDB5	89	I/O	ZDB4
20	I/O	HDB3	55	I/O	XDB4	90	G	VSS
21	I/O	HDB2	56	I/O	XDB3	91		NC
22	I/O	HDB1	57	I/O	XDB2	92	I/O	ZDB7
23		NC	58		NC	93	I	AD03
24	I/O	HDB0	59	I/O	XDB1	94	I	AD00
25	I	HDRQ	60	I/O	XDB0	95		NC
26	I	AD4X1B	61	O	XDRQ	96	I	-ZWT
27	O	-HRST	62		NC	97	I	-ZRD
28	V	VDD	63		NC	98		NC
29	O	-HWR	64	I	-XACK	99	O	-DCLR
30	O	-HRD	65	G	VSS	100	O	-HLDRQ
31	O	-HTC	66	I	-XIOR			
32	O	-HACK	67		NC			
33	O	CLKOUT	68	I	-XIOW			
34	O	WRDTA	69		NC			
35	O	RDGT	70	I	-XCSL			

4.2 PIN FUNCTION

NO.	PIN NAME	I/O	PIN FUNCTION
1	-HINDX	O	Index signal (-INDEX) or servo gate (-SVGT) is output. Selection is made by INDX 1 bit of internal register (W28).
2	-HSCTP	O	-SVGT signal gated by HRD bit of internal register (W28) is output (HRD = 1).
3	VDD	V	Connected to power supply VDD (+ 5V).
4	-HAMFD	O	-AMFUD signal gated by HRD bit of internal register (W28) is output (HRD = 0).
5	HRDGT	I	RDGT from HDC is input.
6	-WTGT	O	Write gate signal to disk.
7	WRDA	I	Write data (NRZ signal) from HDC is input.
8	NC		
9	WRCLK	I	Write clock from HDC is input.
10	-DSEL	I	Drive select signal from HDC is input.
11	RTCD15	I	Data, which is output from WRDTA at "High", is forcibly turned into "4E" pattern.
12	-DHLDRQ	I	Bus request signal input.
13	NC		
14	HDB7	I/O	Connected to host data bus of HDC.
15	VSS	G	Connected to power supply GND.
16	HDB6	I/O	Connected to host data bus of HDC.
17	NC		
18	HDB5	I/O	Connected to host data bus of HDC.
19	HDB4	I/O	
20	HDB3	I/O	
21	HDB2	I/O	
22	HDB1	I/O	
23	NC		
24	HDB0	I/O	Connected to host data bus of HDC.
25	HDRQ	I	Data request signal (REQ) from HDC is connected.
26	AD4X1B	I	I/O decode signal (TS1) from HDC is connected.
27	-HRST	O	Data transfer control signal to HDC.
28	VDD	V	Connected to power supply VDD (+ 5V).
29	-HWR	O	Data transfer control signal to HDC.
30	-HRD	O	Data transfer control signal to HDC.
31	-HTC	O	Data transfer control signal to HDC.
32	-HACK	O	Data transfer control signal to HDC.

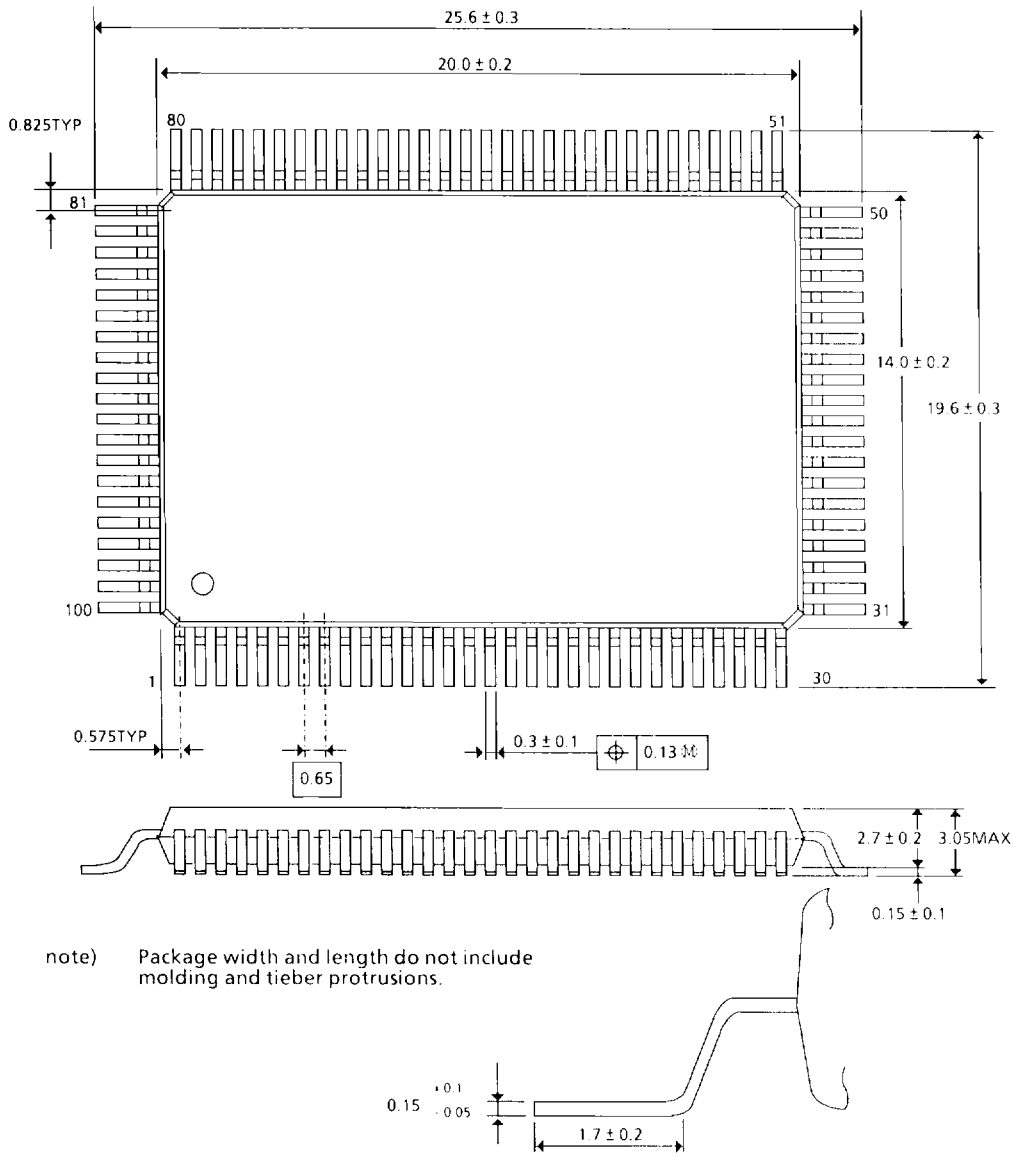
NO.	PIN NAME	I/O	PIN FUNCTION
33	CLKOUT	O	Clock which is input from F4F, or clock of its 1/2 division is output. Controlled by -M20 signal. At -M20 = "High", clock of 1/2 division is output.
34	WRDTA	O	Write data output to VFO (NRZ signal).
35	RDGT	O	Read gate signal to VFO.
36	-AMFUD	I	Address mark detection signal from VFO is input.
37	NC		
38	F4F	I	Clock signal which is the base of output to CLKOUT.
39	-INDX	I	Index signal from disk is input.
40	VSS	G	Connected to power supply GND.
41	NC		
42	-SVGT	I	Servo gate signal from disk is input.
43	WRGT	I	Write gate signal (WRGT) from HDC is input.
44	PSAVE	O	Power save signal to disk. Becomes "High", when drive is not selected (-DSEL = "Low") or SSBSY1 signal (busy signal) is not "1" internally.
45	NC		
46	-CLR	I	System reset signal which is reset at "Low".
47	XAEN	I	Control signal of XT bus.
48	NC		
49	XINT	O	Control signal of XT bus.
50	NC		
51	XDB7	I/O	Data bus of XT bus.
52	XDB6	I/O	
53	VDD	V	Connected to power supply VDD (+ 5V).
54	XDB5	I/O	Data bus of XT bus.
55	XDB4	I/O	
56	XDB3	I/O	
57	XDB2	I/O	
58	NC		
59	XDB1	I/O	Data bus of XT bus.
60	XDB0	I/O	
61	XDREQ	O	Control signal of XT bus.
62	NC		
63			
64	-XACK	I	Control signal of XT bus.
65	VSS	G	Connected to power supply GND.
66	-XIOR	I	Control signal of XT bus.

NO.	PIN NAME	I/O	PIN FUNCTION
67	NC		
68	-XIOW	I	Control signal of XT bus.
69	NC		
70	-XCSL	I	Control signal of XT bus.
71	NC		
72			
73	XA1	I	Address bus of XT bus.
74	XA0	I	
75	EXT31	I	General-purpose input port. This port address is 28H.
76	EXT11	I	
77	EXT01	I	
78	VDD	V	Connected to power supply GND (+ 5V).
79	-M20	I	Clock division changeover signal. The same signal as RLL (MFM/RLL changeover signal) of VFO is input. VFO of quadrupled transfer rate as X'tal is used in MFM mode and that of doubled transfer rate is used in RLL mode. Since system clock always requires the doubled transfer rate, input X'tal frequency to F4F and fetch system clock from CLKOUT.
80	-DTYP0	I	Switch input terminal. Can be read by VTYP register from host side.
81	-DTYP1	I	
82	-DTYP2	I	
83	-DTYP3	I	
84	ZDB0	I/O	Connected to CPU data bus of HDC.
85	ZDB1	I/O	
86	ZDB2	I/O	
87	NC		
88	ZDB3	I/O	Connected to CPU data bus of HDC.
89	ZDB4	I/O	
90	VSS	G	Connected to power supply GND.
91	NC		
92	ZDB7	I/O	Connected to CPU data bus of HDC.
93	AD03	I	Connected to CPU address bus of HDC.
94	AD00	I	
95	NC		
96	-ZWT	I	Connected to -WR of HDC.
97	-ZRD	I	Connected to -RD of HDC.
98	NC		
99	-DCLR	O	Reset signal to HDC. Connected to -RESET.
100	-HLDRQ	O	Hold request signal to HDC. Connected to -BUSREQ, TBRQ.

7. PACKAGE DIMENSION

QFP100-P-1420B

Unit : mm



note) Package width and length do not include molding and tieber protrusions.