IDT821024
Non-Programmable Quad PCM CODEC

Preliminary Data Sheet, December 2000 (Ver 1.0)

File No. IDT821024DS(L)

Features

- 4 channel CODEC with on-chip filters
- Selectable A-law or μ-law companding
- Master clock frequency selection: 2.048 MHz, 4.096 MHz or 8.192 MHz
  – Internal timing automatically adjusted based on MCLK and frame sync signal
- Separate PCM and master clock
- Single PCM port with up to 8.192 MHz operation (128 channels)
- Transhybrid balance impedance hardware programmable via external components
- Transmit gains hardware programmable via external components
- Low power +5.0 V CMOS technology
- +5.0 V single power supply
- Instant recovery after audio reception/transmission interrupted by spurious transient states.
- Package available:
  IDT821024-XL 32 pin PLCC

Description

The IDT821024 is a single-chip, four channel PCM CODEC with on-chip filters. The device provides both μ-law and A-law companding digital-to-analog and analog-to-digital conversions based on ITU-T G.711 - G.714 specifications. It also provides the two-to-four wire conversion function (the external balance impedance required). The digital filters in IDT821024 provides the necessary transmit and receive filtering for voice telephone circuit to interface with time-division multiplexed systems. All of the digital filters are performed in digital signal processors operating from an internal clock, which is derived from MCLK. The fixed filters set the transmit and receive gain and frequency response.
In IDT821024, the PCM data is read and written to the PCM highway in time slots determined by the individual Frame Sync signals (FSR_n and FSX_n, where n = 1–4) at rates from 256 KHz to 8.192 MHz. Both Long and Short Frame Sync modes are available in the device.

The IDT821024 can be used in digital telecommunication applications such as PBX, Central Office Switch, Digital Telephone and Integrated Voice/Data Access Unit.

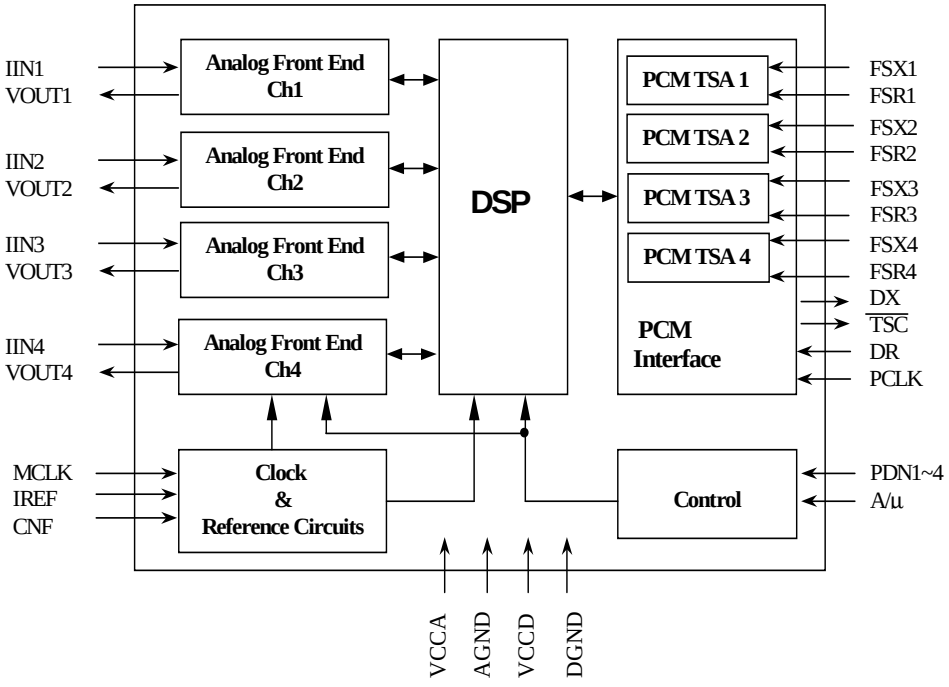


Figure-1. Block Diagram

Pin Connection

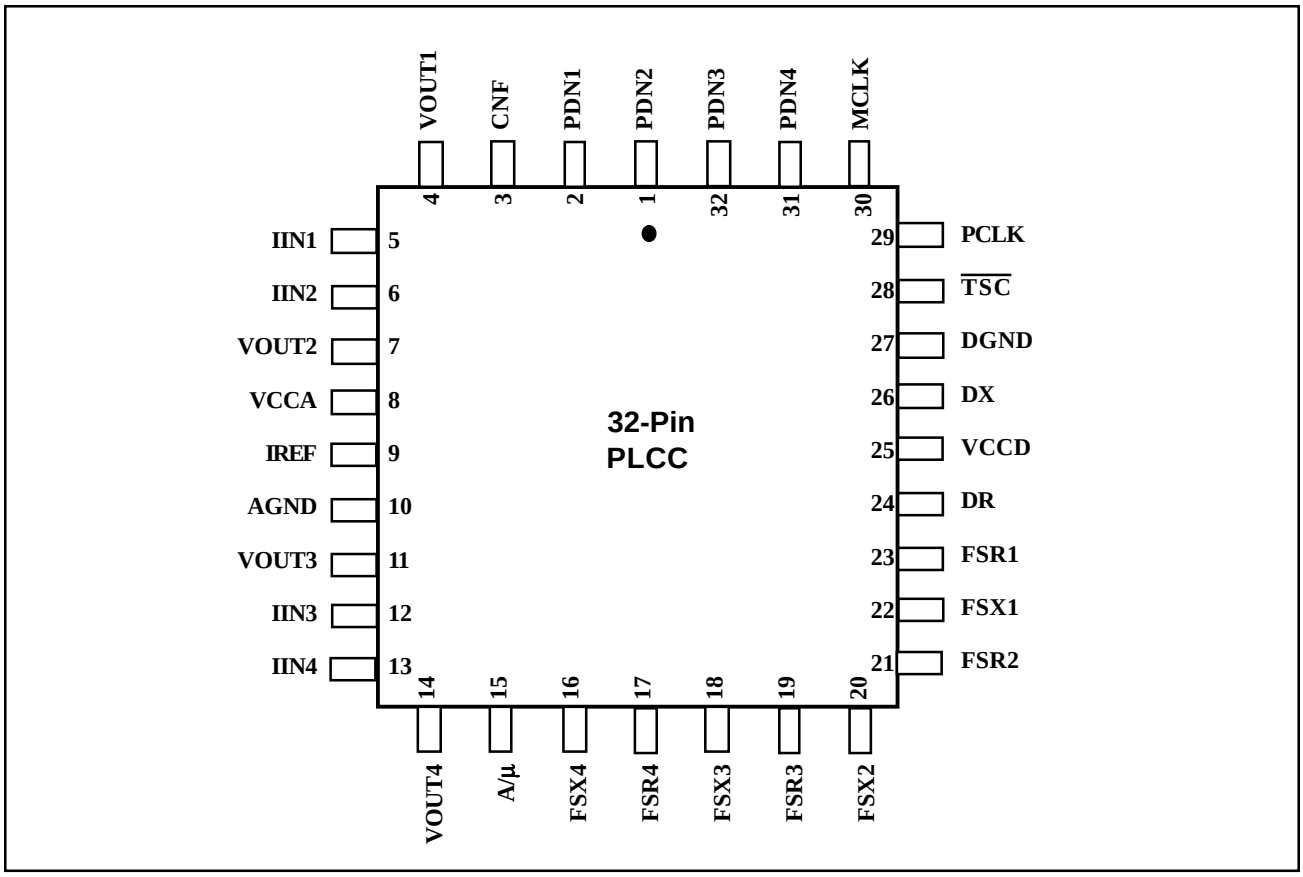


Figure-2. Pin Assignment

Pin Description

Name	Type	Pin Number	Description
AGND	--	10	**Analog Ground.** All ground pins should be connected to the ground plane of the circuit board.
VCCA	--	8	**+5 V Analog Power Supply.** All power supply pins should be connected to the power plane of the circuit board.
DGND	--	27	**Digital Ground.** All ground pins should be connected to the ground plane of the circuit board.
VCCD	--	25	**+5 V Digital Power Supply.** All power supply pins should be connected to the power plane of the circuit board.
DR	I	24	**Receive PCM Data Input.** The PCM data for Channels 1, 2, 3 and 4 is shifted serially into DR pin during the time slot determined by the Receive Frame Sync Signal (FSR) with MSB first. A byte of data for each channel is received every 125 µs at the PCLK rate.
DX	O	26	**Transmit PCM Data Output.** The PCM data for Channels 1, 2, 3 and 4 is shifted serially out of DX pin during the time slot determined by the Transmit Frame Sync Signal (FSX) with MSB first. A byte of data for each channel is transmitted every 125 µs at the PCLK rate. DX is high impedance between time slots.
FSR1 FSR2 FSR3 FSR4	I	23 21 19 17	**Receive Frame Sync Input for Channel 1/2/3/4** This 8kHz signal pulse identifies the receive time slot for Channel N on a system's receive PCM frame. It must be synchronized to PCLK.
FSX1 FSX2 FSX3 FSX4	I	22 20 18 16	**Transmit Frame Sync Input for Channel 1/2/3/4** This 8 kHz signal pulse identifies the transmit time slot for Channel N on a system's transmit PCM frame. It must be synchronized to PCLK.
IREF	O	9	**Reference Current.** The IREF1 output is biased at the internal reference voltage.
VOUT1 VOUT2 VOUT3 VOUT4	O	4 7 11 14	**Voice Frequency Receiver Output for Channel 1/2/3/4** This is the output of receiver power amplifier for Channel N. The received digital data at DRA is processed and converted to an analog signal at this pin.
I1IN1 I1IN2 I1IN3 I1IN4	I	5 6 12 13	**Voice Frequency Transmitter Input for Channel 1/2/3/4** This is the input to the gain setting amplifier in the transmit path for Channel N. The analog voice band voltage signal is applied to this pin through a resistor. This input is a virtual AC ground input which is biased at the IREF1 pin. The audio signal is processed and converted into an digital signal for DXA.
MCLK	I	30	**Master Clock.** The Master Clock provides the clock for DSP. It can be either 2.048 MHz or 4.096 MHz. The device determines the MCLK frequency by the FSX inputs and makes the necessary internal adjustments automatically. The MCLK must be an integer multiple of the FSX frequency.
PCLK	I	29	**PCM Clock.** The PCM Clock shifts out PCM data from DXA pin and shifts in PCM data on DRA pin. It is an integer multiple of the frame sync frequency. When PCLK is connected with MCLK, it can generate the DSP clock as well.
$\overline{TSC}$	O	28	**Time Slot Control.** This open drain output is low active. When PCM data is transmitted on DXA pin for any of the four channels, this pin will be pulled low.

Pin Description(continued)

Name	Type	Pin Number	Description
A/μ	I	15	**A/μ-Law Selection.** When this pin is low, μ-Law is selected; when this pin is high, A-Law is selected. This pin can be connected to VCCD or DGND pin directly.
PDN1 PDN2 PDN3 PDN4	I	2 1 32 31	**Channel 1/2/3/4 Power Down.** When this pin is high, Channel N is powered down.
CNF	O	3	**Capacitor For Noise Filter.** This pin should be connected to AGND via a 0.1μF capacitor.

Functional Description

The IDT821024 contains four channel PCM CODEC with on chip digital filters. It provides the four-wire solution for the subscriber line circuitry in digital switches. The device converts analog voice signal into digital PCM samples, and converts digital PCM samples back into analog signal. Digital filters are used to bandlimit the voice signals during conversion. Either A-law or μ-law is supported by IDT821024, and the law selection is performed by A/μ pin.

The frequency of the master clock (MCLK) can be 2.048 MHz, 4.096 MHz, or 8.192 MHz. Internal circuitry determines the master clock frequency automatically.

Four channels of serial PCM data are time multiplexed via two pins, DX and DR. The time slots of the four channels are determined by the individual Frame Sync signals at rates from 256 kHz to 8.192 MHz. For each channel, the IDT821024 provides a transmit and receive Frame Sync input.

The IDT821024 can be powered down on a per-channel basis to save power consumption. Channel Power Down Pins PDN1-4 configures channels to be active (power-on) or standby (power-down) specificly.

Operation Control

The following operation description applies to all four channels of the IDT821024.

Power-on Sequence and Master Clock Configuration

To power on IDT821024, users should follow this sequence:
1. Apply ground;
2. Apply VCC, finish signal connections;
3. Set PDN1-4 pins high, thus all of the 4 channels are powered down;

The master clock (MCLK) frequency of IDT821024 can be configured as 2.048 MHz, 4.096 MHz and 8.192 MHz. Using the Transmit Frame Sync (FSX) inputs, the device determines the MCLK frequency and makes the necessary internal adjustments automatically. The MCLK frequency must be an interger multiple of the Frame Sync frequency.

Operating Modes

There are two operating modes for each transmit or receive channel: standby mode (when the channel is powered down) and normal mode (when the channel is powered on). In standby mode, all circuits are powered down with the analog outputs placed in high impedance state.

Each of the four channels in the IDT821024 can be in either normal mode or standby mode. The mode selection of each channel is done by its corresponding PDN pin. When PDNn is 1, Channel N is in standby mode; when PDNn is 0, Channel N is in normal mode.When in normal mode, each channel of the IDT821024 is able to transmit and receive both PCM and analog information. This is the operating mode when a telephone call is in progress.

Companding Law Selection

A device pin A/μ is provided by IDT821024 for the companding law selection. When the pin is low, μ-law is selected; when the pin is high, A-law is selected.

Signal Processing

High performance oversampling Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) are used in the IDT821024 to provide the required conversion accuracy. The associated decimation and interpolation filters are realized with both dedicated hardware and Digital Signal Processor (DSP). The DSP also handles all other necessary functions such as PCM bandpass filtering and sample rate conversion.

Transmit Signal Processing

In the transmit path, the analog input signal is received by the ADC and converted into digital data. The digital output of the oversampling ADC is decimated and sent to the DSP. The transmit filter is implemented in the DSP as a digital bandpass filter. The filtered signal is further decimated and compressed to PCM format.

Transmit PCM Interface

The transmit PCM interface clocks out 1 byte (8 bits) PCM data out of DX pin every 125 µs. The transmit logic, synchronized by the Transmit Frame Synchronization signal (FSXn), controls the data transmission. The FSXn pulse identifies the transmit time slot of the PCM frame for Channel N. The PCM Data is transmitted serially on DX pin with the Most Significant Bit (MSB), or Bit 1, first. When the PCM data is being output on DX pin, the $\overline{TSC}$ signal will be pulled low

Receive Signal Processing

In the receive path, the PCM code is received at the rate of 8,000 samples per second. The PCM code is expanded and sent to the DSP for interpolation and receive channel filtering function. The receive filter is implemented in the DSP as a digital lowpass filter. The filtered signal is then sent to an oversampling DAC. The DAC output is post-filtered and then delivered at VOUT pin by a power amplifier. The amplifier can drive resistive load higher than 2 KΩ.

Receive PCM Interface

The receive PCM interface clocks 1 byte (8 bits) PCM data into DR pin every 125 µs. The receive logic, synchronized by the Receive Frame Synchronization signal (FSRn), controls the data transmission. The FSRn pulse identifies the receive time slot of the PCM frame for Channel N. The PCM Data is received serially on DR pin with the Most Significant Bit (MSB), or Bit 1, first.

Hardware Gain Setting In Transmit Path

The transmit gain of IDT821024 for each channel can be set by 2 resistors, R_{REF} and R_{TXn} (as shown in Figure-3), according to the following equation:

$$Gt = \frac{3 * R_{REF}}{R_{TXn}}$$

The receive gain of IDT821024 is fixed and equal to 1.

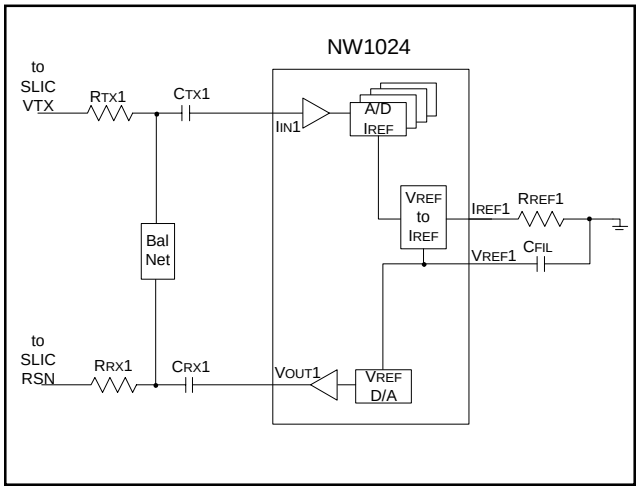


Figure 3. IDT821024 Transmit Gain Setting for Channel 1

Maximum Rating - Exceeding the following listed values may cause permanent damage, functional operation not implied.

Power Supply Voltage: ≤ 6.5 V
Voltage on Any Pin with Respect to Ground: -0.5 V to VDD + 0.5 V
Package Power Dissipation: ≤ 600 mW
Storage Temperature: -65 °C to +150 °C

Recommended Operating Conditions

Operating Temperature: -40 °C to +85 °C
Power Supply Voltage: 4.75 V to 5.25 V
MCLK: 2.048 MHz, 4.096 MHz, or 8.192 MHz with tolerance of ± 50 ppm

Electrical Characteristics

Digital Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
V_{IL}	Input Low Voltage			0.8	V	All digital inputs
V_{IH}	Input High Voltage	2.0			V	All digital inputs
V_{OL}	Output Low Voltage			0.4	V	DX, TSC,I_L = 14mA
				0.8	V	All other digital outputs, I_L = 4mA.
				0.2	V	All digital pins, I_L = 14mA
V_{OH}	Output High Voltage	VDD -0.6			V	DX, I_H = -7 mA, all other outputs, I_H = -4 mA
		VDD -0.2			V	All digital pins, I_H = -1mA
I_I	Input Current	-10		10	µA	Any digital inputs GND<V_{IN}<V_{DD}
I_{OZ}	Output Current in High-impedance State	-10		10	µA	DX
C_I	Input Capacitance			5	pF	

Note: Total current must not exceed absolute maximum ratings.

Power Dissipation

Parameter	Description	Min	Typ*	Max	Units	Test Conditions
PD2	Operating Power Dissipation 1		180	240	mW	All channels are active
PD1	Operating Power Dissipation 1		60	90	mW	Only one channel is active
PD0	Standby Power Dissipation		4	10	mW	All channels are powered down,with only MCLK present

Note: Power measurements are made at MCLK = 4.096 MHz, outputs unloaded

Analog Interface

Parameter	Description	Min	Typ	Max	Units	Test Condition
V_{IN}	Input Voltage,IIN	2.3	2.4	2.55	V	
V_{OUT1}	Output Voltage,VOUT	2.25	2.4	2.6	V	Alternating±zero μ-law PCM code applied to DR.
V_{OUT2}	Output Voltage Swing,VOUT	3.25			V_{P-P}	RL=2000Ω
R_G	Load Resistance	10			kΩ	
R_O	Output Resistance, VOUT			20	Ω	0dBm0,1020Hz PCM code applied to DR.
R_L	Load Resistance, VOUT	2000			Ω	External loading
I_I	Input Leakage Current,IIN	-1.0			μA	0.25V<VFXI<VDD-0.25V
I_Z	Output Leakage Current, VOUT	-10		10	μA	Power down
C_G	Load Capacitance			50	pF	
C_L	Load Capacitance, VOUT			100	pF	External loading

Transmission Characteristics

0dBm0 is defined as 0.6776Vrms for A-law and 0.6778 Vrms for μ-law, both for 600 Ω load. Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave; the input amplifier is set for unity gain. The digital input is a PCM bit stream equivalent to that obtained by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. The output level is sin(x)/x-corrected.

Gain

Absolute Gain

Parameter	Description	Typ	Deviation	Units	Test Condition
G_{XA}	Transmit Gain,Absolute	0.00	±0.25	dB	Signal input of 0dBm0,μ-law or A-law
G_{XA}	Recieve Gain,Absolute	0.00	±0.25	dB	Measured relative to 0 dBmo, ,μ-law or A-law,PCM input of 0 dBm0 1020Hz,RL=10kΩ

Gain Tracking

Parameter	Description	Min	Typ	Max	Units	Test Conditions
GT_X	Transmit Gain tracking					Tested by Sinusoidal Method, μ-law/A-law
	+3 dBm0 to –40 dBm0	-0.10		0.10	dB	
	-40 dBm0 to –50 dBm0	-0.25		0.50	dB	
	-50 dBm0 to –55 dBm0	-0.50		0.50	dB	
GT_R	Receive Gain tracking					Tested by Sinusoidal Method, μ-law/A-law
	+3 dBm0 to –40 dBm0	-0.10		0.10	dB	
	-40 dBm0 to –50 dBm0	-0.25		0.50	dB	
	-50 dBm0 to –55 dBm0	-0.50		0.50	dB	

Transmission Characteristics (continued)

Frequency Response

Parameter	Description	Min	Typ	Max	Units	Test Conditions
G_{XR}	Transmit Gain, Relative to G_{XA} f=50Hz f=60Hz f=300Hz to 3400Hz f=3600Hz f=4600Hz and above	 -0.15		 -40 -40 0.15 -0.1 -35	 dB dB dB dB dB	
G_{RR}	Receive Gain, Relative to G_{RA} f below 300Hz f=300Hz to 3400Hz f=3600Hz f=4600Hz and above	 -0.15		 0 0.15 -0.2 -35	 dB dB dB dB	

Group Delay

Parameter	Description	Min	Typ	Max	Units	Test Conditions
D_{XA}	Transmit Delay, Absolute *			340	µs	
D_{XR}	Transmit Delay, Relative to 1800Hz f=500Hz – 600Hz f=600Hz –1000Hz f=1000Hz – 2600Hz f=2600Hz-2800Hz			 280 150 80 280	 µs µs µs µs	
D_{RA}	Receive Delay, Absolute *			260	µs	
D_{RR}	Receive Delay, Relative to 1800Hz f=500Hz – 600Hz f=600Hz –1000Hz f=1000Hz – 2600Hz f=2600Hz-2800Hz			 50 80 120 150	 µs µs µs µs	

Note*: Minimum value in transmit and receive path.

Distortion

Parameter	Description	Min	Typ	Max	Units	Test Conditions
STDX / STDX (μ-law)	Transmit / Receive Signal to Total Distortion Ratio Input level=+3 dBm0 to –30 dBm0 Input level=-30 dBm0 to –40 dBm0 Input level=-40 dBm0 to –45 dBm0	 35.5 31 27			 dB dB dB	Sine Wave Method
STDX / STDX (A-law)	Transmit / Receive Signal to Total Distortion Ratio Input level=+3 dBm0 to –30 dBm0 Input level=-30 dBm0 to –40 dBm0 Input level=-40 dBm0 to –45 dBm0	 35.5 30 25			 dB dB dB	Sine Wave Method
SFDX	Single Frequency Distortion, Transmit			-42	dBm0	200Hz –3400Hz,0 dBm0 input,output any other single frequency≤3400Hz
SFDR	Single Frequency Distortion, Receive			-42	dBm0	200Hz –3400Hz,0 dBm0 input,output any other single frequency≤3400Hz
IMD	Intermodulation Distortion			-50	dBm0	Four Tone Method

Noise

Parameter	Description	Min	Typ	Max	Units	Test Conditions
NXC	Transmit Noise,C Message Weighted for μ-law			16	dBmC0	
NXP	Transmit Noise,P Message Weighted for A-law			-68	dBm0p	
NRC	Receive Noise,C Message Weighted for μ-law			12	dBmC0	
NRP	Receive Noise,P Message Weighted for A-law			-78	dBm0p	
NRS	Noise ,Single Frequency f=0kHz –100kHZ			-53	dBm0	VIN=0Vrms,tested at VOUT
PSRX	Power Supply Rejection Transmit f=300Hz -3.4kHz f=3.4kHz -20kHz	 40 25			 dB dB	VDD=5.0 VDC+100 mVrms
PSRR	Power Supply Rejection Receive f=300Hz -3.4kHz f=3.4kHz -20kHz	 40 25			 dB dB	PCM code is positive one LSB,VDD=5.0 VDC+100 mVrms
SOS	Spurious Out-of-Band Signals at VFRO Relative to Input PCM code applied: 4600Hz –20kHz 20kHZ- 50kHz			 -40 -30	 dB dB	0 dBm0,300Hz –3400Hz input

Transmission Characteristics (continued)

Interchannel Crosstalk

Parameter	Description	Min	Typ	Max	Units	Test Conditions
XT_{X-R}	Transmit to Receive Crosstalk		-85	-78	dB	300Hz – 3400Hz,0 dBm0 single into IIN of interfering channel.Idle PCM code into channel under test.
XT_{R-X}	Receive to Transmit Crosstalk		-85	-80	dB	300Hz – 3400Hz,0 dBm0 PCM code into interfering channel.VIN=0 Vrms for channel under test.
XT_{X-X}	Transmit to Transmit Crosstalk		-85	-78	dB	300Hz – 3400Hz,0 dBm0 PCM code into interfering channel.VIN=0 Vrms for channel under test.
XT_{R-R}	Receive to Receive Crosstalk		-85	-80	dB	300Hz – 3400Hz,0 dBm0 PCM code into interfering channel. Idle PCM code into channel under test.

Intrachannel Crosstalk

Parameter	Description	Min	Typ	Max	Units	Test Conditions
XT_{X-R}	Transmit to Receive Crosstalk		-80	-70	dB	300Hz – 3400Hz, 0 dBm0 single into VIN. Idle PCM code into DR.
XT_{R-X}	Receive to Transmit Crosstalk		-80	-70	dB	300Hz – 3400Hz, 0 dBm0 PCM code into DR.VIN=0 Vrms.

Timing Characteristics

Clock

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t1	PCLK Duty Cycle	40		60	%	PCLK=512kHz to 8.192MHz
t2	PCLK Rise and Fall Time			25	ns	PCLK=512kHz to 8.192MHz
t3	MCLK Duty Cycle	40		60	%	MCLK=2.048Hz,4.096MHz or 8.192MHz
t4	MCLK Rise and Fall Time			15	ns	MCLK=2.048Hz,4.096MHz or 8.192MHz
t5	PCLK Clock Period	244			ns	PCLK=512kHz to 8.192MHz

Transmit

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t11	Data Output Delay Time (for Short Frame Sync Mode)	5		70	ns	
t12	Data Hold Time	5		70	ns	
t13	Data Delay to High-Z	50		220 t5+70	ns	
t14	Frame sync Hold Time	50			ns	
t15	Frame sync High Setup Time	55		t5-50	ns	
t16	TSC Enable Delay Time(for Short Frame Sync Mode)	5		80	ns	
t17	TSC Disable Delay Time	50		220 t5+70	ns	
t18	Data Output Delay Time(for Long Frame Sync Mode)	5		40	ns	
t19	TSC Enable Delay Time(for Long Frame Sync Mode)	5		40	ns	
t21	Receive Data Setup Time	25			ns	
t22	Receive Data Hold Time	5			ns	

Note: Timing parameter t13 is referenced to a high-impedance state.

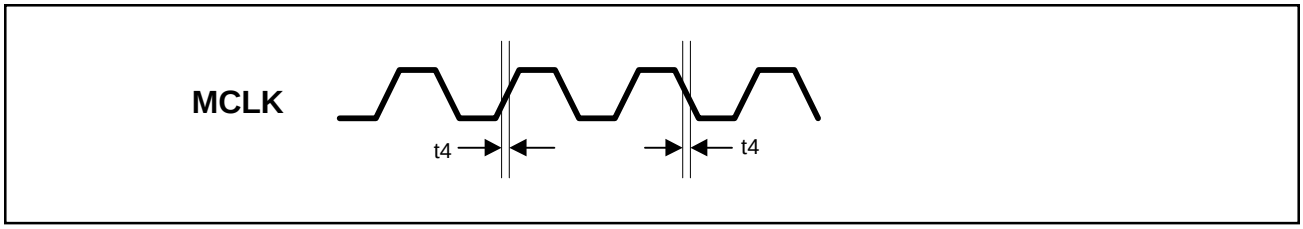


Figure 4. MCLK Timing

Timing Characteristics (continued)

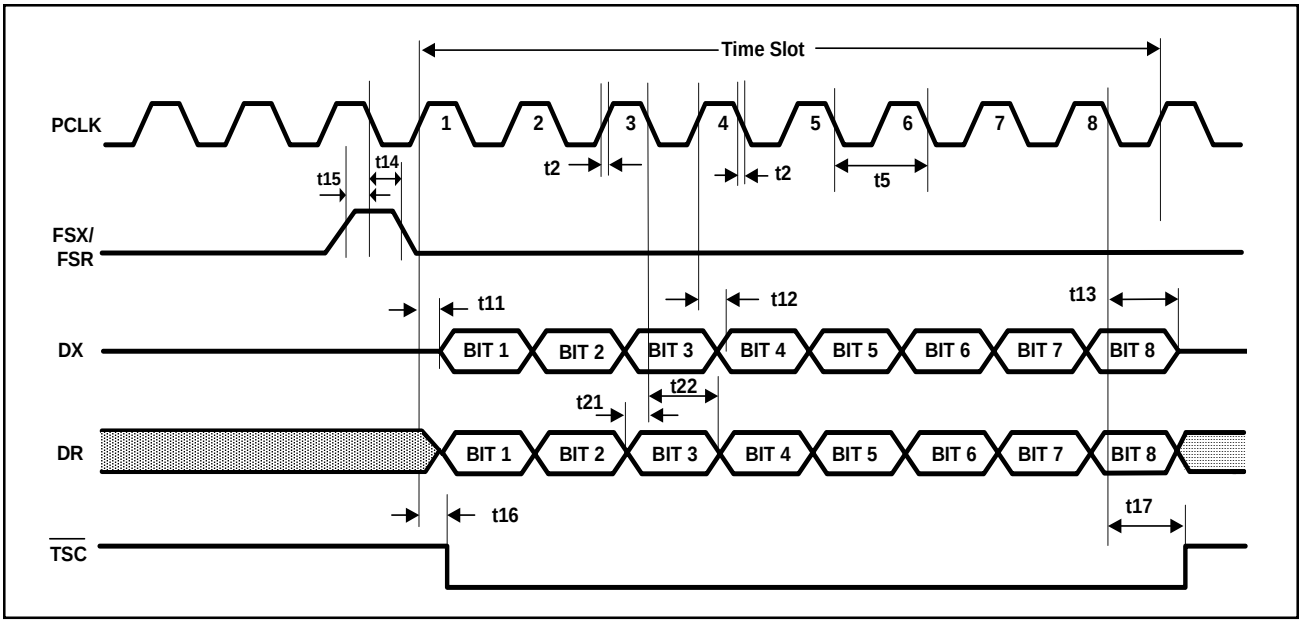


Figure 5. PCM Interface Timing for Short Frame Mode

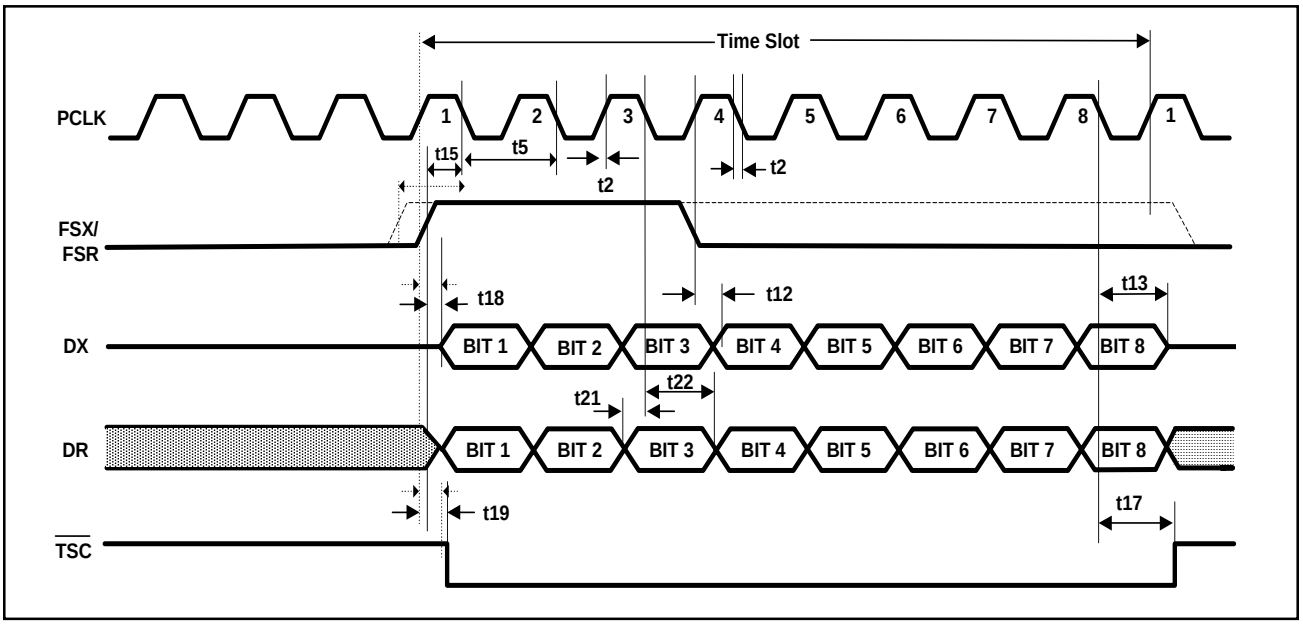
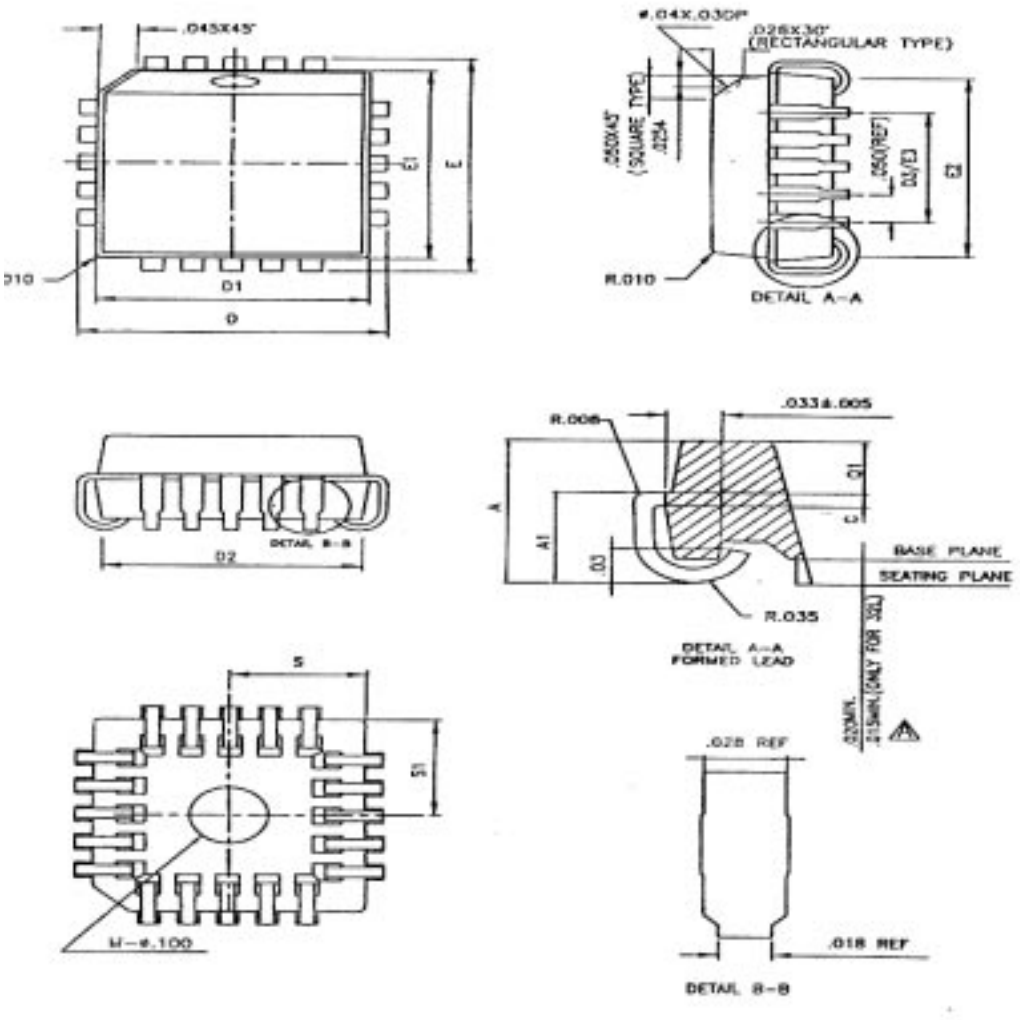


Figure 6. PCM Interface Timing for Long Frame Mode

Physical Dimensions in Inch



Package Type: 32 Pin PLCC														
UNIT: INCH														
DIM	A	A1	Q1	D	D1	D2	D3	E	E1	E2	E3	S	S1	C
Min.		0.080	0.048	0.485	0.450	0.400		0.585	0.550	0.500		0.222	0.222	
Nom.		0.085	0.050	0.490	0.453	0.410	0.300	0.590	0.553	0.510	0.400	0.227	0.227	0.010
Max.	0.140	0.090	0.052	0.495	0.456	0.420		0.595	0.556	0.520		0.232	0.232	

Figure 7. IDT821024-XL 32 Pin PLCC Package Diagram