Electrical Specifications

ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
P_D	Power Dissipation	–	–	1	W
V_{CC}	Supply Voltage	–0.5	–	7.0	V
V_I	Input Voltage	–0.5	–	V_{CC}+0.5	V
V_O	Output Voltage	–0.5	–	V_{CC}+0.5	V
T_{OP}	Operating Temperature (Ambient)	–25	–	85	°C
T_{STG}	Storage Temperature	–40	–	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded.
Functional operation should be restricted to the conditions described under Normal Operating Conditions.

NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage (5V ±10%)	4.5	5	5.5	V
T_A	Ambient Temperature	0	–	70	°C

DAC CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Typ	Max	Units
f_{MAX}	Clock Rate		–	–	85	MHz
	DAC-to-DAC Correlation	See Note 1	–	–	5	%
	DAC-to-DAC Crosstalk		–	TBD	–	dB
	Output Skew	See Note 2	–	–	2	ns
	Output Settling Time	See Note 3	–	13	–	ns
	Output Rise / Fall Time	10% to 90%	–	–	5	ns
	Comparator Sensitivity		–	50	–	mV
	Output Current	See Note 4				
	White referenced to Black		–	–	30	mA
	Black referenced to Blank		–	–	50	µA
	Blank Level		0	–	50	µA

Note: Monotonicity is guaranteed by design.
Unless otherwise specified, Analog Output Load = 50Ω, 30pF.
Note 1: Correlation is measured about the midpoint of the Red, Green, and Blue DAC outputs at full scale.
Note 2: Measured from the 50% point of the Red, Green, and Blue DAC outputs when switching from black level to full scale.
Note 3: Settling time is measured from 50% of the full scale transition to the output remaining within ±1 LSB of the final value.
Note 4: Measured with RSET = 383Ω, LOAD = 50Ω, ≤10pF.

Note: Electrical specifications contained herein are preliminary and subject to change without notice.

DC CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Typ	Max	Units
I_{CCDE}	Power Supply Current	0°C, 5.5V, 72 MHz MCLK	–	150	170	mA
I_{IL}	Input Leakage Current		–100	–	+100	µA
I_{OZ}	Output Leakage Current	High Impedance	–100	–	+100	µA
V_{IL}	Input Low Voltage	All input pins	–0.5	–	0.8	V
V_{IH}	Input High Voltage	All input pins except clocks	2.0	–	V_{CC}+0.5	V
		LCLK, (MCLK, VCLK if external)	2.8	–	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	Under max load per table below (5V)	–	–	0.5	V
V_{OH}	Output High Voltage	Under max load per table below (5V)	V_{CC}–0.5	–	–	V
ESR	Equivalent Series Resistance	XTAL In, XTAL Out Crystal Oscillator	–	–	100	Ω

DC DRIVE CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Output Pins	DC Test Conditions	Min	Units
I_{OL}	Output Low Drive	HSYNC, VSYNC, LRDY#, IRQ9, IOCS16#	$V_{OUT}=V_{OL}$, V_{CC}=5V	-12	mA
		MEMCS16#, ZWS#, WE#, OE#, CASxxx#	$V_{OUT}=V_{OL}$, V_{CC}=5V	-12	mA
		MA4:1, XA4:1	$V_{OUT}=V_{OL}$, V_{CC}=5V	-16	mA
		PCLK, RASx#, MA8:5, MA0, D31:0, AEN, LDEV#	$V_{OUT}=V_{OL}$, V_{CC}=5V	-8	mA
		MCLK	$V_{OUT}=V_{OL}$, V_{CC}=5V	-2	mA
		XTALO	$V_{OUT}=V_{OL}$, V_{CC}=5V	-1	mA
		All other outputs	$V_{OUT}=V_{OL}$, V_{CC}=5V	-4	mA
I_{OH}	Output High Drive	HSYNC, VSYNC, LRDY#, IRQ9, IOCS16#	$V_{OUT}=V_{OH}$, V_{CC}=5V	12	mA
		MEMCS16#, ZWS#, WE#, OE#, CASxxx#	$V_{OUT}=V_{OL}$, V_{CC}=5V	12	mA
		MA4:1, XA4:1	$V_{OUT}=V_{OL}$, V_{CC}=5V	16	mA
		PCLK, RASx#, MA8:5, MA0, D31:0, AEN, LDEV#	$V_{OUT}=V_{OL}$, V_{CC}=5V	8	mA
		MCLK	$V_{OUT}=V_{OL}$, V_{CC}=5V	2	mA
		XTALO	$V_{OUT}=V_{OL}$, V_{CC}=5V	1	mA
		All other outputs	$V_{OUT}=V_{OL}$, V_{CC}=5V	4	mA

AC TEST CONDITIONS

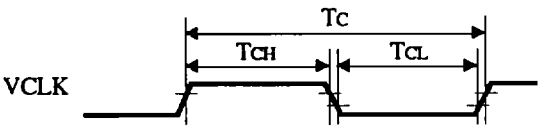
(Under Normal Operating Conditions Unless Noted Otherwise)

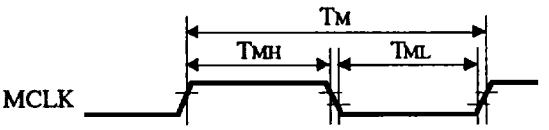
Output Pins	Output Low Voltage	Output High Voltage	Capacitive Load
All Outputs (except XTALO)	V_{OL}	2.4V	50pF

Note: Electrical specifications contained herein are preliminary and subject to change without notice.

AC TIMING CHRACTERISTICS - EXTERNAL CLOCK TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_C	CLK Period	65 MHz external VCLK	15.38	–	–	ns
T_{CH}	CLK High Time		$0.45T_C$	–	$0.55T_C$	ns
T_{CL}	CLK Low Time		$0.45T_C$	–	$0.55T_C$	ns
T_M	MCLK Period	65 MHz external MCLK	15.38	–	–	ns
T_{MH}	MCLK High Time		$0.45T_M$	–	$0.55T_M$	ns
T_{ML}	MCLK Low Time		$0.45T_M$	–	$0.55T_M$	ns
T_{RF}	Clock Rise / Fall		–	–	4	ns
T_{REF}	Reference Clock Period	Reference clock for internal synthesizer	50	69.8	100	ns

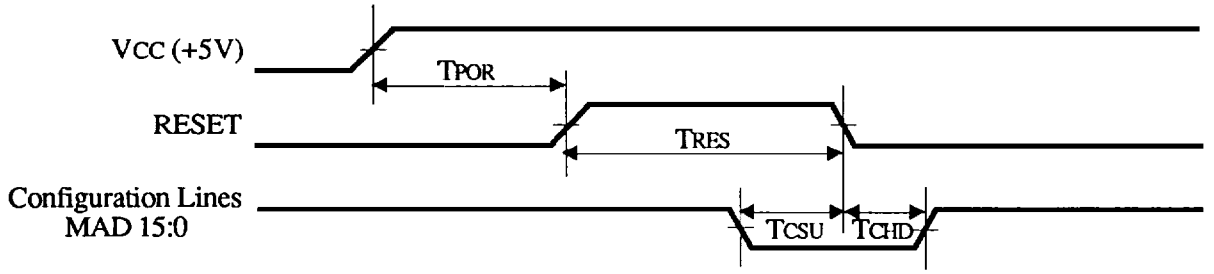




External Clock Timing

AC TIMING CHARACTERISTICS - RESET TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
TRES	RESET Pulse Width		64TM	–	–	ns
TCSU	Configuration setup time		20	–	–	ns
TCHD	Configuration hold time		5	–	–	ns
TPOR	Power on to RESET active delay		–	–	1	s



Reset Timing

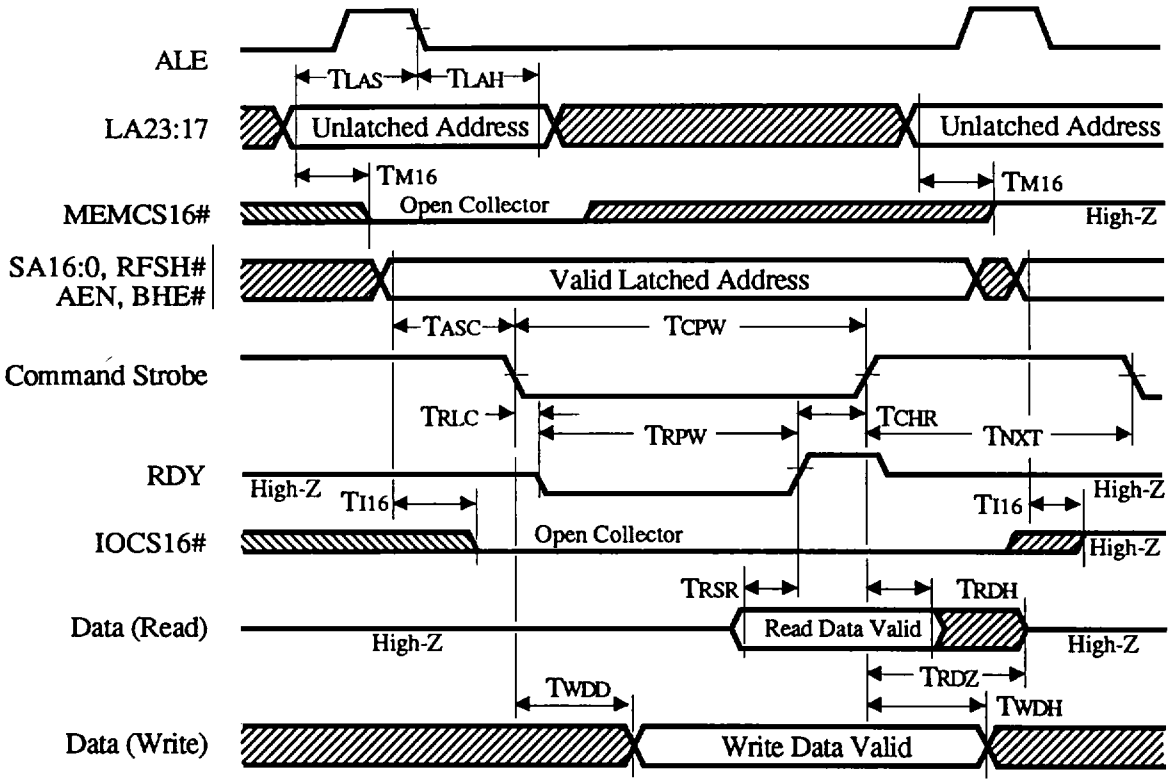
Note: Electrical specifications contained herein are preliminary and subject to change without notice.

AC TIMING CHARACTERISTICS - ISA BUS TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{ASC}	Address Setup to Command Strobe		30	–	–	ns
T_{LAS}	LA Address Setup to ALE Inactive		10	–	–	ns
T_{LAH}	LA Address Hold from ALE Inactive		10	–	–	ns
T_{CPW}	Command Strobe Pulse Width		60	–	–	ns
T_{CHR}	Command Strobe Hold from RDY high		30	–	–	ns
T_{NXT}	Command Strobe Inactive to Next Strobe	See Note 1	$3T_M$	–	–	ns
T_{M16}	MEMCS16# Delay from valid unlatched address		–	–	20	ns
T_{I16}	IOCS16# Delay from valid address		–	–	20	ns
T_{RLC}	RDY Active Low Delay from Command Strobe		–	–	30	ns
T_{RPW}	RDY Pulse Width		0	–	$100T_M$	ns
T_{RSR}	Read Data Setup to Ready		-25	–	–	ns
T_{RDH}	Read Data Hold from Command Strobe Inactive		10	–	–	ns
T_{RDZ}	Read Data Tristate from Command Strobe Inactive		–	–	40	ns
T_{WDD}	Write Data Delay from Command Strobe Active		–	–	T_{CPW}-15	ns
T_{WDH}	Write Data Hold from Command Strobe Inactive		10	–	–	ns

Note 1: This becomes $6T_M$ if host clock=MCLK/2. See XR01[3].

Note: Electrical specifications contained herein are preliminary and subject to change without notice.



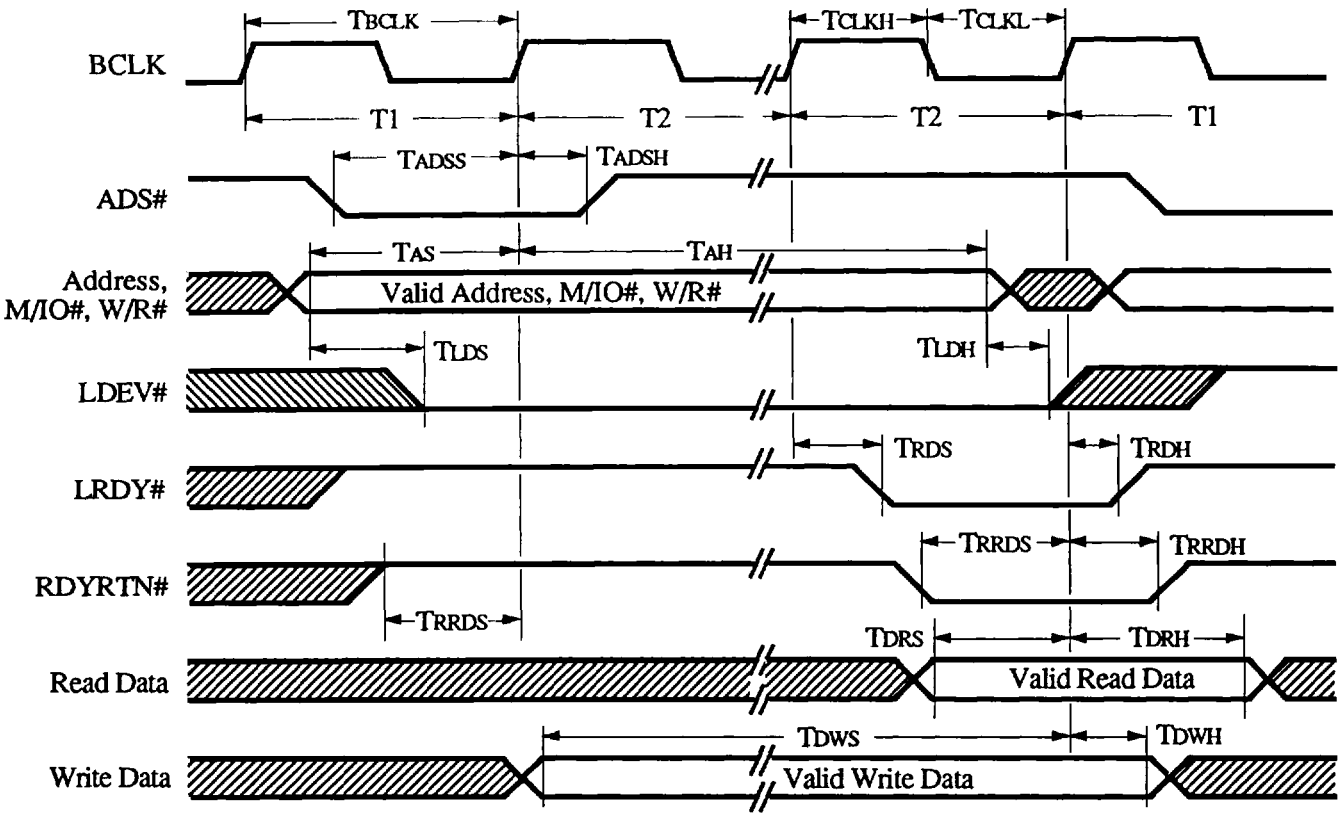
ISA Bus Cycle Timing

Note: Electrical specifications contained herein are preliminary and subject to change without notice.

DC TIMING CHARACTERISTICS - 486 LOCAL BUS TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{BCLK}	Local Bus Clock Cycle Time	50MHz	20			ns
T_{CLKL}	Local Bus Clock Low Time	Duty Cycle 45/55	9	10	11	ns
T_{CLKH}	Local Bus Clock High Time	Duty Cycle 45/55	9	10	11	ns
T_{LDS}	Delay from Address Valid to LDEV#		0	–	20	ns
T_{LDH}	LDEV# Inactive from Address Not Valid		0	–	20	ns
T_{ADSS}	ADS# Setup to BCLK rising edge		4	–	–	ns
T_{ADSH}	ADS# Hold from BCLK rising edge		5	–	–	ns
T_{AS}	Address, M/IO#, R/W# Setup to End of T1		4	–	–	ns
T_{AH}	Address, M/IO#, R/W# Hold from End of T1		T_{CLKH}+8	–	–	ns
T_{RDS}	LRDY# Setup Time from Start of final T2		18	–	–	ns
T_{RDH}	LRDY# Hold Time from End of T2		0	–	15	ns
T_{RRDS}	RDYRTN# Setup Time to End of final T2		18	–	–	ns
T_{RRDH}	RDYRTN# Hold Time from End of final T2		0	–	15	ns
T_{DRS}	Read Data Setup Time to End of final T2		18	–	–	ns
T_{DRH}	Read Data hold Time from End of final T2		0	–	15	ns
T_{DWS}	Write Data Setup Time to End of first T2		18	–	–	ns
T_{DWH}	Write Data hold Time from End of final T2		0	–	15	ns

Note: Electrical specifications contained herein are preliminary and subject to change without notice.



64300 / 301 VL Bus (486 Local Bus) Timing

Note: Electrical specifications contained herein are preliminary and subject to change without notice.

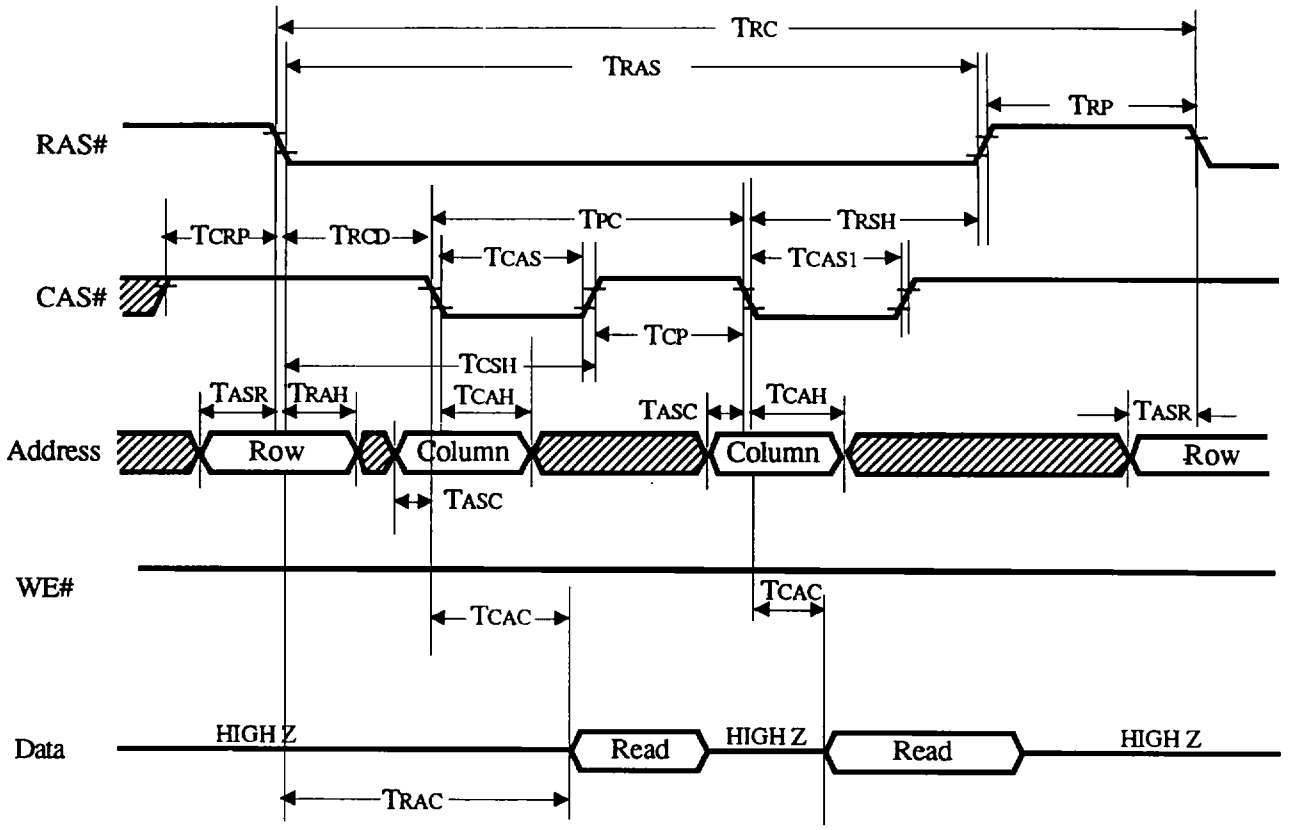
AC TIMING CHARACTERISTICS - DRAM READ/WRITE TIMING

				MCLK Frequency (MHz)			
				72.0	64.3	52.9	
				DRAM Access Time			
Symbol	Parameter	Min	Max	-6	-7	-8	Units
T_{RC}	Read/Write Cycle Time	$9T_M$-5	–	**120.0**	135.1	165.1	ns
T_{RAS}	RAS# Pulse Width (Min)	$5T_M$-5	See Note 1	64.4	72.8	89.5	ns
T_{RP}	RAS# Precharge	$4T_M$-5	–	50.6	57.3	70.6	ns
T_{CRP}	CAS# to RAS# precharge	$4T_M$-7	–	48.6	55.3	68.6	ns
TCSH	CAS# Hold from RAS#	$5T_M$-5	–	63.4	72.8	88.5	ns
T_{RCD}	RAS# to CAS# delay	$3T_M$-5		36.7	41.7	51.7	ns
			$3T_M$+5	46.7	51.7	61.7	ns
T_{RSH}	RAS# Hold from CAS#	$2T_M$-5	–	22.8	26.1	32.8	ns
T_{CP}	CAS# Precharge	T_M-3.9	–	**10.0**	11.7	15.0	ns
T_{CAS}	CAS# Pulse Width	$2T_M$-5	–	22.8	26.1	32.8	ns
T_{WP}	WE# Pulse Width	$2T_M$-5	–	22.8	26.1	32.8	ns
T_{CAS1}	CAS# Pulse Width (Fast Page Cycle)	$2T_M$-5	–	22.8	26.1	32.8	ns
T_{ASR}	Row Address Setup to RAS#	$(3T_M/2)$-15	–	5.8	8.3	13.4	ns
TASC	Column Address Setup to CAS#	$(3T_M/2)$-15	–	5.8	8.3	13.4	ns
T_{RAH}	Row Address Hold from RAS#	T_M-3.9	–	**10.0**	11.7	15.0	ns
T_{CAH}	Column Address Hold from CAS#	$(3T_M/2)$-5.8	–	**15.0**	17.5	22.6	ns
T_{CAC}	Data Access Time from CAS#	–	$2T_M$-7.8	**20.0**	23.3	30.0	ns
T_{AA}	Data Access Time from Column Address	–	$3T_M$-11.7	**30.0**	**35.0**	**45.0**	ns
T_{RAC}	Data Access time from RAS#	–	$5T_M$-5	64.4	72.8	89.5	ns
T_{DS}	Write Data Setup to CAS#	T_M-7	–	6.9	8.6	11.9	ns
T_{DH}	Write Data Hold from CAS#	$(3T_M/2)$-5.8	–	**15.0**	17.5	22.6	ns
T_{DS}	Write Data Setup to WE#	T_M-7	–	6.9	8.6	11.9	ns
T_{DH}	Write Data Hold from WE#	$(3T_M/2)$-5.8	–	**15.0**	17.5	22.6	ns
TPC	CAS# Cycle Time	$3T_M$-1.7	–	**40.0**	**45.0**	55.0	ns

Note: Parameters printed in **bold** are the limiting cases for industry standard DRAM specifications.

Note 1: Maximum RAS pulse width may be as high as 2+(256*3) memory clock cycles = $770T_M$ if the BitBlt Engine is given full memory bandwidth. This depends on other events which have higher priority including refresh cycles and display update.

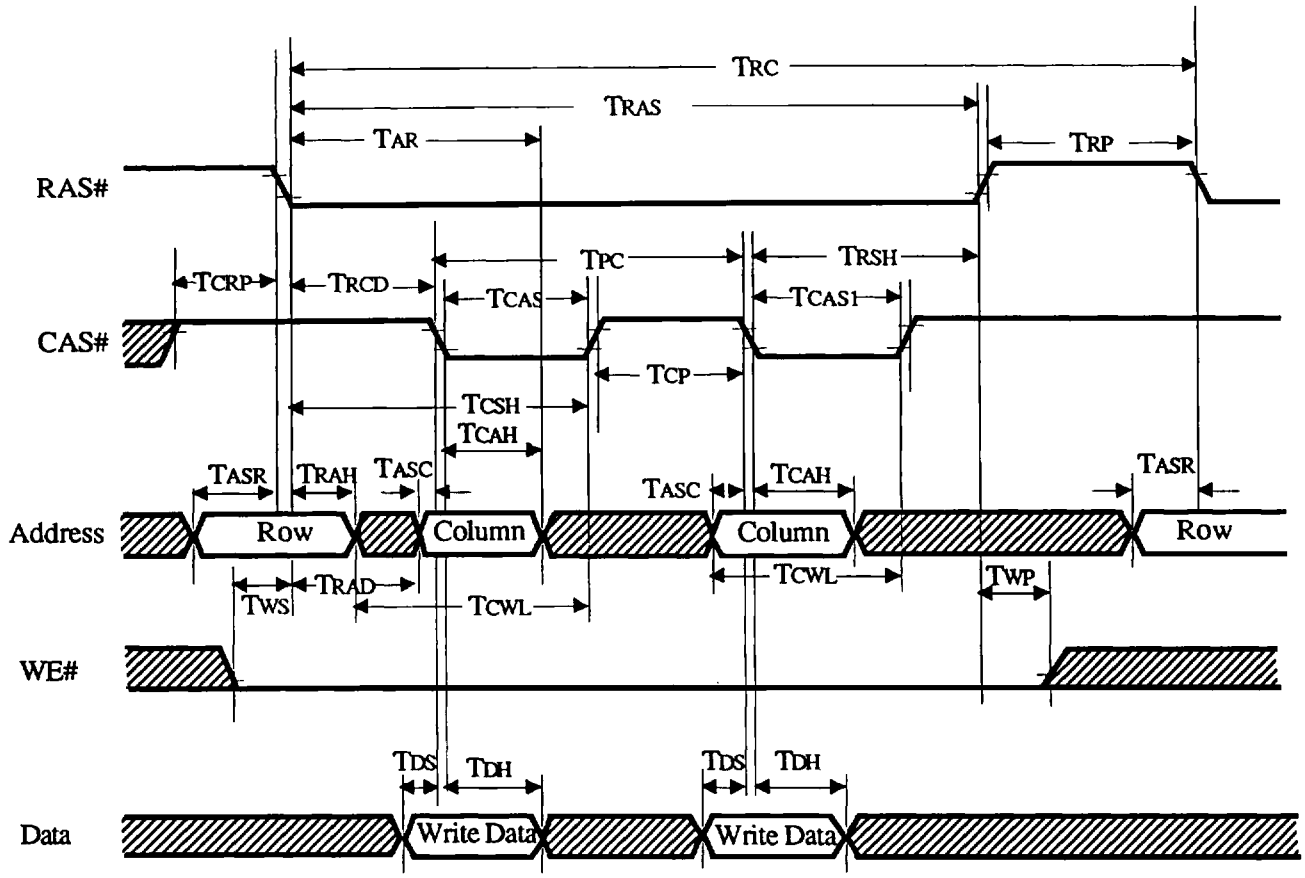
Note: Electrical specifications contained herein are preliminary and subject to change without notice.



DRAM Page Mode Read Cycle Timing

Note: The above diagram represents a typical page mode read cycle. The number of actual CAS cycles may vary.

Note: Electrical specifications contained herein are preliminary and subject to change without notice.

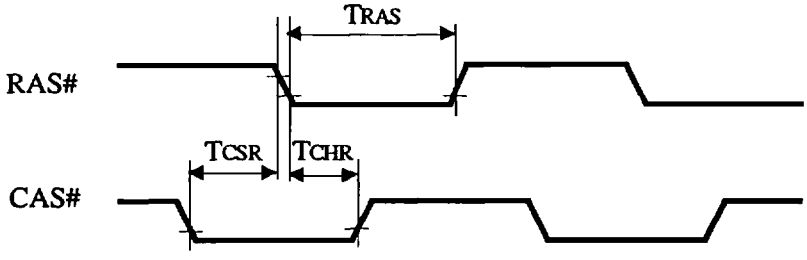


DRAM Page Mode Write Cycle Timing

Note: The above diagram represents a typical page mode write cycle.

AC TIMING CHARACTERISTICS - REFRESH TIMING

				MCLK Frequency (MHz)			
				72.0	64.3	52.9	
				DRAM Access Time			
Symbol	Parameter	Min	Max	-6	-7	-8	Units
T_{CHR}	RAS to CAS delay	$5T_M-6$	–	63.4	71.8	88.5	ns
T_{CSR}	CAS to RAS delay	$2T_M-7.5$	–	20.3	23.6	30.3	ns
TRAS	RAS pulse width	$5T_M-5$	–	64.4	72.8	89.5	ns



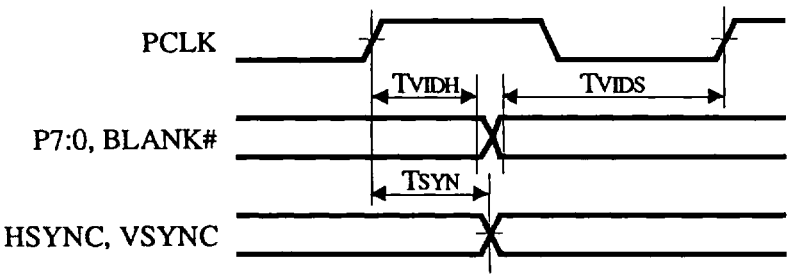
CAS-Before-RAS (CBR) DRAM Refresh Cycle Timing

Note: Electrical specifications contained herein are preliminary and subject to change without notice.

AC TIMING CHARACTERISTICS - CRT VIDEO TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{VIDS}	PCLK Setup to P7:0, BLANK#	PCLK = 45MHz	3	–	19.2	ns
T_{VIDH}	PCLK Hold from P7:0, BLANK#	PCLK = 45MHz	3	–	19.2	ns
T_{SYN}	HSYNC, VSYNC delay from PCLK		–	–	40	ns

Note: Output load on PCLK, P7:0, and BLANK# = 30pF

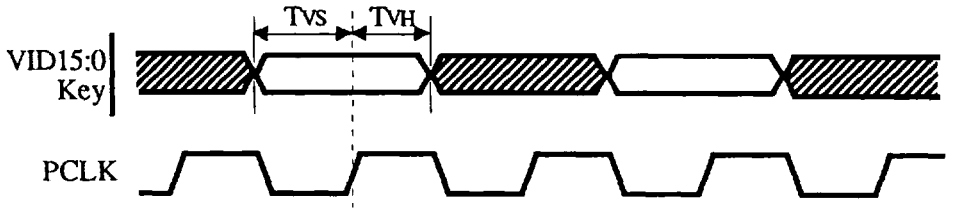


CRT Video Data and Control Signal Timing

AC TIMING CHARACTERISTICS - VIDEO OVERLAY INPUT TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{VS}	KEY, VID15:0 Setup to PCLK rising edge		15	–	–	ns
T_{VH}	KEY, VID15:0 Hold from PCLK rising edge		0	–	–	ns

Note: Output load on PCLK = 30pF



Video Overlay Timing

Note: Electrical specifications contained herein are preliminary and subject to change without notice.