# SONET/SDH/ATM CLOCK RECOVERY UNIT S3026

## FEATURES

- Complies with Bellcore and ITU-T specifications for jitter tolerance, jitter transfer and jitter generation
- On-chip high frequency PLL with internal loop filter for clock recovery
- Supports clock recovery for OC-12/STM-4 (S3026A) (622.08 Mbit/s) or OC-3/STM-1 (155.52 Mbit/s) (S3026A-1) NRZ data
- 19.44 MHz reference frequency
- Lock detect—monitors run length (S3026A only) and frequency
- 350 mW typical power dissipation
- Low-jitter PECL interface
- Maintains downstream clock in absence of data inputs
- Micro-power Bipolar technology
- 5V supply
- Available in a 20 TSSOP package

## GENERAL DESCRIPTION

The function of the S3026 clock recovery unit is to derive high speed timing signals for SONET/SDH-based equipment. The S3026 is implemented using AMCC's proven Phase Locked Loop (PLL) technology.

The S3026 receives either an OC-12/STM-4 or OC-3/STM-1 scrambled NRZ signal and recovers the clock from the data. The chip outputs a differential PECL bit clock and retimed data. Figure 1 shows a typical network application.

The S3026 utilizes an on-chip PLL which consists of a phase detector, a loop filter, and a voltage controlled oscillator (VCO). The phase detector compares the phase relationship between the VCO output and the serial data input. A loop filter converts

***Figure 1. System Block Diagram***

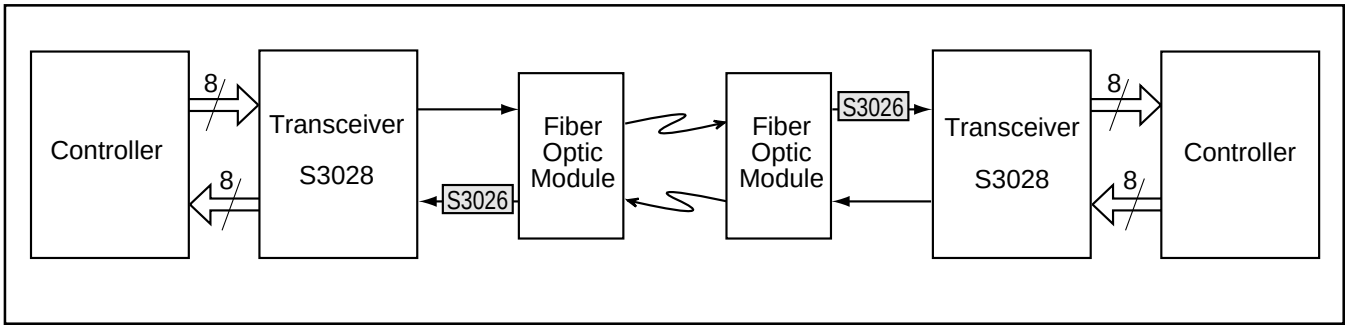
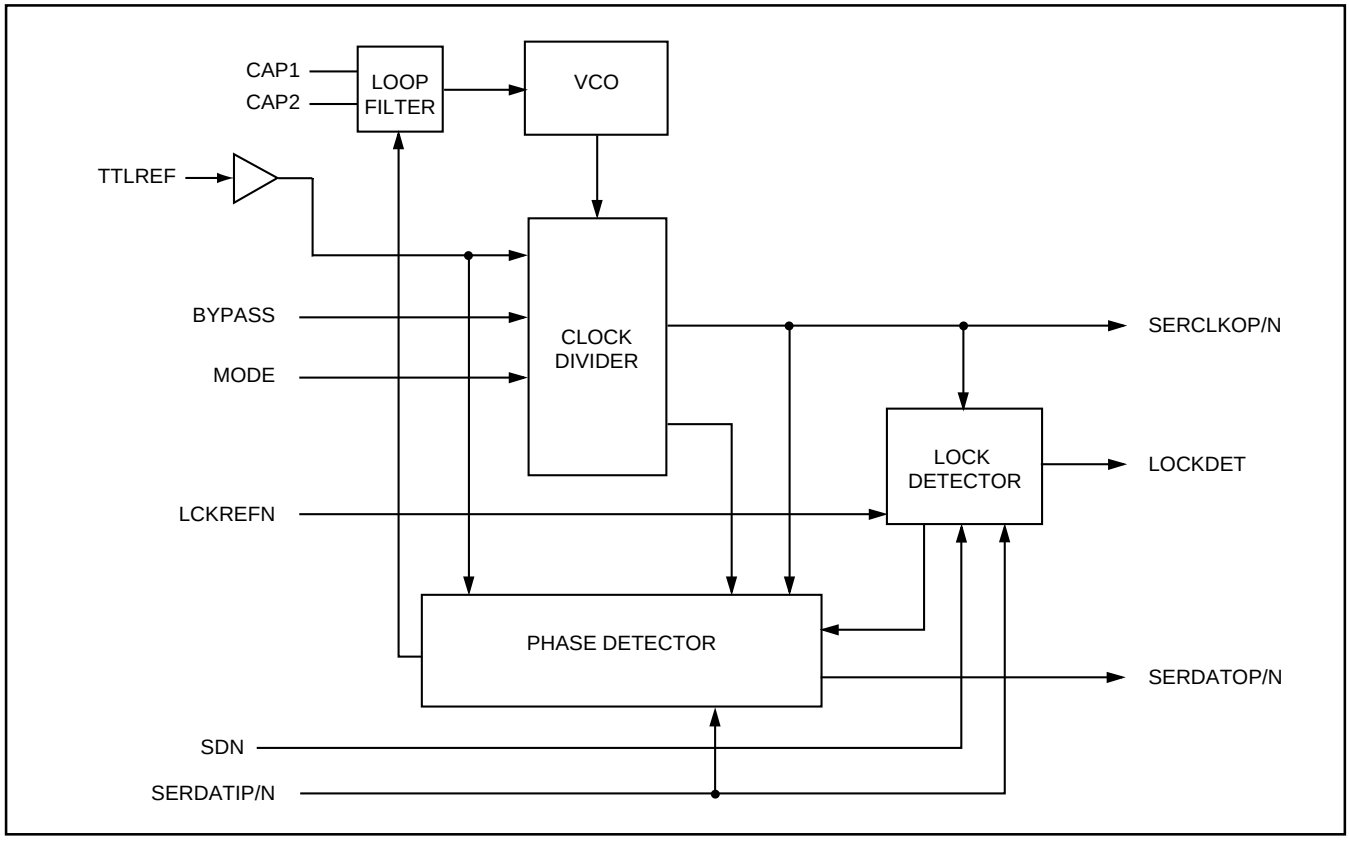


***Figure 2. Functional Block Diagram***



the phase detector output into a smooth DC voltage, and the DC voltage is input to the VCO whose frequency is varied by this voltage. A block diagram is shown in Figure 2.

## OVERVIEW

The S3026 supports clock recovery for the OC-12/STM-4 or OC-3/STM-1 data rates. Differential serial data is input to the chip at the specified rate and clock recovery is performed on the incoming data stream. An external 19.44 MHz crystal oscillator is required to minimize the PLL lock time and provide a stable output clock source in the absence of serial input data. Retimed data and clock are output from the S3026.

## CHARACTERISTICS

### Performance

The S3026 PLL complies with the jitter specifications proposed for SONET/SDH equipment defined by the T1X1.6/91-022 document, when used with differential inputs and outputs as shown in Figure 3.

### Jitter Transfer

The jitter transfer function is defined as the ratio of jitter on the output OC-N/STS-N signal to the jitter applied on the input OC-N/STS-N signal versus frequency. Jitter transfer requirements are shown in Figure 5. The measurement condition is that input sinusoidal jitter up to the mask level in Figure 4 be applied for each of the OC-N/STS-N rates.

### Input Jitter Tolerance

Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. SONET input jitter tolerance requirements are shown in Figure 4. The measurement condition is the input jitter amplitude which causes an equivalent of 1 dB power penalty.

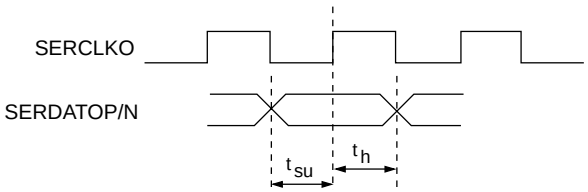
### Serial Data Output Set-up and Hold Time

The output set-up and hold times are represented by the waveforms shown in Figure 3.

### Jitter Generation

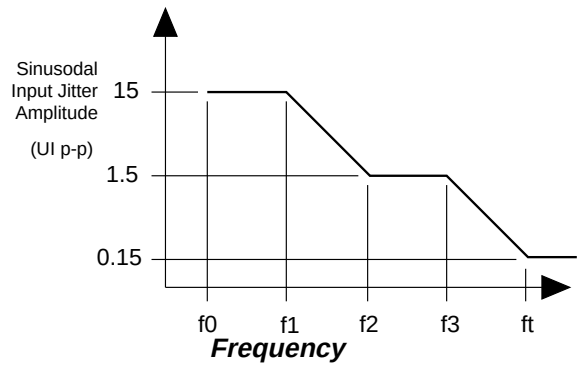
The jitter of the serial clock and serial data outputs shall not exceed 0.01 UI when a serial data input with less than 14 ps (OC-12) or 56 ps (OC-3) rms jitter is presented to the serial data inputs.

***Figure 3. Clock Output to Data Transition Delay***



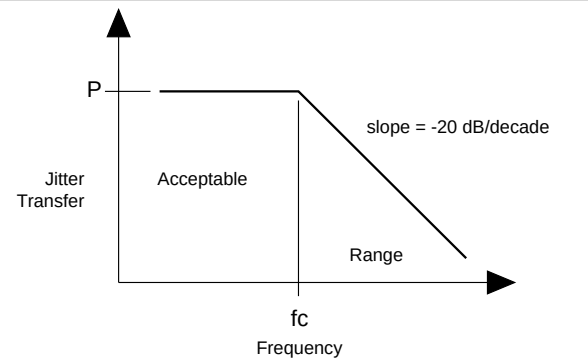

| | Output Frequency | |
|---|---|---|
| | 622.08 MHz | 155.52 MHz |
| SERDATOP/N Setup Time | 450 ps | 2.5 ns |
| SERDATOP/N Hold Time | 450 ps | 2.5 ns |

***Figure 4. Input Jitter Tolerance Specification***




| OC/STS Level | f0 (Hz) | f1 (Hz) | f2 (Hz) | f3 (kHz) | ft (kHz) |
|---|---|---|---|---|---|
| 12 | 10 | 30 | 300 | 25 | 250 |
| 3 | 10 | 30 | 300 | 6.5 | 65 |

***Figure 5. Jitter Transfer Specification***




| OC/STS Level | fc (kHz) | P (dB) |
|---|---|---|
| 12[1,2] | 500 | 0.1 |
| 3[1,2] | 130 | 0.1 |

1. Bellcore Specifications: TR-NWT-000253, Issue 2, December 1991.
2. CCITT Recommendations: G.958.

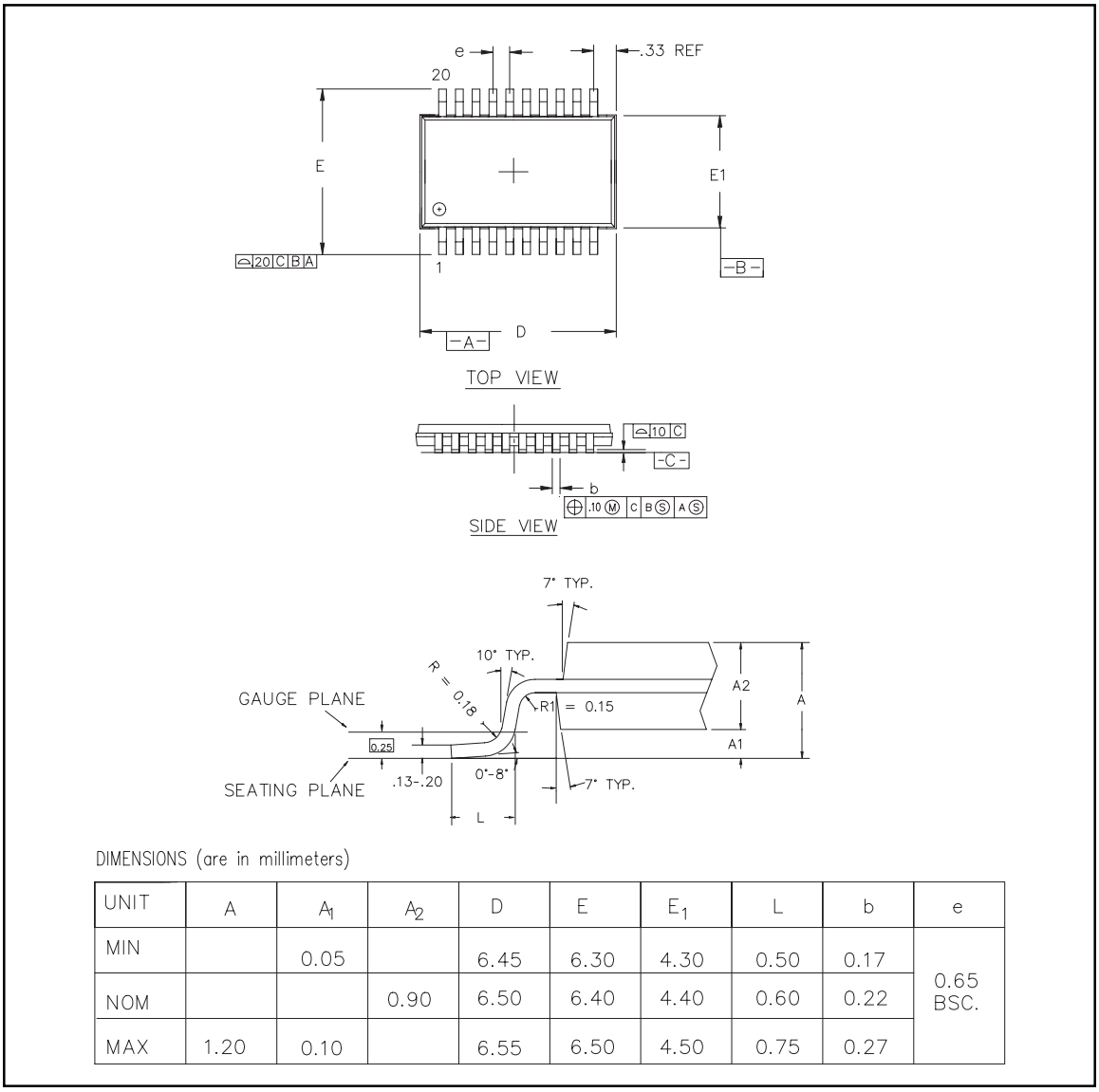
***Table 1. S3026 Pin Assignment and Descriptions***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| SERDATIP<br>SERDATIN | Diff.<br>PECL | I | 2<br>3 | Serial Data In. A clock is recovered from transitions on these inputs. |
| BYPASS | TTL | I | 16 | Bypass Enable. Active High. Used during production test to bypass the VCO in the PLL. Tie to ground for normal operation. |
| SDN | PECL | I | 15 | Signal Detect. Active Low. A single-ended 10K PECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDN is inactive, the PLL will be forced to lock to the TTLREF input and the SERDATOP/N output will be held in the logic low state. When Signal Detect (SDN) is active, data on the SERDATIP/N pins will be processed normally. |
| TTLREF | TTL | I | 7 | Reference clock input used to establish the initial operating frequency of the clock recovery PLL and also used as a standby clock in the absence of data or when LOCKDET is inactive. |
| CAP1<br>CAP2 | – | I | 18<br>17 | The loop filter capacitor and resistors are connected to these pins. The capacitor value should be 1.0µF ±10% tolerance, X7R dielectric. 16–50 V is recommended. The resistor values are 68Ω ±5%. See Figure 7. |
| LCKREFN | TTL | I | 8 | Lock to Reference. Active Low. When active, the serial clock output will be forced to lock to the TTLREF local reference input and the SERDATOP/N output will be held in the logic low state. See Table 3. |
| MODE | TTL | I | 6 | Rate select used to select the bit rate of the device. Set High to select 622.08 Mbit/s. Set Low to select 155.52 Mbit/s. |
| SERDATOP<br>SERDATON | Diff.<br>PECL | O | 14<br>13 | Serial Data Out signal that is the delayed version of the incoming data stream (SERDATI) updated on the falling edge of Serial Clock Out (SERCLKOP). |
| SERCLKOP<br>SERCLKON | Diff.<br>PECL | O | 12<br>11 | Serial Clock Out signal that is phase aligned with Serial Data Out (SERDATOP/N). (See Figure 3.) |

***Table 1. S3026 Pin Assignment and Descriptions (Continued)***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| LOCKDET | PECL | O | 5 | Lock Detect. Active High. When active, this output indicates that the PLL is locked to the serial data inputs and valid clock and data are present at the serial outputs. When inactive, it indicates that the PLL is locked to the local reference clock. The lock detect will go inactive under the following conditions:<br><br>1. If SDN is inactive.<br><br>2. If the VCO drifts away from the local reference clock by more than 1000 ppm.<br><br>3. If LCKREFN is active.<br><br>4. If the serial data inputs contain insufficient run length (100 to 800 bit times). This only applies to the S3026A for OC-12 applications.<br><br>Lock detect will return to the active state if the serial clock is within 250 ppm of the reference clock frequency. |
| DGND | GND | – | 9 | Digital Ground (0V) |
| DVCC | +5V | – | 10 | Digital Power Supply (+5V) |
| AGND | GND | – | 4, 19 | Analog Ground (0V) |
| AVCC | +5V | – | 1, 20 | Analog Power Supply (+5V) |

***Figure 6. S3026A TSSOP Package***




DIMENSIONS (are in millimeters)

| UNIT | A | $A_1$ | $A_2$ | D | E | $E_1$ | L | b | e |
|---|---|---|---|---|---|---|---|---|---|
| MIN | | 0.05 | | 6.45 | 6.30 | 4.30 | 0.50 | 0.17 | 0.65 BSC. |
| NOM | | | 0.90 | 6.50 | 6.40 | 4.40 | 0.60 | 0.22 | |
| MAX | 1.20 | 0.10 | | 6.55 | 6.50 | 4.50 | 0.75 | 0.27 | |

***Table 2. Thermal Management***

| Max Power | Θja | Θjc |
|---|---|---|
| 0.58 W | 77˚ C/W | 25˚ C/W |

***Table 3. Clock and Data Output Control***

| SDN | LCKREFN | LOCK DETECT | SERCLKOP/N | SERDATP/N |
|---|---|---|---|---|
| X | X | 0 | Active | 0 |
| X | 0 | 0 | Active | 0 |
| 1 | X | 0 | Active | 0 |
| 0 | 1 | 1 | Active | Active |

***Table 4. Absolute Maximum Ratings***

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Storage Temperature | –65 | | +150 | ˚C |
| Voltage on $V_{CC}$ with respect to GND | –0.5 | | +7.0 | V |
| Voltage on any TTL Input Pin | –0.5 | | +5.5 | V |
| Voltage on any PECL Input Pin | $V_{CC}$ –2.0 | | $V_{CC}$ | V |
| TTL Output Sink Current | | | 20 | mA |
| TTL Output Source Current | | | 10 | mA |
| High Speed PECL Output Source Current | | | 50 | mA |
| ESD Sensitivity [1] | Under 500 | | | V |

1. Human body model.

***Table 5. Recommended Operating Conditions***

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Ambient Temperature Under Bias (Industrial) | –40 | | +85 | ˚C |
| Ambient Temperature Under Bias (Commercial) | 0 | | +70 | ˚C |
| Voltage on $V_{CC}$ with respect to GND | 4.75 | 5.0 | 5.25 | V |
| Voltage on any TTL Input Pin | 0.0 | | $V_{CC}$ | V |
| Voltage on any PECL Input Pin | $V_{CC}$ –2 | | $V_{CC}$ | V |
| PECL Output Source Current (50Ω to $V_{CC}$ –2V) | | 14 | 25 | mA |
| ICC Supply Current | | 80 | 110 | mA |

***Table 6. Performance Specifications***

| Parameter | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|
| Nominal VCO Center Frequency | | 622.08 | | MHz | |
| Reference Clock Frequency Tolerance Clock Recovery[1] | -250 | | +250 | ppm | |
| OC-12/STS-12 Capture Range | | ±500 | | ppm | With respect to fixed reference frequency |
| Clock Output Duty Cycle | 45 | | 55 | % of UI | Minimum transition density of 20% |
| Acquisition Lock Time[1] OC-12/STS-12 | | | 16 | µsec | With device already powered up and valid REFCLK. |
| PECL Output Rise & Fall Times | | | 600 | ps | 10% to 90%, 50Ω to -2V equivalent load, 5 pF cap |
| SERCLKOP/N Jitter Generation | | 0.005 | 0.01 | UI | With less than 14 ps rms jitter on SERDATIP/N data inputs |
| OC-12/STS-12 Jitter Tolerance[1] | 0.5 | | | UI | Sinusoidal input jitter. Amplitude on SERDATIP/N data inputs from 250 kHz to 5 MHz. |

1. Guaranteed but not tested.

### *Table 7. TTL Input/Output DC Characteristics*[1]

($T_A$ = -40°C to +85°C, $V_{CC}$ = 5 V ±5%)

| Symbol | Parameters | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IL}$[1] | Input Low Voltage | | | 0.8 | V | Guaranteed input Low voltage for all inputs |
| $V_{IH}$[1] | Input High Voltage | 2.0 | | | V | Guaranteed input High voltage for all inputs |
| $I_{IL}$ | Input Low Current | –400.0 | | | µA | $V_{CC}$ = MAX, $V_{IN}$ = 0.5V |
| $I_{IH}$ | Input High Current | | | 50.0 | µA | $V_{CC}$ = MAX, $V_{IN}$ = 2.7V |
| $I_I$ | Input High Current at Max $V_{CC}$ | | | 1.0 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 5.25V |
| $I_{OS}$ | Output Short Circuit Current | –100.0 | | –25.0 | mA | $V_{CC}$ = MAX, $V_{OUT}$ = 0.5V |
| $V_{IK}$ | Input Clamp Diode Voltage | –1.2 | | | V | $V_{CC}$ = MIN, $I_{IN}$ = 18.0mA |
| $V_{OL}$ | TTL Output Low Voltage | | | 0.5 | V | $V_{CC}$ = MIN, $I_{OL}$ = 8mA |
| $V_{OH}$ | TTL Output High Voltage | 2.4 | | | V | $V_{CC}$ = MIN, IOH = –1.0mA |

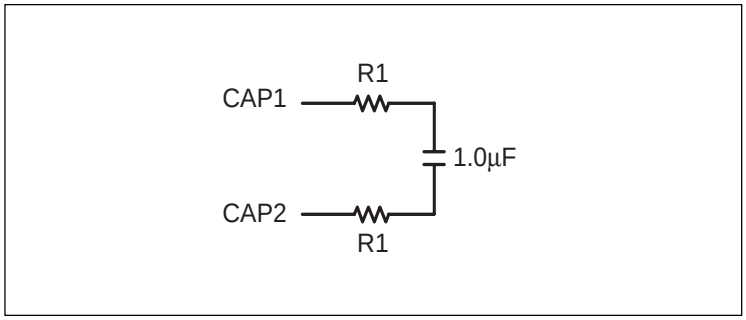
1. These input levels provide a zero–noise immunity and should only be tested in a static, noise-free environment.

### *Table 8. PECL Input/Output DC Characteristics*

($T_A$ = -40°C to +85°C, $V_{CC}$ = 5 V ±5%)

| Symbol | Parameters | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | $V_{CC}$ –2.000 | | $V_{CC}$ –1.441 | V | Guaranteed input Low voltage for single-ended inputs |
| $V_{IH}$ | Input High Voltage | $V_{CC}$ –1.225 | | $V_{CC}$ –0.570 | V | Guaranteed input High voltage for single-ended inputs |
| $V_{IL}$ | Input Low Voltage | $V_{CC}$ –2.000 | | $V_{CC}$ –0.700 | V | Guaranteed input Low voltage for differential inputs |
| $V_{IH}$ | Input High Voltage | $V_{CC}$ –1.750 | | $V_{CC}$ –0.450 | V | Guaranteed input High voltage for differential inputs |
| $V_{ID}$ | Input Differential Voltage | 0.250 | 0.500 | 1.400 | V | Differential input voltage |
| $I_{IH}$ | Input High Current | –0.500 | | 20.000 | µA | $V_{ID}$ = 500mV |
| $I_{IL}$ | Input Low Current | –0.500 | | 20.000 | µA | $V_{ID}$ = 500mV |
| $V_{OL}$ | Output Low Voltage | $V_{CC}$ –2.000 | | $V_{CC}$ –1.500 | V | 50Ω termination to $V_{CC}$ –2V |
| $V_{OH}$ | Output High Voltage | $V_{CC}$ –1.110 | | $V_{CC}$ –0.670 | V | 50Ω termination to $V_{CC}$ –2V |
| $V_{OD}$ | Output Differential Voltage | 0.390 | | 1.330 | V | Differential output voltage |

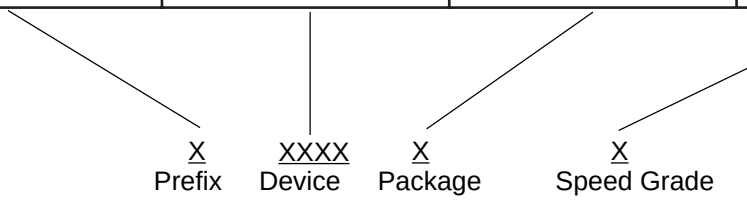
***Figure 7. External Loop Filter***




R1 = 68Ω for 622.08 Mbps
R1 = 84Ω for 155.52 Mbps

***Ordering Information***

| PREFIX | DEVICE | PACKAGE | SPEED GRADE |
|---|---|---|---|
| S – Integrated Circuit | 3026 | A – 20 TSSOP | 1– 155 Mbps<br>Blank – 622 Mbps |

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