LXP2180A

T1 ESF Framer/Formatter

General Description

The LXP2180A is one of a family of Level One T1 interface solutions. It is compatible with the LXT300 series transceivers and LXP600 series clock adapters. The device interfaces to the DS1 1.544 Mbps digital trunk. A pin compatible drop-in replacement for the Dallas DS2180A, the LXP2180A provides all formatting necessary for transmission on the T1 link. It supports both 193S and 193E superframe standards and provides clear channel capability through appropriate zero suppression and signaling modes.

The transmit framer/formatter circuits generate appropriate framing bits, insert robbed bit signaling, supervise zero suppression, generate alarms and provide output clocks for data conditioning and decoding. The receive and synchronizer circuits establish frame and multiframe boundaries, extract signaling data and report alarms and signaling formats. Control functions allow both stand-alone Hardware mode operation and Host mode operation for use with a microprocessor/microcontroller.

The LXP2180A is a monolithic CMOS device which requires only a single +5V power supply.

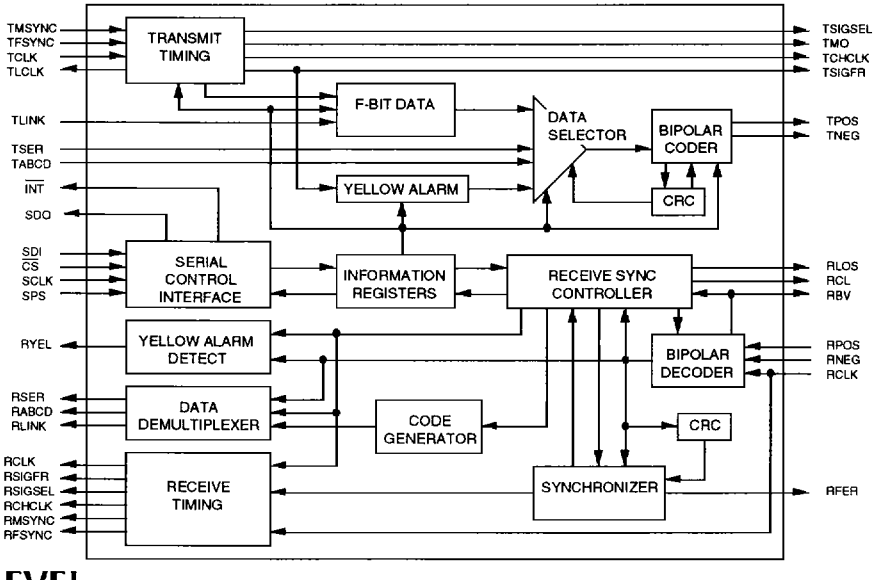
Applications

- DS1/ESF digital trunk interfaces
- Computer to PBX interfaces (DMI and CPI)
- High speed computer to computer data links
- Digital cross-connect interface

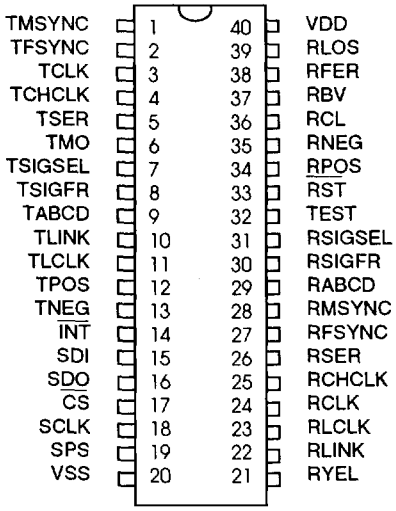
Features

- Drop-in replacement for the DS2180A
- Single chip DS1 rate framer/formatter
- Supports common framing standards
  - 12 frames/superframe "193S"
  - 24 frames/superframe "193E"
- Three zero suppression modes
  - B7 stuffing
  - B8ZS
  - Transparent
- Simple serial interface for configuration, control and status monitoring in Host mode
- Hardware mode for stand-alone applications requires no host processor
- Compatible with LXT300 series transceivers
- Selectable 0, 2, 4, 16 state robbed bit signaling modes
- Allows mix of "clear" and "non-clear" DS0 channels on same DS1 link
- Alarm generation and detection
- Receive error detection and counting for transmission performance monitoring
- +5V supply, low-power CMOS technology
- Available in 40-pin plastic DIP and 44-pin PLCC

Figure 1: Block Diagram



40-Pin DIP



44-Pin PLCC

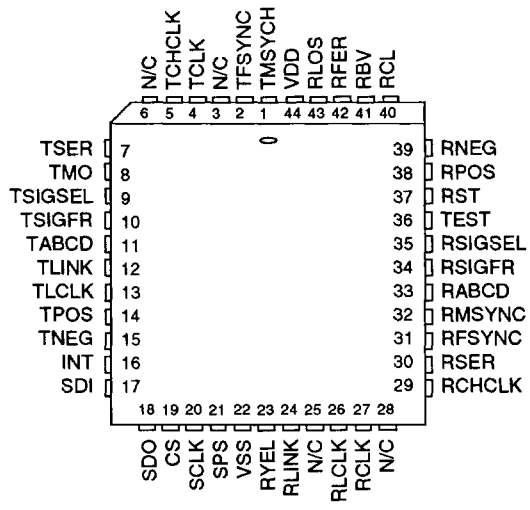


Table 1: Transmit Pin Descriptions

Pin# DIP	Pin# PLCC	Sym	I/O	Name	Description
1	1	TMSYNC	I	Transmit Multi-frame Sync	Transmit Multiframe Sync may be pulsed high at multiframe boundaries to reinforce multiframe alignment, or tied low, which allows internal multiframe counter to free run.
2	2	TFSYNC	I	Transmit Frame Sync Channel B2	Transmit Frame Sync. Rising edge identifies frame boundary. May be pulsed every frame to reinforce internal frame counter, or tied low to allow TMSYNC to establish frame/multiframe alignment.
3	4	TCLK	I	Transmit Clock	1.544 MHz primary clock.
4	5	TCHCLK	O	Transmit Channel Clock	192 kHz clock which identifies time slot (channel) boundaries. Useful for parallel to serial conversion of channel data.
5	7	TSER	I	Transmit Serial Data	NRZ data input, sampled on falling edge of TCLK.
6	8	TMO	O	Transmit Multi-frame Out	Output of internal multiframe counter, indicates multiframe boundaries. 50% duty cycle.
7	9	TSIGSEL	O	Transmit Signaling Select	In 193E framing mode, this output is a 0.667 kHz clock which identifies signaling frames A and C. In 193S framing, it's a 1.33 kHz clock.
8	10	TSIGFR	O	Transmit Signaling Frame	High during signaling frames, low otherwise.
9	11	TABCD	I	Transmit ABCD Signaling	When enabled via TCR.4, sampled during channel LSB time in signaling frames on falling edge of TCLK.

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Table 1: Transmit Pin Descriptions continued

Pin# DIP	Pin# PLCC	Sym	I/O	Name	Description
10	12	TLINK	I	Transmit Data Link	Sampled during F-bit time (falling edge of TCLK) of odd frames for insertion into the outgoing data stream (193E-FDL insertion). Sampled during the F-bit time of even frames for insertion into the outgoing data (193S-External S-Bit insertion).
11	13	TLCLK	O	Transmit Link Clock	Transmit Link Clock is a 4 kHz demand clock for TLINK input.
12	14	TPOS	O	Transmit Positive and	Transmit Bipolar Data Outputs. Updated on rising edge of TCLK.
13	15	TNEG	O	Negative Data	

Table 2: Port Pin Description

Pin# DIP	Pin# PLCC	Sym	I/O	Name	Description
14	16	$\overline{INT}$ [1]	O	Receive Alarm Interrupt	In Host mode, an active low, open drain output which flags the host controller during alarm conditions.
15	17	SDI[1]	I	Serial Data Input	Serial port input data for on-board registers. Sampled on rising edge of SCLK (Host mode).
16	18	SDO[1]	O	Serial Data Output	Serial output of control and status information from on-board registers. Updated on falling edge of SCLK, tri-stated during serial port write or when $\overline{CS}$ is high (Host mode).
17	19	$\overline{CS}$[1]	I	Chip Select	Must be low to write or read the serial port registers (Host mode).
18	20	SCLK[1]	I	Serial Data Clock	Used to read or write the serial port registers (Host mode).
19	21	SPS	I	Serial Port Select	Tie to VDD to select serial port (Host mode). Tie to VSS to select the Hardware mode.

1. Multifunction pins; see Hardware mode description.

Table 3: Power and Test Pin Descriptions

Pin# DIP	Pin# PLCC	Sym	I/O	Name	Description
20	22	VSS	–	Signal Ground	0.0 V signal ground.
32	36	TEST	I	Test Mode	Tie to VSS for normal operation.
40	44	VDD	–	Positive Supply	+5V power supply input.

Table 4: Receive Pin Descriptions

Pin# DIP	Pin# PLCC	Sym	I/O	Name	Description
21	23	RYEL	O	Receive Yellow Alarm	Transitions high when yellow alarm detected, goes low when alarm clears.
22	24	RLINK	O	Receive Link Data	Updated with extracted FDL data one RCLK before start of odd frames (193E) and held until next update. Updated with extracted S-bit data one RCLK before start of even frames (193S) and held until next update.
23	26	RLCLK	O	Receive Link Clock	4 kHz demand clock for RLINK.
24	27	RCLK	I	Receive Clock	1.544 MHz primary clock.
25	29	RCHCLK	O	Receive Channel Clock	192 kHz clock, identifies time slot (channel) boundaries.
26	30	RSER	O	Receive Serial Data	Received NRZ serial data, updated on rising edge of RCLK.
27	31	RFSYNC	O	Receive Frame Sync	Extracted 8 kHz clock, one RCLK wide, indicates F-bit position in each frame.
28	32	RMSYNC	O	Receive Multi-frame Sync	Extracted multiframe sync; edge indicates start of multiframe. 50% duty cycle.
29	33	RABCD	O	Receive ABCD Signaling	Extracted signaling data output, valid for each channel time in signaling frames. In non-signaling frames, RABCD outputs the LSB of each channel word.
30	34	RSIGFR	O	Receive Signaling Frame	High during signaling frames, low during re-sync and non-signaling frames.
31	35	RSIGSEL	O	Receive Signaling Select	In 193E framing a .667 kHz clock which identifies signaling frames A and C. A 1.33 kHz clock in 193S framing.
33	37	$\overline{\text{RST}}$	I	Reset	High-low transition clears all internal registers and resets receive side counters. High-low-high transition initiates a receive resync.
34	38	RPOS	I	Receive Positive and Negative Inputs	Receive Bipolar Data Inputs are sampled on the falling edge of RCLK. Tie together to receive NRZ data and disable bipolar violation monitoring circuitry.
35	39	RNEG	I		
36	40	RCL	O	Receive Carrier Loss	Receive Carrier Loss goes high if 32 consecutive "0's" appear at RPOS and RNEG. Goes low after next "1."
37	41	RBV	O	Receive Bipolar Violation	Receive Bipolar Violation goes high during accused bit tie at RSER if bipolar violation detected, low otherwise.
38	42	RFER	O	Receive Frame Error	Receive Frame Error. High during F-bit time when FT or FS errors occur (193S) or when FPS or CRC errors occur (193E). Low during resync.
39	43	RLOS	O	Receive Loss of Sync	RLOS indicates sync status. Goes high when internal resync is in progress, low otherwise.

Table 5: Register Summary

Register	Address	Side[1]	Description / Function
RSR	0000	R[2]	Receive Status Register. Reports all receive alarm conditions.
RIMR	0001	R	Receive Interrupt Mask Register. Allows masking of individual alarm generated interrupts.
BVCR	0010	R	Bipolar Violation Count Register. An 8-bit presetable counter which records individual bipolar violations.
ECR	0011	R	Error Count Register. Two independent 4-bit counters which record OOF occurrences, and individual frame bit or CRC errors.
CCR[3]	0100	T/R	Common Control Register. Selects device operating characteristics common to receive and transmit sides.
RCR[3]	0101	R	Receive Control Register. Programs device operating characteristics unique to the receive side.
TCR[3]	0110	T	Transmit Control Register. Selects additional transmit side modes.
TIR1 TIR2 TIR3	0111 1000 1001	T T T	Transmit Idle Registers. Designate which outgoing channels are to be substituted with idle code.
TTR1 TTR2 TTR3	1010 1011 1100	T T T	Transmit Transparent Registers. Designate which outgoing channels are to be treated transparently. (No robbed bit signaling or bit 7 zero insertion.)
RMR1 RMR2 RMR3	1101 1110 1111	R R R	Receive Mark Registers. Designate which incoming channels are to be replaced with idle or digital milliwatt codes (under control of RCR).

Notes

[1] Transmit or Receive side register.

[2] RSR is a read-only register. All other registers are read/write.

[3] Reserved bit locations in control registers should be programmed to 0 to maintain compatibility with future transceiver products.

Operating Modes

In the Host mode, pins 14 through 18 comprise a microprocessor/microcontroller compatible serial port which can be used for device configuration, control and status monitoring.

In the Hardware mode no offboard processor is required. Pins 14 through 18 are re-configured into "Hardwired" select pins. Features such as selective "clear" DS0 channels, insertion of idle code and alteration of sync algorithm are unavailable in the Hardware mode.

Host Mode

Serial Port Interface

Pins 14 through 18 of the LXP2180A serve as a microprocessor/microcontroller compatible serial port. Sixteen onboard registers allow the user to update operational characteristics and monitor device status via a host controller, minimizing hardware interfaces. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous reads and/or writes by the host.

Address/Command Byte

Reading or writing the control, configuration or status registers requires writing one address/command byte (ACB) prior to transferring register data. As shown in Figure 2, the first bit written (LSB) of the address/command word specifies register read or write. The following 4-bit nibble identifies the register address. The next two bits are reserved and must be set to zero for proper operation. The last bit of the address/command word enables burst mode when set; the burst mode causes all registers to be consecutively written or read. Data is written to and read from the transceiver LSB first.

Chip Select and Clock Control

All data transfers are initiated by driving the $\overline{CS}$ input low. Input data is latched on the rising edge of SCLK and must be valid during the previous low period of SCLK to prevent momentary corruption of register data during writes. Data is output on the falling edge of SCLK and held to the next falling edge. All data transfers are terminated if the $\overline{CS}$ input transitions high. Port control logic is disabled and SDO tristated when $\overline{CS}$ is high.

Data I/O

Data I/O timing is shown in Figure 3. Following the eight SCLK cycles that input an address/command byte to write, a data byte is strobed into the addressed register on the rising edges of the next eight SCLK cycles. Following an address/command word to read, contents of the selected register are output on the falling edges of the next eight SCLK cycles. The SDO pin is tri-stated during device write, and may be tied to SDI in applications where the host processor has a bidirectional I/O pin.

Burst Mode

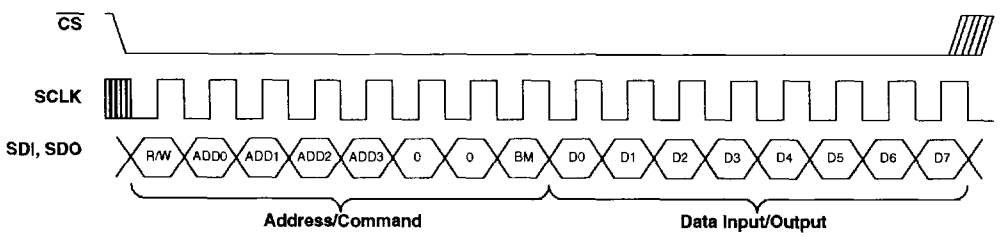
The burst mode allows all on-board registers to be consecutively read or written by the host processor. A burst read is used to poll all registers; RSR contents will be unaffected. This feature minimizes device initialization time on power-up or system reset. Burst mode is initiated when ACB.7 is set and the address nibble is 0000. Burst is terminated by low-high transition on $\overline{CS}$.

Figure 2: Address/Command Byte (ACB)

(MSB)							(LSB)
BM	-	-	ADD3	ADD2	ADD1	ADD0	R/W

Symbol	Position	Name And Description
BM	ACB.7	Burst Mode. If set (and ACB.1 through ACB.4 = 0) burst read or write is enabled.
-	ACB.6	Reserved. Must be set to 0 for proper operation.
-	ACB.5	Reserved. Must be set to 0 for proper operation.
ADD3	ACB.4	MSB of register address.
ADD0	ACB.1	LSB of register address.
R/$\overline{W}$	ACB.0	Read/Write Select. 0 = write addressed register. 1 = read addressed register.

Figure 3: Serial Port Read/Write



1. SDI sampled on rising edge of SCLK.
2. SDO updated on falling edge of SCLK.

Common Control Register

The Common Control Register (CCR) is shown in Figure 4.

Loopback

Enabling loopback will typically induce an Out Of Frame (OOF) condition. If appropriate bits are set in the receive control register (RCR), the receiver will resync to the looped transmit frame alignment. During the looped condition, the transmit outputs (TPOS, TNEG) will transmit all "1's" unframed. All operating modes (B8ZS, alarm, signaling, etc.) except for blue alarm transmission are available in loopback.

Bit Seven Stuffing

Existing systems meet ones density requirements by forcing bit 7 of all zero channels to 1. Bit 7 stuffing is globally enabled by asserting bit CCR.1, and may be disabled on an individual channel basis by setting appropriate bits in TTR1 - TTR3.

B8ZS

The LXP2180A supports existing and emerging zero suppression formats. Selection of B8ZS coding maintains system ones density requirements without disturbing data integrity as required in emerging clear channel applications. B8ZS coding replaces eight consecutive outgoing zeros with a B8ZS code word. Any received B8ZS code word is replaced with all zeros.

Figure 4: Common Control Register

(MSB)							(LSB)
–	FRSR2	EYELMD	FM	SYELMD	B8ZS	B7	LPBK

Symbol	Position	Name And Description
–	CCR.7	Reserved. Must be set to 0 for proper operation.
FRSR2	CCR.6	Function of Rec Status Register 2. 0 = Detected B8ZS code words reported at RSR.2. 1 = Change of Frame Alignment (COFA) reported at RSR.2 when last resync resulted in change of frame or multiframe alignment.
EYELMD	CCR.5	193E Yellow Mode Select. 0 = Yellow alarm is a repeating pattern set of 00 hex and FF hex. 1 = Yellow alarm is a "0" in the bit 2 position of all channels.
FM	CCR.4	Frame Mode Select. 0 = D4 (193S, 12 frames/superframe). 1 = Extended (193E, 24 frames/superframe)
SYELMD	CCR.3	193S Yellow Mode Select. Determines yellow alarm type to be transmitted and detected while in 193S framing. If set, yellow alarms are a "1" in the S-bit position of frame 12. If cleared, yellow alarm is a "0" in bit 2 of all channels. Does not affect 193E yellow alarm operation.
B8ZS	CCR.2	Bipolar Eight Zero Suppression. 0 = No B8ZS. 1 = B8ZS enabled.
B7	CCR.1	Bit Seven Zero Suppression. If CCR.1 = 1, channels with an all zero content will be transmitted with bit 7 forced to "1." If CCR.1 = 0, no bit 7 stuffing occurs.
LPBK	CCR.0	Loopback. When set, the device internally loops output transmit data into the incoming receive data buffers and TCLK is internally substituted for RCLK.

Transmit Control Register

The Transmit Control Register (TCR) is shown in Figure 5.

Transmit Blue Alarm

The blue alarm, also known as the Alarm Indication Signal (AIS), is an unframed, all 1's sequence enabled by asserting TCR.1. Blue alarm overrides all other transmit data patterns and is disabled by clearing TCR.1. Use of the TIR registers allows an unframed, all 1's alarm transmission if required by the network.

Transmit Yellow Alarm

In 193E framing, a yellow alarm is a repeating pattern set of FF (Hex) and 00 (Hex) on the 4 kHz facility data link (FDL). In 193S framing, the yellow alarm format is dependent on the state of bit CCR.3. In all modes, yellow alarm is enabled by asserting TCR.0 and disabled by clearing TCR.0.

Transmit Signaling

When enabled via TCR.4, channel signaling is inserted in frames 6 and 12 (193S); or 6, 12, 18 and 24 (193E) in the 8th bit position of every channel word. Signaling data is sampled at TABCD on the falling edge of TCLK during bit 8 of each input word during signaling frames. Logical combination of clocks TMO, TSIGFR and TSIGSEL allow external multiplexing of separate links for A, B or A, B, C, D signaling sources.

Transmit Transparency Registers

The Transmit Transparency Registers, TTR1 - TTR3, are shown in Figure 6. Individual DS0 channels in the T1 frame

Figure 5: Transmit Control Register

(MSB)							(LSB)
ODF	TFPT	TCP	RBSE	TIS	193SI	TBL	TYEL

Symbol	Position	Name And Description
ODF	TCR.7	Output Data Format. 0 = Bipolar data at TPOS and TNEG. 1 = NRZ data at TPOS; TNEG = 0.
TFPT	TCR.6	Transmit Framing Pass Through. 0 = FT/FPS sourced internally. 1 = FT/FPS sampled at TSER during F-bit time.
TCP	TCR.5	Transmit CRC Pass Through. 0 = Transmit CRC code internally generated. 1 = TSER sampled at CRC F-bit time for external CRC insertion.
RBSE	TCR.4	Robbed Bit Signaling Enable. 1 = signaling inserted in all channels during signaling frames. 0 = No signaling inserted. (The TTR registers allow the user to disable signaling insertion on selected DS0 channels.)
TIS	TCR.3	Transmit Idle Code Select. Determines idle code format to be inserted into channels marked by the TIR registers. 0 = insert 7F (Hex) into marked channels. 1 = insert FF (Hex) into marked channels.
193SI	TCR.2	193S S-bit Insertion. Determines source of transmitted S-bit. 0 = internal S-bit generator. 1 = external (sampled at TLINK input).
TBL	TCR.1	Transmit Blue Alarm. 0 = disabled. 1 = enabled.
TYEL	TCR.0	Transmit Yellow Alarm. 0 = disabled. 1 = enabled.

may be programmed clear (no inserted robbed bit signaling and no bit 7 zero suppression) by setting the appropriate bits in the TTR registers. Channel transparency is required in mixed voice/data and data-only environments such as ISDN, where data integrity must be maintained.

Transmit Idle Code Insertion

The Transmit Idle Registers, TIR1 - TIR3, are shown in Figure 7. Individual outgoing channel in the frame can be programmed with idle code by asserting the appropriate bits in the transmit idle registers. One of two idle code formats, 7F (Hex) and FF (Hex) may be selected by the user via TCR.3. If enabled, robbed bit signaling data is inserted into the idle channel, unless the appropriate TTR bit is set for that channel. This feature eliminates external hardware currently required to intercept and stuff unoccupied channels in the DS1 bit stream. Transmit insertion hierarchy is shown in Figure 8.

Transmit Multiframe Timing

Transmit multiframe timing for 193S framing and 193E framing is shown in Figures 9 and 10, respectively. Transmit multiframe boundary timing is shown in Figure 11.

Figure 6: Transmit Transparency Registers

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TTR1
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TTR2
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TTR3

Symbol	Position	Name And Description
CH24	TTR3.7	Transmit Transparency Registers. Each of these bit positions represents a DS0 channel in the outgoing frame. When set, the corresponding channel is transparent.
CH1	TTR1.0	

Figure 7: Transmit Idle Registers

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3

Symbol	Position	Name And Description
CH24	TIR3.7	Transmit Idle Registers. Each of these bit positions represents a DS0 channel in the outgoing frame. When set, the corresponding channel will output an idle code format determined by TCR.3.
CH1	TIR1.0	

Figure 8: Transmit Insertion Hierarchy

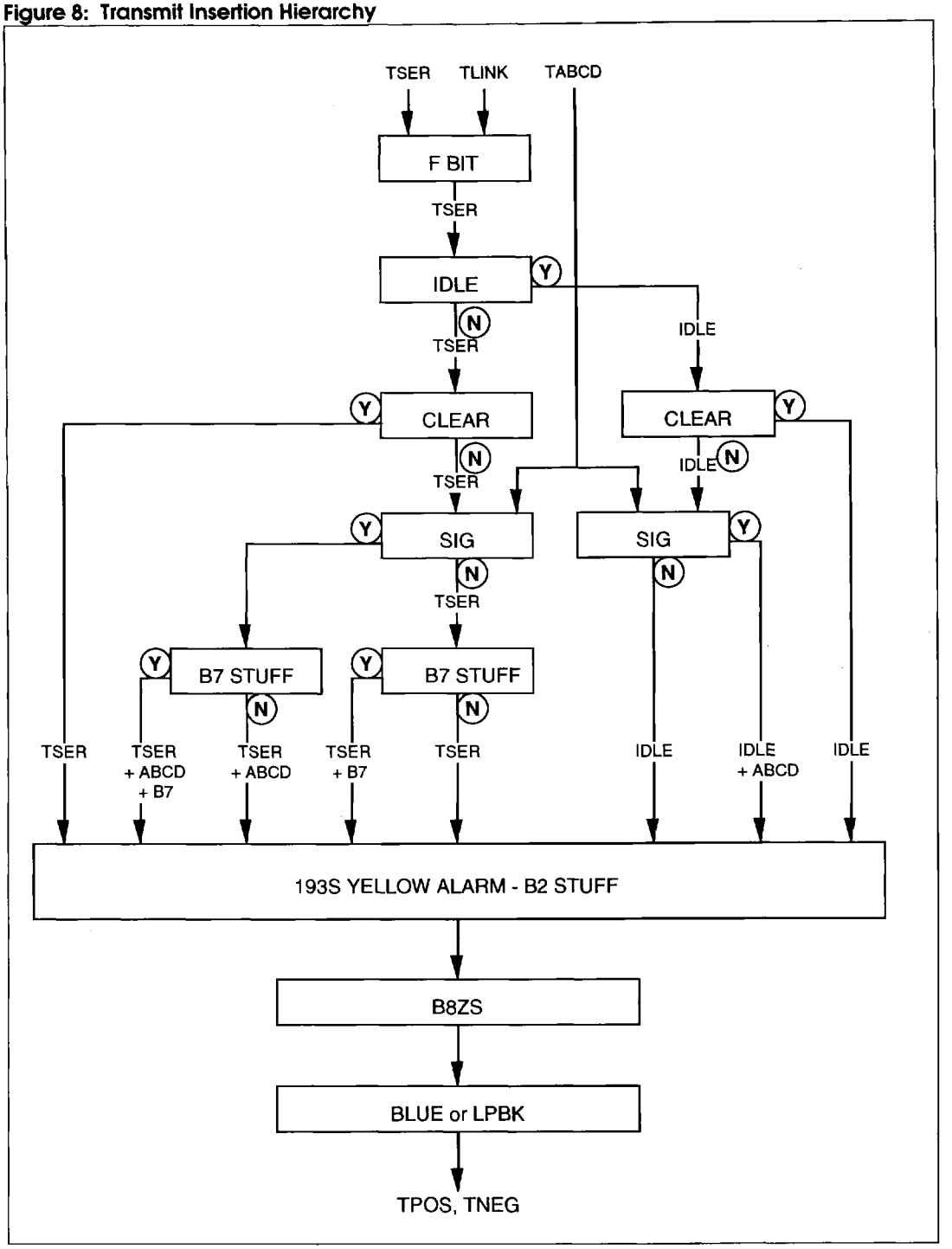
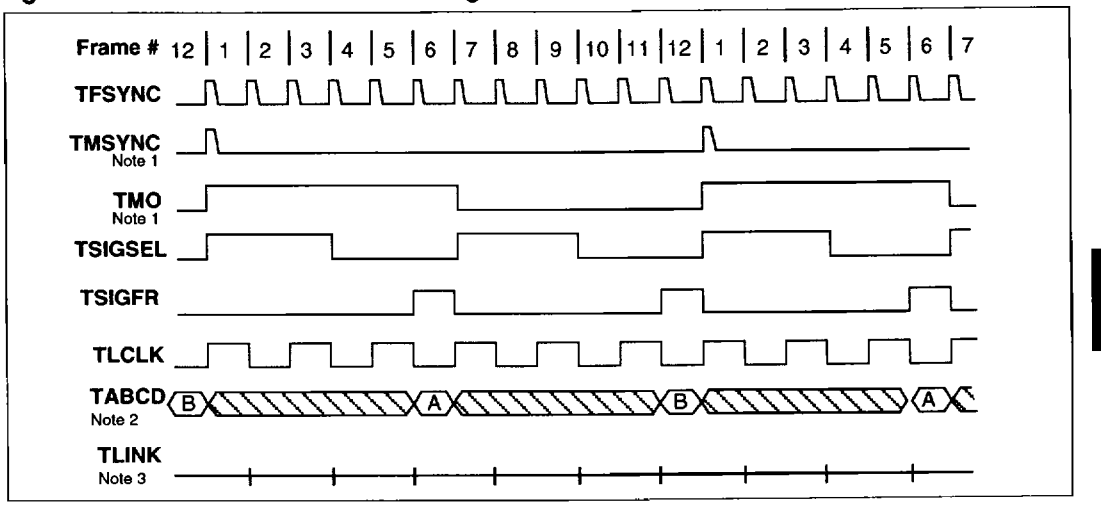
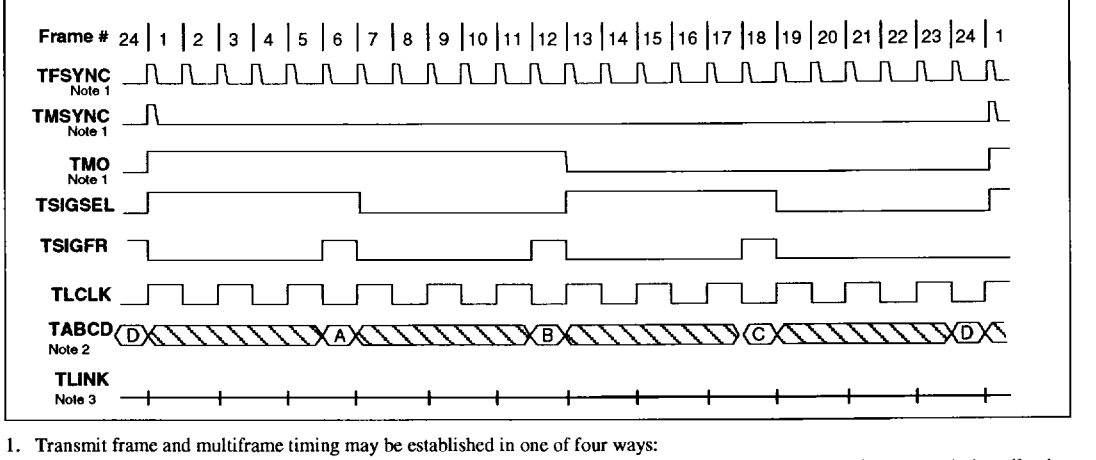


Figure 9: 193S Transmit Multiframe Timing



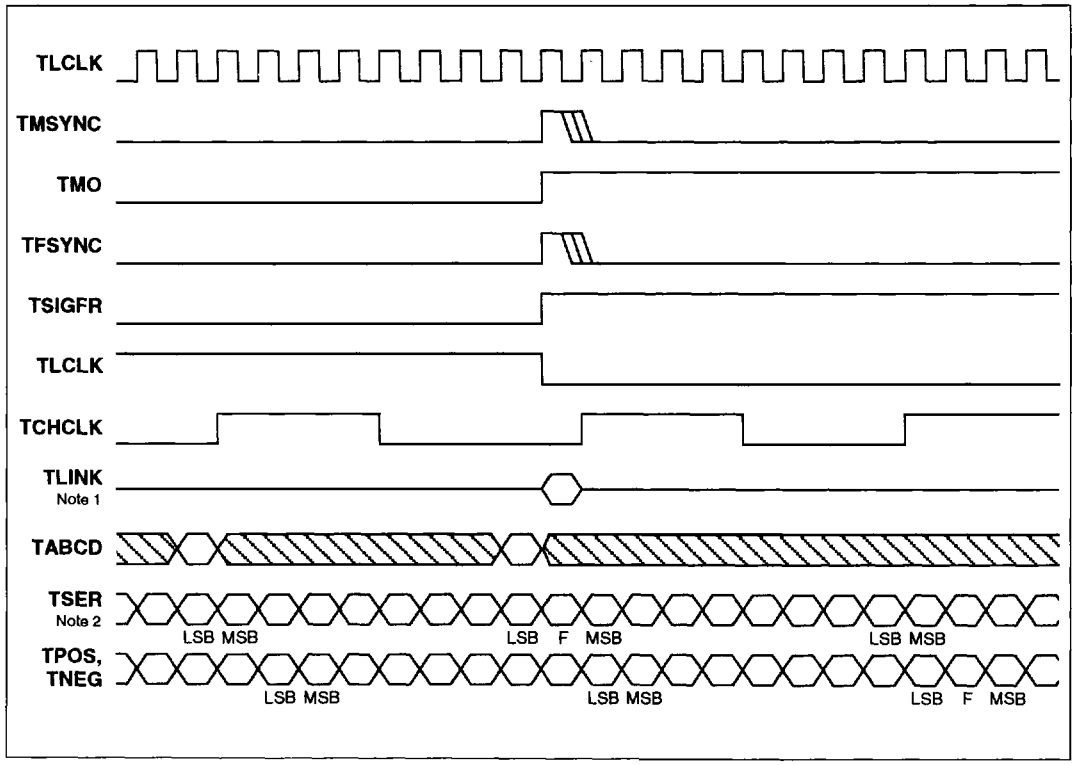
1. Transmit frame and multiframe timing may be established in one of four ways:
   a. With TFSYNC tied low, TMSYNC may be pulsed high once every multiframe period to establish multiframe boundaries, allowing internal counters to determine frame timing.
   b. TFSYNC may be pulsed every 125 microseconds; pulsing TMSYNC once establishes multiframe boundaries.
   c. TMSYNC and TFSYNC may be continuously pulsed to establish and reinforce frame and superframe timing.
   d. If TMSYNC is tied low and TFSYNC is pulsed at frame boundaries, the transmitter will establish an arbitrary multiframe boundary as indicated by TMO.
2. Channels in which robbed bit signaling is enabled will sample TABCD during the LSB bit time in frames indicated.
3. When external S-bit insertion is enabled, TLINK will be sampled during the F-bit time of even frames and inserted into the outgoing data stream.

Figure 10: 193E Transmit Multiframe Timing



1. Transmit frame and multiframe timing may be established in one of four ways:
   a. With TFSYNC tied low, TMSYNC may be pulsed high once every multiframe period to establish multiframe boundaries, allowing internal counters to determine frame timing.
   b. TFSYNC may be pulsed every 125 microseconds; pulsing TMSYNC once establishes multiframe boundaries.
   c. TMSYNC and TFSYNC may be continuously pulsed to establish and reinforce frame and superframe timing.
   d. If TMSYNC is tied low and TFSYNC is pulsed at frame boundaries, the transmitter will establish an arbitrary multiframe boundary as indicated by TMO.
2. Channels in which robbed bit signaling is enabled will sample TABCD during the LSB bit time in frames indicated.
3. TLINK is sampled during the F-bit time of odd frames and inserted into the outgoing data stream (FDL data).

Figure 11: Transmit Multiframe Boundary Timing



1. TLINK timing shown is for 193E framing. In 193E framing, TLINK is sampled as indicated for insertion into F-bit position of odd frames. When S-bit insertion is enabled in 193S framing, TLINK is sampled during even frames.
2. If TCR.5 = 1, TSER is sampled during the F-bit time of CRC frames for insertion into the outgoing data stream (193E framing only).

Receive Control Register

The Receive Control Register (RCR) is shown in Figure 12.

Receive Code Insertion

Incoming receive channels can be replaced with idle (Hex 7F) or digital milliwatt (u-Law format) codes. The Receive Mark Registers (RMR 1 - RMR3) indicate which channels are inserted. RMR registers are shown in Figure 13. When set, bit RCR.5 serves as a global enable for marked channels, and bit RCR.4 selects inserted code format: 0 = idle code, 1 = digital milliwatt.

Receive Synchronizer

Bits RCR.0 through RCR.3 allow the user to control operational characteristics of the synchronizer. Sync algorithm, candidate qualify testing, auto resync, and command resync modes may be altered at any time in response to changing span conditions.

2

Figure 12: Receive Control Register

(MSB)							(LSB)
ARC	OOF	RCI	RCS	SYNCC	SYNCT	SYNCE	RESYNC

Symbol	Position	Name And Description
ARC	RCR.7	Auto Resync Criteria. 0 = Resync on OOF or RCL event. 1 = resync on OOF only.
OOF	RCR.6	Out-Of-Frame Condition Detection. 0 = two of four framing bits in error. 1 = two of five framing bits in error.
RCI	RCR.5	Receive Code Insert. When set, the receive code selected by RCR.4 is inserted into channels marked by RMR registers. If clear, no code is inserted.
RCS	RCR.4	Receive Code Select. 0 = idle code. 1 = digital Milliwatt.
SYNCC	RCR.3	Sync Criteria. Determines the type of algorithm used by the receive synchronizer and differs for each frame mode. **193S Framing** (CCR.4 = 0). 0 = synchronize to frame boundaries using F_T pattern, then search for multiframe using F_S. 1 = cross couple F_T and F_S patterns in sync algorithm. **193E Framing** (CCR.4 = 1). 0 = normal sync (uses FPS only). 1 = validate new alignment with CRC before declaring sync.
SYNCT	RCR.2	Sync Time. If set, 24 consecutive F-bits of the framing pattern must be qualified before sync is declared. If clear, 10 bits are qualified.
SYNCE	RCR.1	Sync Enable. If clear, the transceiver will automatically begin a resync if two of the previous four or five framing bits were in error, or if carrier loss is detected. If set, no auto resync occurs.
RESYNC	RCR.0	Resync. When toggled low to high, the transceiver will initiate resync immediately. The bit must be cleared, then set again for subsequent resyncs.

Receive Signaling

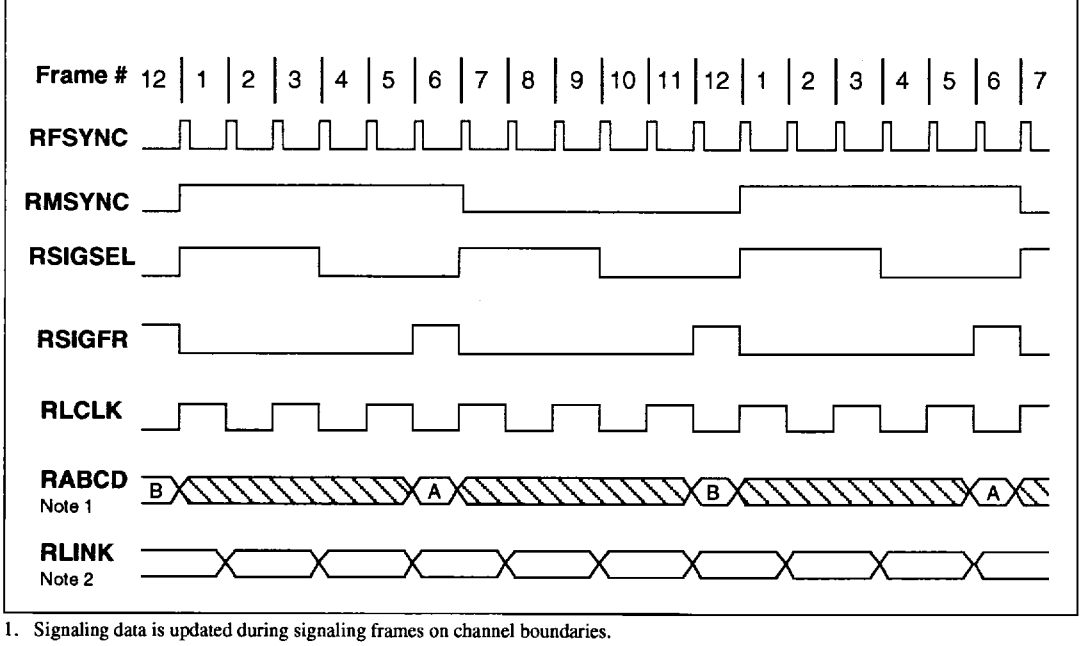
Robbed bit signaling data is presented at RABCD during each channel time in signaling frames for all 24 incoming channels. Logical combination of clocks RMSYNC, RSIGFR and RSIGSEL allow the user to identify and extract AB or ABCD signaling data. Receive multiframe timing for 193S and 193E framing modes are shown in Figures 14 and 15, respectively. Receive multiframe boundary timing is shown in Figure 16.

Figure 13: Receive Mark Registers

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RMR1
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RMR2
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RMR3

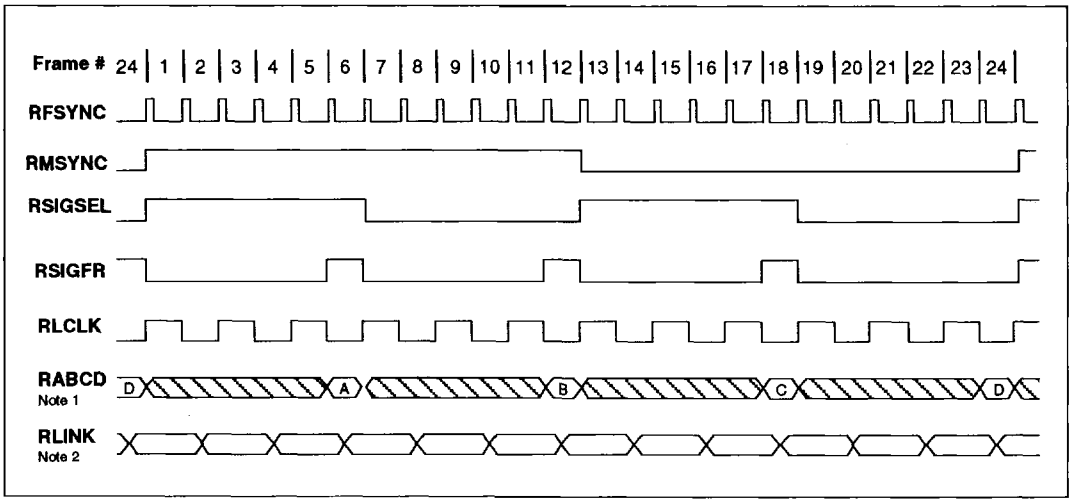
Symbol	Position	Name And Description
CH24	RMR3.7	Receive Mark Registers. Each of these bit positions represents a DS0 channel in the incoming T1 frame. When set, the corresponding channel will output codes determined by RCR.4 and RCR.5.
CH1	RMR1.0	

Figure 14: 193S Receive Multiframe Timing



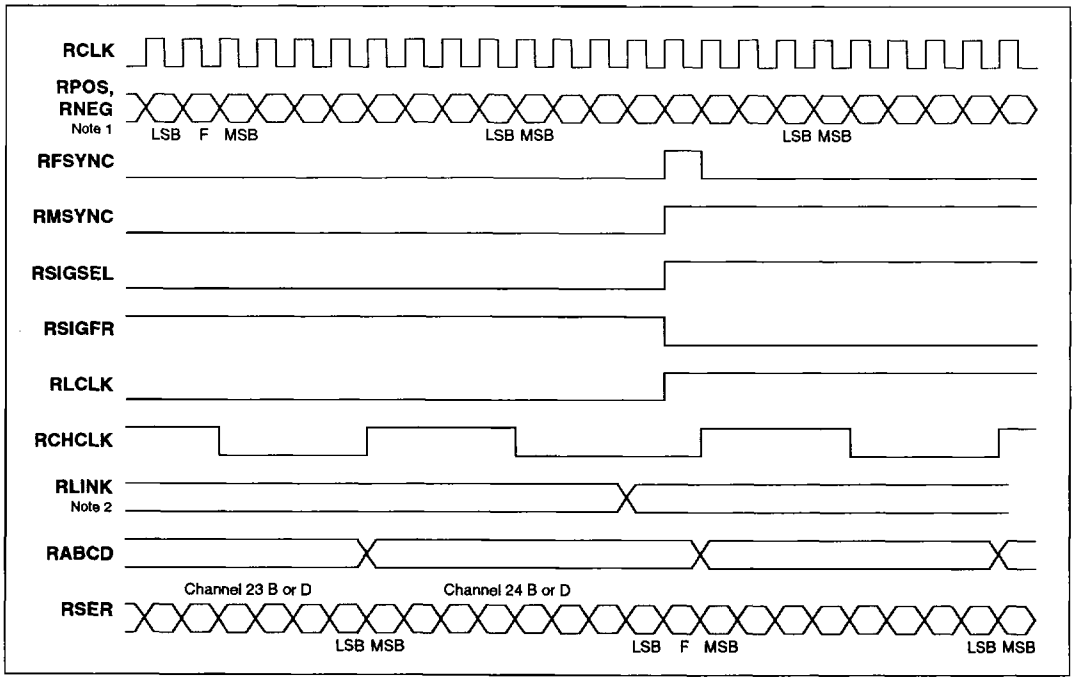
1. Signaling data is updated during signaling frames on channel boundaries. RABCD is the LSB of each channel word in non-signaling frames.
2. RLINK data (S-bit) is updated one bit time prior to S-bit frames and held for two frames.

Figure 15: 193E Receive Multiframe Timing



1. Signaling data is updated during signaling frames on channel boundaries. RABCD is the LSB of each channel word in non-signaling frames.
2. RLINK data (FDL-bit) is updated one bit time prior to odd frames and held for two frames.

Figure 16: Receive Multiframe Boundary Timing



1. Total delay from RPOS and RNEG to RSER output is 13 RCLK periods.
2. RLINK timing shown is for 193E timing. In 193S timing, RLINK is updated on even frame boundaries and is held across multiframe edges.

Receive Alarm Reporting

Incoming serial data is monitored by the transceiver for alarm occurrence. Alarm conditions are reported in two ways: (1) via transition on the alarm output pins; and (2) registered interrupt, in which the host controller reads the Receive Status Register (RSR) in response to an alarm driven interrupt. The RSR register is shown in Figure 17. Interrupts may be direct, in which the transceiver demands service for a real time alarm, or count-overflow triggered, in which an on-board alarm event counter exceeds a user-programmed threshold. The user may mask individual alarm conditions by clearing the appropriate bits in the receive interrupt mask register (RIMR). The RIMR register is shown in Figure 18.

Alarm Servicing

The host controller must service the transceiver in order to clear an interrupt condition. Clearing appropriate bits in the RIMR will unconditionally clear an interrupt. Direct interrupts (those driven from real-time alarms) will be cleared when the RSR is directly read, unless the alarm condition still exists. Count-overflow interrupts (BVCS, FCS) are not cleared by a direct read of the RSR. They will be cleared only when the user presets the appropriate count register to a value other than all "1's." A burst read of the RSR will not clear an interrupt condition.

Alarm Counters

The three on-board alarm event counters (BPV, OOF, and ESF) allow the transceiver to monitor and record error events without processor intervention on each event occurrence. All of these counters are presetable by the user, establishing an event count interrupt threshold. As each counter saturates, the next error event occurrence will set a bit in the RSR and generate an interrupt unless masked. The user may read these registers at any time; in many systems, the host will periodically poll these registers to establish link error rate performance.

Figure 17: Receive Status Register (RSR)

(MSB)							(LSB)
BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS

Symbol	Position	Name And Description
BVCS	RSR.7	Bipolar Violation Count Saturation. Set when the 8-bit counter at BVCR saturates.
ECS	RSR.6	Error Count Saturation. Set when either of the 4-bit counters at ECR saturates.
RYEL	RSR.5	Receive Yellow Alarm. Set when yellow alarm detected. (Detected yellow alarm format determined by CCR.4 and CCR.3.)
RCL	RSR.4	Receive Carrier Loss. Set when 32 consecutive "0's" appear at RPOS and RNEG.
FERR	RSR.3	Frame Bit Error. Set when F_T (193S) or FPS (193E) bit error occurs.
B8ZSD	RSR.2	Bipolar Eight Zero Substitution Detect. Set when B8ZS code word detected.
RBL	RSR.1	Receive Blue Alarm. Set when two consecutive frames have less than three zeros (total) in the data stream (F-bit positions not tested).
RLOS	RSR.0	Receive Loss of Sync. Set when resync is in progress; if RCR.1 = 0, RLOS transitions high on an OOF event or carrier loss, indicating auto resync.

BVCR - Bipolar Violation Count Register

The BVCR register is shown in Figure 19. This 8-bit binary up counter saturates at 255 and will generate an interrupt for each occurrence of a bipolar violation once saturated (RIMR.7 = 1). Presetting this register allows the user to establish specific count interrupt thresholds. The counter will count "up" to saturation from the preset value, and may be read at any time. Counter increments occur at all times and are not disabled by resync.

Figure 18: Receive Interrupt Mask Register (RIMR)

(MSB)							(LSB)
BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS

Symbol	Position	Name And Description
BVCS	RIMR.7	Bipolar Violation Count Saturation Mask. 1 = interrupt enabled. 0 = interrupt masked.
ECS	RIMR.6	Error Count Saturation Mask. 1 = interrupt enabled. 0 = interrupt masked.
RYEL	RIMR.5	Receive Yellow Alarm Mask. 1 = interrupt enabled. 0 = interrupt masked.
RCL	RIMR.4	Receive Carrier Loss Mask. 1 = interrupt enabled. 0 = interrupt masked.
FERR	RIMR.3	Frame Bit Error Mask. 1 = interrupt enabled. 0 = interrupt masked.
B8ZSD	RIMR.2	Bipolar Eight Zero Substitution Detect Mask. 1 = interrupt enabled. 0 = interrupt masked.
RBL	RIMR.1	Receive Blue Alarm Mask. 1 = interrupt enabled. 0 = interrupt masked.
RLOS	RIMR.0	Receive Loss of Sync Mask. 1 = interrupt enabled. 0 = interrupt masked.

Figure 19: Bipolar Violation Count Register (BVCR)

(MSB)							(LSB)
BVD7	BVD6	BVD5	BVD4	BVD3	BVD2	BVD1	BVD0

Symbol	Position	Name And Description
BVD7	BVCR.7	MSB of bipolar violation count.
BVD0	BVCR.0	LSB of bipolar violation count.

Error Count Register - Out Of Frame and Errored Superframe Events

These separate 4-bit binary up counters saturate at a count of 15 and will generate an interrupt for each occurrence of an OOF event or an ESF event after saturation (RIMR.6 = 1). Presetting these counters allows the user to establish specific count interrupt thresholds. The counters will count up to saturation from the preset value, and may be read at any time. These counters share the same register address, and must be written to or read from simultaneously.

Out Of Frame (OOF) is declared when at least two of four (or five) consecutive framing bits are in error. F_T bits are tested for OOF occurrence in 193S; the FPS bits are tested in 193E. OOF events are recorded by the 4-bit OOF counter in the error count register. The OOF counter records out of frame events in both 193S and 193E. In the 193E framing mode, the OOF event is logically "OR'ed" with an on-chip generated CRC checksum. This event, known as errored superframe, is recorded by the 4-bit ESF error counter in the error count register. In the 193S framing mode, the 4-bit ESF counter records individual F_T and F_S errors when RCR.3 = 1, or F_T errors only when RCR.3 = 0. ECR counter increments are disabled when resync is in progress (RLOS high).

Alarm Outputs

The transceiver also provides direct alarm outputs for applications when additional decoding and demuxing are required to supplement the on-board alarm logic. Alarm output timing is shown in Figure 21.

RLOS Output

The receive loss of sync output indicates the status of the receiver synchronizer circuitry: when high, an off-line resynchronization is in progress and a high-low transition indicates resync is complete. The RLOS bit (RSR.0) is a latched version of the RLOS output. If the auto-resync mode is selected (RCR.1 = 0) RLOS is a real time indication of a carrier loss or OOF event occurrence.

RYEL Output

The yellow alarm output transitions high when a yellow alarm is detected. A high-low transition indicates the alarm condition has been cleared. The RYEL bit (RSR.5) is a latched version of the RYEL output. In 193E framing, the yellow alarm pattern detected is 16 pattern sets of 00 (Hex) and FF (Hex) received at RLINK. In 193S framing, the yellow alarm format is dependent on CCR.3: if CCR.3 = 0, the RYEL output transitions high if bit 2 of the 256 or more consecutive channels is 0; If CCR.3 = 1, yellow alarm is declared when the S-bit received in frame 12 is 1.

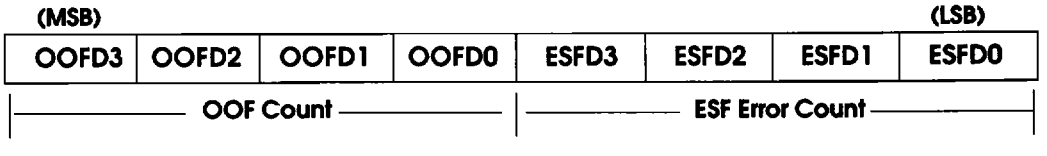
RBV output

The bipolar violation output transitions high when the accused bit emerges at RSER. RBV will go low at the next bit time if no additional violations are detected.

RFER Output

The receive frame error output transitions high at the F-bit time and is held high for two bit periods when a frame error

Figure 20: Error Count Register (ECR)



Symbol	Position	Name And Description
OOFD3	ECR.7	MSB of OOF event count.
OOFD0	ECR.4	LSB of OOF event count.
ESFD3	ECR.3	MSB of ESF error count.
ESFD0	ECR.0	LSB of ESF error count.

occurs. In 193S framing, F_T and F_S patterns are tested. The FPS pattern is tested in 193E framing. Additionally, in 193E framing, RFER reports a CRC error by a low-high-low transition (one bit period wide) one half RCLK period before a low-high transition on RMSYNC.

Reset

A high-low transition on $\overline{RST}$ clears all registers and forces immediate receive resync when $\overline{RST}$ returns high. This reset has no effect on transmit frame, multiframe, or channel counters. $\overline{RST}$ must be held low on system power-up to insure proper initialization of transceiver counters and registers. Following reset, the host processor should restore all control modes by writing appropriate registers with control data.

Hardware Mode

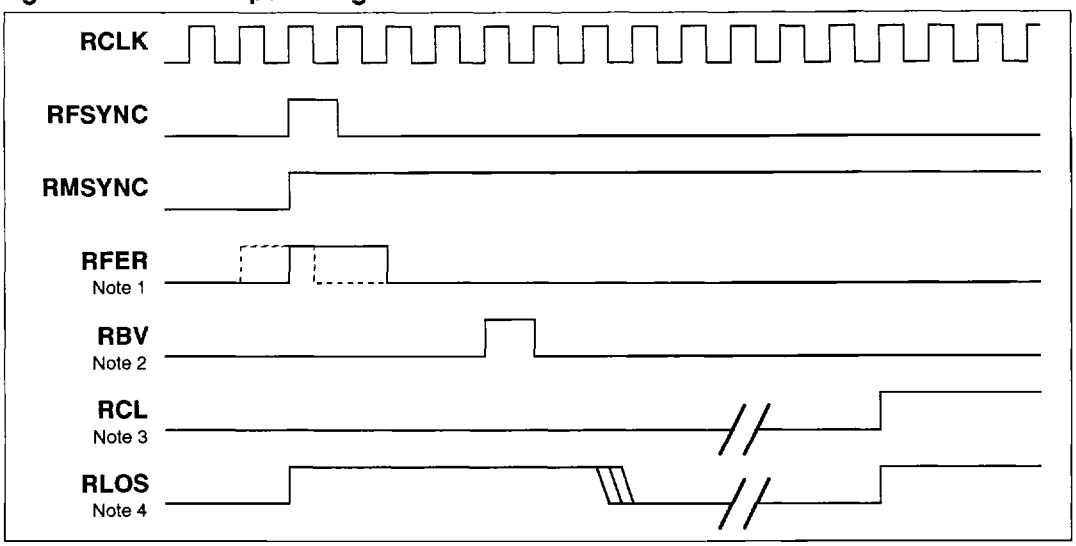
For preliminary system prototyping or applications which do not require the features offered by the serial port, the transceiver can be reconfigured by the SPS pin. Tying SPS to VSS disables the serial port, clears all internal registers except CCR and TCR and redefines pins 14 through 18 as mode control inputs. Hardware mode control inputs are listed in Table 6. The Hardware mode allows device retrofit into existing applications where mode control and alarm conditioning circuits are often designed with discrete logic.

Hardware Common Control

In the Hardware mode bits TCR.2, CCR.4, TCR.0, CCR.1 and CCR.2 map to pins 14 through 18. The loopback feature (bit CCR.0) is enabled by tying pins 17 (zero suppression) and 18 (B8ZS) to 1. (The last states of pins 17 and 18 are latched as when both pins are taken high, preserving the current zero suppression mode). Robbed bit signaling (bit TCR.4) is enabled for all channels. The user may tie TSER to TABCD externally to disable signaling if so desired. Bit CCR.3 is forced to 0, which selects bit 2 yellow alarm in 193S framing. Contents of the RCR, as well as the remaining bit locations in the CCR and TCR, are cleared in the Hardware mode. The $\overline{RST}$ input may be used to force immediate receiver resync, and has no effect on transmit.

2

Figure 21: Alarm Output Timing



NOTES:

1. RFER transitions high during F-bit time if received framing pattern bit is in error. (Frame 12 F-bits in 193S are ignored if CCR.3 = 1.) Also, in 193E, RFER transitions ½ bit time before the rising edge of RMSYNC to indicate a CRC error for the previous multiframe.
2. RBV indicates received bipolar violations and transitions high when accused bit emerges from RSER. If B8ZS is enabled, RBV will not report the zero replacement code.
3. RCL transitions high (during 32nd bit time) when 32 consecutive bits received are "0". RCL transitions low when the next "1" is received.
4. RLOS transitions high during the F-bit time that caused an OOF event (any 2 of 4 consecutive FT or FPS bits are in error) if auto-resync mode is selected (RCR.1 = 0). Resync will also occur when loss of carrier is detected (RCL = 1). When RCR.1 = 1, RLOS remains low until resync occurs, regardless of OOF or carrier loss flags. In this situation, resync is initiated only when RCR.0 transitions low-to-high or the $\overline{RST}$ pin transitions high-low-high.

T1 OVERVIEW

Framing Standards

The LXP2180A is compatible with the existing Bell System D4 framing standard described in AT&T PUB 43801 and the new extended superframe format (ESF) as described in AT&T C.B. #142. In this document, D4 framing is referred to as 193S, and ESF (also known as Fe) is referred to as 193E. Programmable features of the LXP2180A allow support of other framing standards which are derivatives of 193E and 193S. The salient differences between the 193S and 193E formats are the number of frames per superframe and use of the F-bit position (refer to Tables 7 and 8). In 193S, 12 frames make up a superframe; in 193E, 24. A frame consists of 24 channels (time-slots) of 8-bit data preceded by an F-bit. Channel data is transmitted and received MSB first.

F-Bits

The use of the F-bit position in 193S is split between the terminal framing pattern (known as F_T-Bits) which provides frame alignment information, and the signaling framing pattern (known as F_S-bits) which provides multiframe alignment information. In 193E framing, the F-bit position is shared by the framing pattern sequence (FPS), which provides frame and multiframe alignment information, a 4 kHz data link (Facility data link) known as FDL, and CRC (cyclic redundancy check) bits. The FDL bits are used for control and maintenance (inserted by the user at TLINK). The CRC bits are an indicator of link quality and may be monitored by the user to establish error performance.

Signaling

During frames 6 and 12 in 193S, A and B signaling information is inserted into the LSB of all channels transmitted. In 193E, A and B data is inserted into frames 6 and 12; C and D data is inserted into frames 18 and 24. This allows a maximum of four signaling states to be transmitted per superframe in 193S; 16 states per superframe in 193E.

Alarms

The LXP2180A supports all alarm pattern generation and detection required in typical Bell System applications. These alarm modes are explained in AT&T PUB 43801, AT&T C. B. #142 and elsewhere in this document.

Line Coding

T1 line data is transmitted in a bipolar alternate mark inversion (AMI) line format; ones are transmitted as alternating negative and positive pulses and zeros are simply the absence of pulses. This technique minimizes DC voltage on the T1 span and allows clock to be extracted from data. The network currently has a one's density constraint to keep clock extraction circuitry functioning, which is usually met by forcing bit 7 of any channel consisting of all 0's to 1. The use of Bipolar Eight Zero Substitution (B8ZS) satisfies all the ones density requirements, while allowing data traffic to be transmitted without corruption. This feature is known as clear channel and is explained more completely in AT&T C.B. #144. When the B8ZS feature is enabled, any outgoing stream of eight consecutive zeros is replaced with a B8ZS code word. If the last "one" transmitted was positive, the

Table 6: Hardware Mode Pin Descriptions

Pin #	Register Bit Location	Name and Description
14	TCR-D2	193S - S-bit Insertion[1]. 1 = external; 0 = internal
15	CCR-D4	Framing Mode Select. 1 = 193E; 0 = 193S
16	TCR-D0	Transmit Yellow Alarm[2,3]. 1 = enabled; 0 = disabled
17	CCR-D1	Zero Suppression[3]. 1 = bit 7 stuffing; 0 = transparent
18	CCR-D2	B8ZS[3]. 1 = enabled; 0 = disabled

NOTES:
1. S-bit yellow alarm (193S) is not internally supported; however, the user may elect to insert external S-bits for alarm purposes.
2. Bit 2 (193S) and data link (193E) yellow alarms are supported.
3. Tying pins 17 and 18 high enables loopback in the Hardware mode.

inserted code is 000 + - 0 - +; if negative, the code word inserted is 000 - + 0 + -. Bipolar violations occur in the fourth and seventh bit positions, which are ignored by the DS2180A error monitoring logic when B8ZS is enabled. Any received B8ZS code word is replaced with all 0's if B8ZS is enabled. Also, the receive status register will report any occurrence of B8ZS code words to the host controller. This allows the user to monitor the link for upgrade to clear channel capability, and respond to it. The B8ZS monitoring feature works at all times and is independent of the state of CCR.2.

TRANSMITTER OVERVIEW

The transmit side of the LXP2180A is made up of six major functional blocks: timing and clock generation, data selector, bipolar coder, yellow alarm, F-bit data and CRC. The timing and clock generation circuit develops all on-board and output clocks to the system from inputs TCLK, TFSYNC and TMSYNC. The yellow alarm circuitry generates mode dependent yellow alarms. The CRC block generates checksum results utilized in 193E framing. F-bit data provides mode dependent framing patterns and allows insertion of link or S-bit data externally. All of these blocks feed into the data selector, where (under control of the CCR, TCR, TIRs and TTRs) the contents of the outgoing data stream are established by bit selection and insertion. The bipolar coder formats the output of the data selector to make it compatible with bipolar transmission techniques and inserts zero suppression codes. The bipolar coder also supports the on-board loopback feature. Input-to-output delay of the transmitter is 10 TCLK cycles.

Table 7: 193E Framing Format

Frame #	F-Bit Use			Bit use In Each Channel		Signaling-Bit Use		
	FPS[1]	FDL[2]	CRC[3]	Data	Signaling[4,5]	2-State	4-State	16-State
1	–	M	–	Bits 1 - 8				
2	–	–	C1	Bits 1 - 8				
3	–	M	–	Bits 1 - 8				
4	0	–	–	Bits 1 - 8				
5	–	M	–	Bits 1 - 8				
6	–	–	C2	Bits 1 - 7	Bit 8	A	A	A
7	–	M	–	Bits 1 - 8				
8	0	–	–	Bits 1 - 8				
9	–	M	–	Bits 1 - 8				
10	–	–	C3	Bits 1 - 8				
11	–	M	–	Bits 1 - 8				
12	1	–	–	Bits 1 - 7	Bit 8	A	B	B
13	–	M	–	Bits 1-8				
14	–	–	C4	Bits 1 - 8				
15	–	M	–	Bits 1 - 8				
16	0	–	–	Bits 1 - 8				
17	–	M	–	Bits 1 - 8				
18	–	–	C5	Bits 1 - 7	Bit 8	A	A	C
19	–	M	–	Bits 1-8				
20	1	–	–	Bits 1 - 8				
21	–	M	–	Bits 1 - 8				
22	–	–	C6	Bits 1 - 8				
23	–	M	–	Bits 1 - 8				
24	1	–	–	Bits 1 - 7	Bit 8	A	B	D

NOTES:
1. FPS - Framing Pattern Sequence.
2. FDL - 4 kHz Facility Data Link; M = message bits.
3. CRC - Cyclic Redundancy Check Bits. The CRC code will be internally generated by the device when TCR.5 = 0. When TCR.5 = 1, externally supplied CRC data will be sampled at TSER during the F-bit time of frames 2, 6, 10, 14, 18 and 22.
4. The user may program any individual channels clear, in which case Bit 8 will be used for data, not signaling.
5. Depending on application, the user can support 2-state, 4-state or 16-state signaling by the appropriate decodes of TMO, TSIGFR, TSIGSEL (transmit side) and RMSYNC, RSIGFR and RSIGSEL (receive side).

RECEIVER OVERVIEW

Synchronizer

The heart of the receiver is the synchronizer/sync monitor. This circuit serves two purposes: 1) monitoring the incoming data stream for loss of frame or multiframe alignment; and 2) searching for a new frame alignment pattern when sync loss is detected. When sync loss is detected, the synchronizer begins an off-line search for the new alignment; all output timing signals remain at the old alignment with the exception of RSIGFR, which is forced low during resync. When one and only one candidate is qualified, the output timing will move to the new alignment at the beginning of the next multiframe. One frame later, RLOS will transition low, indicating valid sync and the resumption of the normal sync monitoring mode. Several bits in the RCR allow tailoring of the resync algorithm by the user. These bits are described in the following paragraphs.

Sync Time (RCR.2)

Bit RCR.2 determines the number of consecutive framing pattern bits to be qualified before SYNC is declared. If RCR.2 = 1, the algorithm will validate 24 bits, if RCR.2 =0, 10 bits are validated. 24-bit testing results in superior false framing protection, while 10-bit testing minimizes reframe time (although in either case, the synchronizer will only establish resync when one and only one candidate is found).

Resync (RCR.0)

A zero-to-one transition of RCR.0 causes the synchronizer to search for the framing pattern sequence immediately, regardless of the internal sync status. In order to initiate another resync command, this bit must be cleared and then set again.

Sync Enable (RCR.1)

When RCR.1 is cleared, the receiver will initiate automatic resync if any of the following events occur:
1) an OOF event (Out-Of-Frame), or 2) carrier loss (32 consecutive 0's appear at RPOS and RNEG). An OOF event occurs any time that 2 of 4 F_T or FPS bits are in error. When RCR.1 is set, the automatic resync circuitry is disabled; in this case, resync can only be initiated by setting RCR.0 to 1, or externally via a low-high transition on $\overline{RST}$. Note that using $\overline{RST}$ to initiate resync resets the receive output timing while $\overline{RST}$ is low; use of RCR.1 does not affect output timing until the new alignment is located.

Sync Criteria (RCR.3)

193E Bit RCR.3 determines which sync algorithm is utilized when resync is in progress (RLOS = 1). In 193E framing, when RCR.3 = 0, the synchronizer will lock only to the FPS pattern and will move to the new frame and multiframe alignment after the framing candidate is

Table 8: 193S Framing Format

Frame #	F-Bit Use		Bit use In Each Channel		Signaling-Bit Use
	Ft[1]	Fs[2]	Data	Signaling[4]	
1	1	–	Bits 1 - 8		
2	–	0	Bits 1 - 8		
3	0	–	Bits 1 - 8		
4	–	0	Bits 1 - 8		
5	1	–	Bits 1 - 8		
6	–	1	Bits 1 - 7	Bit 8	A
7	0	–	Bits 1 - 8		
8	–	1	Bits 1 - 8		
9	1	–	Bits 1 - 8		
10	–	1	Bits 1 - 8		
11	0	–	Bits 1 - 8		
12	–	0[3]	Bits 1 - 7	Bit 8	B

NOTES:
1. FT (terminal framing) bits provide frame alignment information.
2. FS (signaling frame) bits provide multiframe alignment information.
3. The S-bit in frame 12 may be used for yellow alarm transmission and detection in some applications.
4. The user may program any individual channels clear, in which case Bit 8 will be used for data, not signaling.

qualified. RLOS will go low one frame after the move to the new alignment. When RCR.3 = 1, the new alignment is further tested by a CRC code match. RLOS will transition low after a CRC match occurs. If no CRC match occurs in three attempts (three multiframes), the algorithm will reset and a new search for the framing pattern begins. It takes 9 ms for the synchronizer to check the first CRC code after the new alignment has been loaded. Each additional CRC test takes 3 ms. Regardless of the state of RCR.3, if more than one candidate exists after about 24 ms, the synchronizer will begin eliminating emulators by testing their CRC codes online in order to find the true framing candidate.

193S In 193S framing, when RCR.3 = 1, the synchronizer will cross check the FT pattern with the FS pattern to help eliminate false framing candidates such as digital milliwatts. The FS patterns are compared to the repeating pattern . . . 00111000111000 . . . (001llX0 if CCR.3—YELMD—is equal to a 1). In this mode, FT and FS patterns must be correctly identified by the synchronizer before sync is declared. Clearing RCR.3 causes the synchronizer to search for FT patterns (101010 . . .) without cross-coupling the FS pattern. Frame sync will be established using the FT information, while multiframe sync will be established only if valid FS information is present. If no valid FS pattern is identified, the synchronizer will move to the FT alignment, RLOS will go low, and a false multiframe position may be indicated by RMSYNC. RFER will indicate when the received S-bit pattern does not match the assumed internal multiframe alignment. This mode can be used in applications where non-standard S-bit patterns exist. In such applications, multiframe alignment information can be decoded externally by using the S-bits present at RLINK.

APPLICATIONS

Backplane Interface

A typical backplane interface circuit is shown in Figure 22. The LXP2180A is shown in Host mode with an LXP2176 providing the interface to the backplane, and an LXT300 providing the line interface.

Processor-Based Signaling

Many robbed-bit signaling applications utilize a microprocessor to insert transmit signaling data into the outgoing data stream. The circuit shown in Figure 23 decouples the processor timing from that of the LXP2180A by use of a small FIFO memory. The processor writes to the FIFO (6 bytes are written: 3 for A data, 3 for B data) only when signaling updates are required. The FIFO automatically retransmits old data when no updates occur. The system is interrupt-driven from the transmit multiframe sync input; the processor must update the FIFO prior to Frame 6 (625 µs after interrupt) to prevent data corruption. The application circuit shown supports 193S framing; additional hardware is required for 193E applications.

Table 9: Average Reframe Time[1]

Frame Mode	RCR.2 = 0			RCR.2 = 1			Units
	Min	Avg	Max	Min	Avg	Max	
193S	3.0	3.75	4.5	6.5	7.25	8.0	ms
193E	6.0	7.5	9.0	13.0	14.5	16.0	ms

NOTES:
1. Average Reframe Time is defined here as the average time it takes from the start of resync (rising edge of RLOS) to the actual loading of the new alignment (on a multiframe edge) into the output receive timing.

Figure 22: Backplane Interface Application using LXP2180A with LXP2176

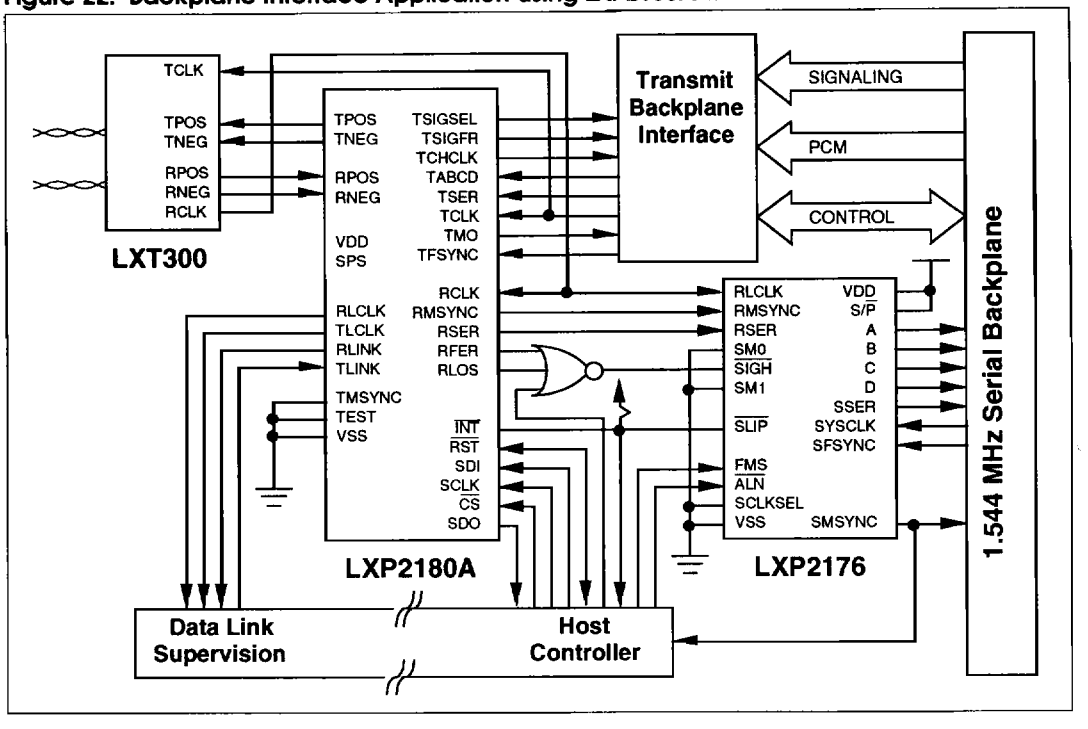
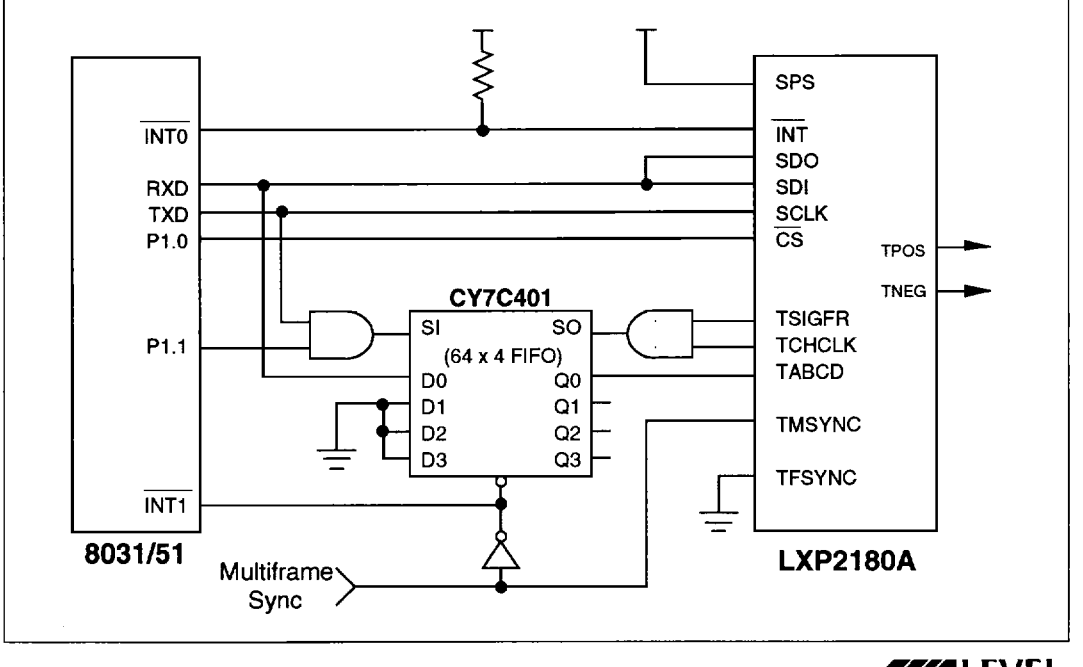


Figure 23: Processor-Based Transmit Signaling Insertion Application



Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- Voltage on any pin relative to ground -1.0V to + 7V
- Operating temperature -40 °C (min) to +85 °C (max)
- Storage temperature -55 °C (min) to +125 °C (max)
- Soldering temperature 260 °C for 10 seconds

2

Recommended Operating Conditions (Voltages are with respect to ground (GND) unless otherwise stated)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Logic 1	V_{IH}	2.0	–	V_{DD} + .3	V	
Logic 0	V_{IL}	-0.3	–	+0.8	V	
Supply voltage	V_{DD}	4.5	5	5.5	V	
Capacitance						
Input capacitance	C_{IN}	–	–	5	pF	
Output capacitance	C_{OUT}	–	–	7	pF	
DC Electrical Characteristics - Clocked operation over recommended temperature and power supply ranges						
Supply current	I_{DD}	–	3	10	mA	See Notes 2 and 3
Input leakage	I_{IL}	–	–	1	µA	
Output leakage	I_{OL}	–	–	1	µA	See Note 4
Output high current	I_{OH}	-1	–	–	mA	V_{OH} = 2.4 V, See Note 5
Output low current	I_{OL}	+4	–	-	mA	V_{OL} = 0.4 V, See Note 6

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] TCLK = RCLK = 1.544 MHz
[3] Outputs open.
[4] Applies to SDO when tristated.
[5] All outputs except INT, which is open collector.
[6] All outputs.

A.C. Electrical Characteristics - Serial Port

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions[2]
SDI to SCLK Setup	t_{DC}	50	–	–	ns	C load = 100 pF
SCLK to SDI Hold	t_{CDH}	50	–	–	ns	C load = 100 pF
SDI to SCLK Falling Edge	t_{CD}	50	–	–	ns	C load = 100 pF
SCLK Low Time	t_{CL}	250	–	–	ns	C load = 100 pF
SCLK High Time	t_{CH}	250	–	–	ns	C load = 100 pF
SCLK Rise and Fall Time	t_F, t_F	–	–	500	ns	C load = 100 pF
$\overline{CS}$ to SCLK Setup	t_{CC}	50	–	–	ns	C load = 100 pF
SCLK to $\overline{CS}$ Hold	t_{CCH}	50	–	–	ns	C load = 100 pF
$\overline{CS}$ Inactive Time	t_{CWH}	250	–	–	ns	C load = 100 pF
SCLK to SDO Valid	t_{CDV}	–	–	200	ns	C load = 100 pF
$\overline{CS}$ to SDO High Z	t_{CDZ}	–	–	75	ns	C load = 100 pF
SCLK Setup to $\overline{CS}$ Falling	t_{SSC}	50	–	–	ns	C load = 100 pF

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Measured at V_{IH} = 2.0V, V_{IL} = .8V, and 10 ns maximum rise and fall time.

Figure 24: Serial Port Write A.C. Timing

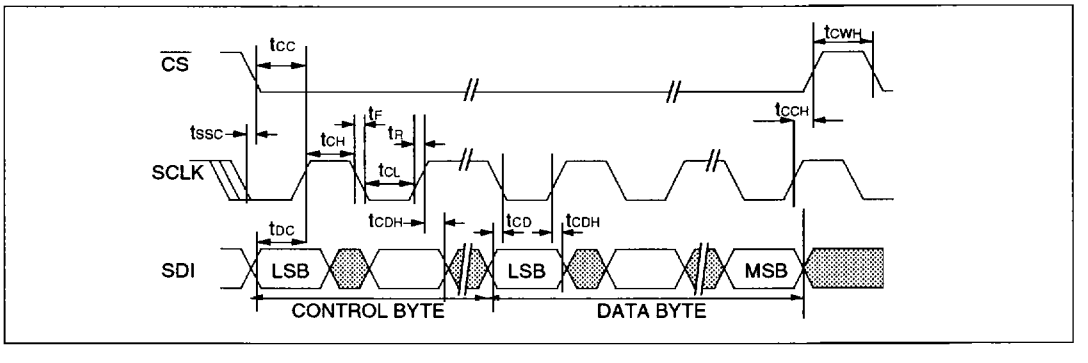
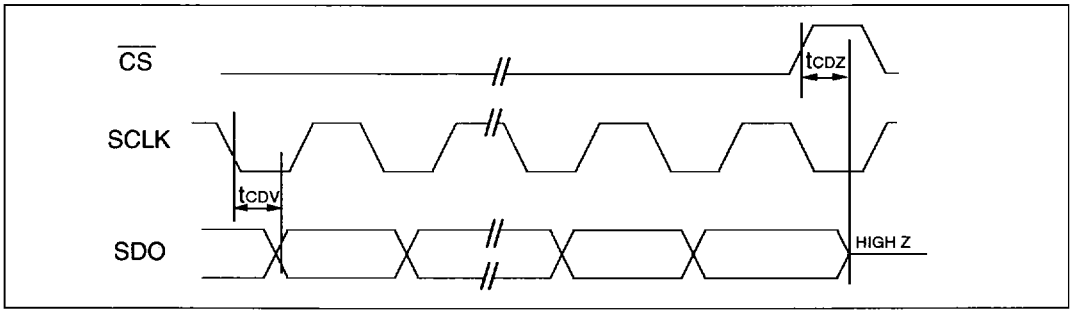


Figure 25: Serial Port Read A.C. Timing



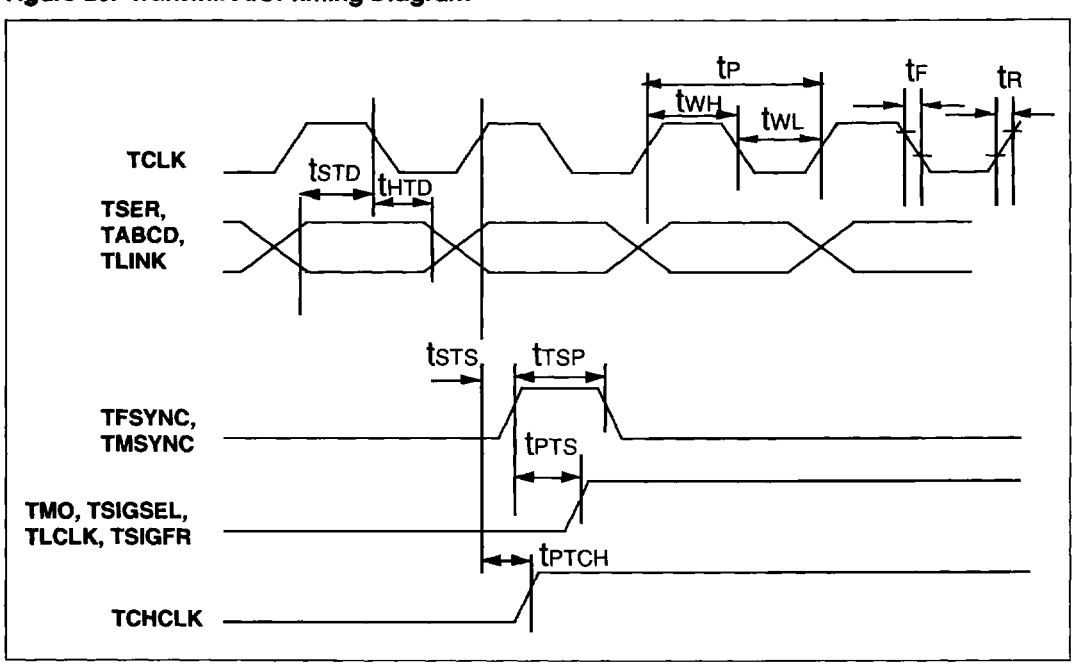
A.C. Electrical Characteristics - Transmit

Parameter	Sym	Min	Max	Units	Test Conditions[1]
TCLK Period	t_P	250	–	ns	C load = 100 pF
TCLK Pulse Width	t_{WL}, t_{WH}	125	–	ns	C load = 100 pF
TCLK, RCLK Rise & Fall Times	t_R, t_F	–	–	ns	C load = 100 pF
TSER, TABCD, TLINK Setup to TCLK Falling	t_{STD}	50	–	ns	C load = 100 pF
TSER, TABCD, TLINK Hold from TCLK Falling	t_{HTD}	50	–	ns	C load = 100 pF
TFSYNC, TMSYNC Setup to TCLK Rising	t_{STS}	-125	125	ns	C load = 100 pF
Propagation Delay TFSYNC to TMO, TSIGSEL, TSIGFR, TLCLK	t_{PTS}	–	75	ns	C load = 100 pF
Propagation Delay TCLK to TCHCLK	t_{PTCH}	–	75	ns	C load = 100 pF
TFSYNC, TMSYNC Pulse Width	t_{TSP}	100	–	ns	C load = 100 pF

[1] Measured at V_{IH} = 2.0V, V_{IL} = .8V, and 10 ns maximum rise and fall time.

2

Figure 26: Transmit A.C. Timing Diagram



A.C. Electrical Characteristics - Receive

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions[2]
Propagation Delay RCLK to RMSYNC, RFSYNC, RSIGSEL, RSIGFR, RLCLK, RCHCLK	t_{PRS}	–	–	75	ns	C Load = 100 pF
Propagation Delay RCLK to RSER, RABCD, RLINK	t_{PRD}	–	–	75	ns	C Load = 100 pF
Transition Time, All Outputs	t_{TTR}	–	–	20	ns	C Load = 100 pF
RCLK Period	t_P	250	648	–	ns	C Load = 100 pF
RCLK Pulse Width	t_{WL}, t_{WH}	125	324	–	ns	C Load = 100 pF
RCLK Rise & Fall Times	t_R, t_F	–	20	–	ns	C Load = 100 pF
RPOS, RNEG Setup to RCLK Falling	t_{SRD}	50	–	–	ns	C Load = 100 pF
RPOS, RNEG Hold to RCLK Falling	t_{HRD}	50	–	–	ns	C Load = 100 pF
Propagation Delay RCLK to RYEL, RCL, RFER, RLOS, RBV	t_{PRA}	–	–	–	ns	C Load = 100 pF
Minimum $\overline{RST}$ Pulse Width on System Power Up or Restart	t_{RST}	1	–	–	µs	C Load = 100 pF

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Measured at V_{IH} = 2.0V, V_{IL} = .8V, and 10 ns maximum rise and fall time.

Figure 27: Receive A.C. Timing Diagram