PRELIMINARY DATA SHEET

INFORMATION STORAGE DEVICES

ISD2500 Series

Single-Chip Voice Record/Playback Devices 45-, 60-, 75-, and 90-Second Durations

GENERAL DESCRIPTION

Information Storage Devices' ISD2500 Series provides high-quality, single-chip record/playback solutions for 45- to 90-second messaging applications. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smoothing filter, and speaker amplifier. In addition, the ISD2500 is fully microprocessor-compatible, allowing complex messaging and addressing to be achieved.

Recordings are stored in on-board non-volatile memory cells, providing zero-power message storage. This unique solution is made possible through ISD's patented Direct Analog Storage Technology (DAST™), whereby voice and audio signals are stored directly, in their natural analog form, into memory. Direct analog storage allows natural voice reproduction in a single-chip, solid-state solution.

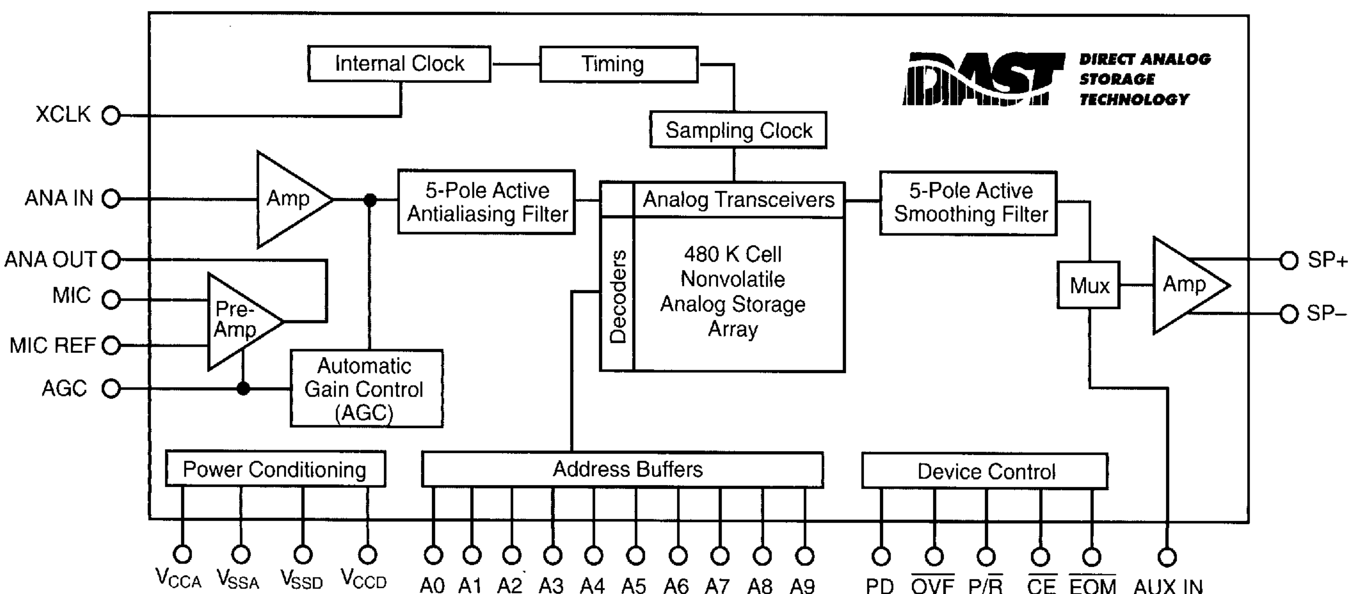
ISD2500-SERIES SUMMARY

Part Number	Duration (Seconds)	Input Sample Rate (KHz)	Upper Pass Band (KHz)
ISD2545	45	10.6	4.5
ISD2560	60	8.0	3.4
ISD2575	75	6.4	2.7
ISD2590	90	5.33	2.3

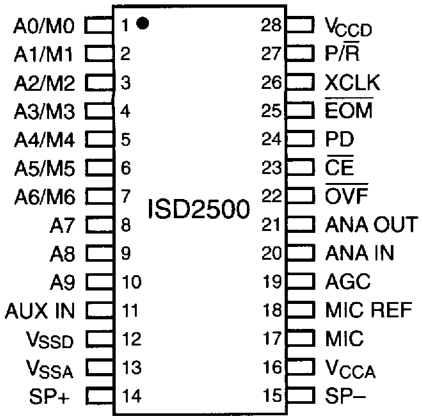
FEATURES

- **Easy-to-use single-chip voice record/playback solution**
  - No external ICs required
  - No development system required
- **High-quality, natural voice/audio reproduction**
- **Manual switch or microprocessor controllable**
  - Playback can be edge- or level-activated
- **Single-chip durations of 45, 60, 75, and 90 seconds**
- **Directly cascadable for longer durations**
- **Zero-power message storage**
  - Eliminates battery backup circuits
- **Automatic Power-Down (Push-Button Mode)**
  - 1 µA standby current (typical)
- **Fully addressable to handle multiple messages**
- **100-year message retention (typical)**
- **100K record cycles (typical)**
- **On-chip clock source**
- **On-chip Automatic Gain Control (AGC)**
- **Programmer support for play-only applications**
- **Single +5 volt supply (4.5 V to 6.5 V operating range)**
  - Low-voltage (3.6 V to 4.0 V) versions available
- **Available in die form, DIP, SOIC, and TSOP packaging**
- **Industrial-temperature (-40°C to 85°C) versions available**

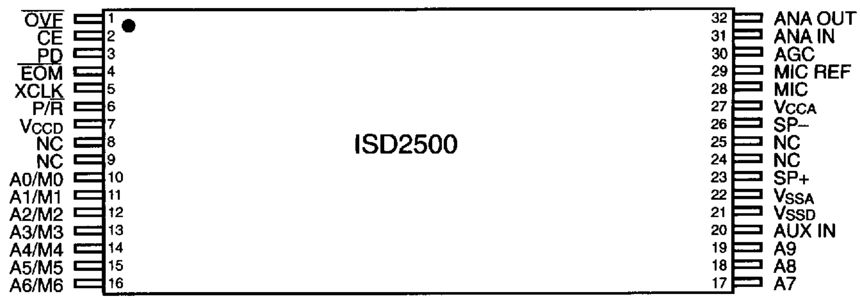
ISD2500-SERIES BLOCK DIAGRAM



ISD2500 SERIES PINOUTS



DIP/SOIC



TSOP

ISD2500 SERIES — DETAILED DESCRIPTIONS

Speech/Sound Quality

The ISD2500 Series includes devices offered at 5.3, 6.4, 8.0, and 10.6 KHz sampling frequencies, allowing the user a choice of speech quality options. The speech samples are stored directly into on-board non-volatile memory without the digitization and compression associated with other solutions. Direct analog storage provides a very true, natural sounding reproduction of voice, music, tones, and sound effects not available with most solid-state digital solutions.

Duration

To meet end system requirements, the ISD2500 Series offers single-chip solutions at 45, 60, 75, and 90 seconds. Parts may also be cascaded together for longer durations.

EEPROM Storage

One of the benefits of ISD's DAST technology is the use of on-board non-volatile memory, providing zero-power message storage. The message is retained for up to 100 years without power. In addition, the device can be re-recorded over 100,000 times.

Microcontroller Interface

In addition to its simplicity and ease of use, the ISD2500 Series includes all the interfaces necessary for microcontroller-driven applications. The address and control lines can be interfaced to a microcontroller and manipulated to perform a variety of tasks, including message assembly, message concatenation, predefined fixed message segmentation, and message management.

Programming

The ISD2500 Series is also ideal for playback-only applications, where single or multiple messages are referenced through buttons, switches, or a microcontroller. Once the desired message configuration is created, duplicates can easily be generated via an ISD programmer.

ISD2500 SERIES — PIN DESCRIPTIONS

Microphone Input (MIC)

The microphone input transfers its signal to the on-chip preamplifier. An on-board Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from -15 to 24 dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 K Ohm resistance on this pin, determines the low frequency cutoff for the ISD2500-Series passband.

Microphone Reference Input (MIC REF)

By connecting this pin to V_{SSA} (analog ground) via a series capacitor, common mode noise can be rejected at the preamplifier. The capacitor value should be exactly the same value as the input coupling capacitor used for microphone input. Using this approach may provide up to a 10 dB noise improvement. IF THIS INPUT IS UNUSED, IT MUST BE LEFT DISCONNECTED.

Analog Output (ANA OUT)

This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

Analog Input (ANA IN)

The analog input pin transfers its signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 3.0 KΩ input impedance of ANA IN, can be selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.

Automatic Gain Control Input (AGC)

The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of whispers to loud sounds to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C2 on the schematic on page 7) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R2) and an external capacitor (C2) connected in parallel between the AGC Pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 µF give satisfactory results in most cases.

Speaker Outputs (SP+/SP-)

All devices in the ISD2500 Series include an on-chip differential speaker driver, capable of driving 50 milliwatts into 16 Ω.

The speaker outputs are held at V_{SSA} levels during record and power down. It is therefore not possible to parallel speaker outputs of multiple ISD2500 devices or the outputs of other speaker drivers.

CONNECTION OF SPEAKER OUTPUTS IN PARALLEL MAY CAUSE DAMAGE TO THE DEVICE.

While a single output may be used alone (including a coupling capacitor between the SP pin and the speaker), the two opposite-polarity outputs used together yield a 4:1 improvement in output power.

NEVER GROUND OR DRIVE AN UNUSED SPEAKER OUTPUT.

Power Down Input (PD)

When not recording or playing back, the PD pin should be pulled HIGH to place the part in a very low power mode (see I_{SB} specification). When $\overline{OVF}$ pulses LOW for an overflow condition, PD should be brought HIGH to reset the address pointer back to the beginning of the Record/Playback space. The PD pin has additional functionality in the M6 (Push-Button) Operational Mode described later in the Operational Mode section.

Chip Enable Input ($\overline{CE}$)

The $\overline{CE}$ pin is taken LOW to enable all Playback and Record operations. The address inputs and Playback/Record input (P/$\overline{R}$) are latched by the falling edge of $\overline{CE}$. $\overline{CE}$ has additional functionality in the M6 (Push-Button) Operational Mode described later in the Operational Mode section.

Playback/Record Input (P/$\overline{R}$)

The P/$\overline{R}$ input is latched by the falling edge of the $\overline{CE}$ pin. A HIGH level selects a Playback cycle while a LOW level selects a Record cycle. For a Record cycle, the address inputs provide the starting address and recording continues until PD or $\overline{CE}$ is pulled HIGH or an overflow is detected (i.e. the chip is full). When a Record cycle is terminated by pulling PD or $\overline{CE}$ HIGH, an End-Of-Message ($\overline{EOM}$) marker is stored at the current address in memory. For a Playback cycle, the address inputs provide the starting address and the device will play until an $\overline{EOM}$ marker is encountered. The device can continue past an $\overline{EOM}$ marker in an operational mode, or if $\overline{CE}$ is held LOW in address mode. (See Table 1, Page 5 for more Operational Modes).

Address/Mode Inputs (Ax/Mx)

The Address/Mode Inputs have two functions depending on the level of the two Most Significant Bits (MSB) of the address.

If either of the two MSBs is LOW, the inputs are ALL interpreted as address bits and are used as the start address for the current Record or Playback cycle. The address pins are inputs only and do not output internal address information as the operation progresses. Address inputs are latched by the falling edge of $\overline{CE}$.

If both MSBs are HIGH, the Address/Mode Inputs are interpreted as Mode bits according to the Operational Mode Table 1 on page 4. There are six (6) operational modes (M0..M6) available as indicated on Table 1. It is possible to use multiple operational modes simultaneously. Operational Modes are sampled on EACH falling edge of $\overline{CE}$, and thus Operational Modes and direct addressing are mutually exclusive.

External Clock Input (XCLK)

The ISD2500 devices are configured at the factory with an internal sampling clock frequency centered to ±1 % of specification. The frequency is maintained to a total variation of ±2.25 % over the entire commercial temperature and operating voltage ranges. If greater precision is required, the device can be clocked through the XCLK pin as follows:

Part Number	Sample Rate	Required Clock
ISD2590	5.33 KHz	682.7 KHz
ISD2575	6.4 KHz	819.2 KHz
ISD2560	8.0 KHz	1024 KHz
ISD2545	10.6 KHz	1365.3 KHz

These recommended clock rates should not be varied because the anti-aliasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two. IF THE XCLK IS NOT USED, THIS INPUT MUST BE CONNECTED TO GROUND.

ISD2500 SERIES — PIN DESCRIPTIONS, CONT.

End-Of-Message / RUN Output ($\overline{EOM}$)

A non-volatile marker is automatically inserted at the end of each recorded message. It remains there until the message is recorded over. The $\overline{EOM}$ output pulses LOW for a period of T_{EOM} at the end of each message.

In addition, the ISD2500 Series has an internal V_{CC} detect circuit to maintain message integrity should V_{CC} fall below 3.5V. In this case, $\overline{EOM}$ goes LOW and the device is fixed in Playback-only mode.

When the device is configured in Operational Mode M6 (Push-Button Mode), this pin provides an active-HIGH RUN signal, indicating the device is currently recording or playing. This signal can conveniently drive an LED for a visual indicator of a Record or Playback operation in process.

Overflow Output ($\overline{OVF}$)

This signal pulses LOW at the end of memory space, indicating the device has been filled and the message has overflowed. The $\overline{OVF}$ output then follows the $\overline{CE}$ input until a PD pulse has reset the device. This pin can be used to cascade several ISD2500 devices together to increase Record/Playback durations.

Auxiliary Input (AUX IN)

The Auxiliary Input is multiplexed through to the output amplifier and speaker output pins when $\overline{CE}$ is HIGH and Playback has ended, or if the device is in overflow. When cascading multiple ISD2500 devices, the AUX IN pin is used to connect a Playback signal from a following device to the previous output speaker drivers. For noise considerations, it is suggested that the auxiliary input not be driven when the storage array is active.

Voltage Inputs (V_{CCA}, V_{CCD})

To minimize noise, the analog and digital circuits in the ISD2500 Series devices use separate power busses. These +5 V busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.

Ground Inputs (V_{SSA}, V_{SSD})

The ISD2500 Series of devices utilizes separate analog and digital ground busses. These pins should be tied together as close to the package as possible and connected through a low-impedance path to power supply ground.

OPERATIONAL MODES

The ISD2500 Series is designed with several built-in operational modes provided to allow maximum functionality with a minimum of additional components. These are described in detail below. The operational modes use the address pins on the ISD2500 devices, but are mapped outside the valid address range. When the two Most Significant Bits (MSBs) are HIGH, the remaining address signals are interpreted as mode bits and NOT as address bits. Therefore, operational modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using operational modes. First, all operations begin initially at address 0, which is the beginning of the ISD2500 address space. Later operations can begin at other address locations, depending on the operational mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from Record to Playback, Playback to Record (except M6 mode), or when a Power-Down cycle is executed.

Second, Operational Modes are executed when $\overline{CE}$ goes LOW and the two MSBs are HIGH. This Operational Mode remains in effect until the next LOW-going $\overline{CE}$ signal, at which point the current address/mode levels are sampled and executed.

OPERATIONAL MODE DESCRIPTIONS

The Operational Modes can be used in conjunction with a microcontroller, or they can be hard-wired to provide the desired system operation.

TABLE 1. OPERATIONAL MODES

Mode Control	Function	Typical Use	Jointly* Compatible
M0	Message cueing	Fast-forward through messages	M4, M5, M6
M1	Delete $\overline{EOM}$ markers	Position $\overline{EOM}$ marker at the end of the last message	M3, M4, M5, M6
M2	Not applicable	Reserved	N/A
M3	Looping	Continuous playback from address 0	M1, M5, M6
M4	Consecutive addressing	Record/Play multiple consecutive messages	M0, M1, M5
M5	$\overline{CE}$ level-activated	Allows message pausing	M0, M1, M3, M4
M6	Push-button control	Simplified device interface	M0, M1, M3

* *Indicates additional operational modes which can be used simultaneously with the given mode.*

M0 — Message Cueing

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each $\overline{\text{CE}}$ LOW pulse causes the internal address pointer to skip to the next message. This mode should be used for Playback only, and is typically used with the M4 Operational Mode.

M1 — Delete $\overline{\text{EOM}}$ Markers

The M1 Operational Mode allows sequentially recorded messages to be concatenated into a single message with only one $\overline{\text{EOM}}$ marker set at the end of the combined message. When this operational mode is configured, messages recorded sequentially are played back as one continuous message.

M2 — Unused

When operational modes are selected, the M2 pin should be LOW.

M3 — Message Looping

The M3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space. A message CAN completely fill the ISD2500 device and will loop from beginning to end without $\overline{\text{OVF}}$ going LOW.

M4 — Consecutive Addressing

During normal operations, the address pointer will reset when a message is played through to an $\overline{\text{EOM}}$ marker. The M4 Operational Mode inhibits the address pointer reset on $\overline{\text{EOM}}$, allowing messages to be played back consecutively.

M5 — $\overline{\text{CE}}$ Level Activated

The default mode for ISD2500 devices is for $\overline{\text{CE}}$ to be edge-activated on Playback and level-activated on Record. The M5 Operational Mode causes the $\overline{\text{CE}}$ pin to be interpreted as level-activated as opposed to edge-activated during Playback. This is specifically useful for terminating Playback operations using the $\overline{\text{CE}}$ signal.

In this mode, $\overline{\text{CE}}$ LOW begins a Playback cycle, $\overline{\text{CE}}$ HIGH stops the cycle, and $\overline{\text{CE}}$ LOW again will begin playing at the point where the message was stopped without resetting the address pointer.

M6 — Push-Button Mode

The ISD2500 Series of devices contain a push-button operational mode. The push-button mode is used primarily in very low-cost applications and is designed to minimize external circuitry and components, thereby reducing system cost. In order to configure the device in push-button operational mode, the two most significant address bits (pins 9 and 10) must be HIGH, and the M6 mode pin (pin 7) must also be HIGH. A device in this mode always powers down at the end of each Playback or Record cycle after $\overline{\text{CE}}$ goes HIGH.

When this operational mode is implemented, several of the pins on the device have alternate functionality:

Pin Name	Alternate Functionality in Push-Button Mode
Pin 23, $\overline{\text{CE}}$	Start/Pause Push-Button (LOW Pulse-Activated)
Pin 24, PD	Stop/Reset Push-Button (HIGH Pulse-Activated)
Pin 25, $\overline{\text{EOM}}$	Active-HIGH Run Indicator

Pin 23: $\overline{\text{CE}}$ (Start/Pause)

In push-button Operational Mode, $\overline{\text{CE}}$ acts as a LOW-going pulse-activated Start/Pause signal. If no operation is currently in progress, a LOW-going pulse on this signal will initiate a Playback or a Record cycle according to the level on the P/$\overline{\text{R}}$ pin. A subsequent pulse on the $\overline{\text{CE}}$ pin, before an End-Of-Message is reached in Playback or an overflow condition occurs, will cause the device to pause. The address counter is not reset, and another $\overline{\text{CE}}$ pulse will cause the device to continue the operation from the place where it was paused.

Pin 24: PD (Stop/Reset)

In push-button Operational Mode, PD acts as a HIGH-going pulse-activated Stop/Reset signal. When a Playback or Record cycle is in progress and a HIGH-going pulse is observed on PD, the current cycle is terminated and the address pointer is reset to address 0, the beginning of the message space.

Pin 25: $\overline{\text{EOM}}$ (Run)

In push-button Operational Mode, $\overline{\text{EOM}}$ becomes an active-HIGH run signal which can be used to drive an LED or other external device. It is HIGH whenever a Record or Playback operation is in progress.

Recording in Push-Button Mode

1) The PD pin should be LOW, usually using a pulldown resistor.
2) The P/$\overline{\text{R}}$ pin is taken LOW.
3) The $\overline{\text{CE}}$ pin is pulsed LOW. Recording starts, $\overline{\text{EOM}}$ goes HIGH to indicate an operation in progress.
4) The $\overline{\text{CE}}$ pin is pulsed LOW. Recording pauses, $\overline{\text{EOM}}$ goes back LOW. The internal address pointers are not

OPERATIONAL MODE DESCRIPTIONS, CONT.

cleared, but an $\overline{EOM}$ marker is stored in memory to point to the message end. The P/$\overline{R}$ pin may be taken HIGH at this time. Any subsequent $\overline{CE}$ would start a playback at address 0.

5) The $\overline{CE}$ pin is pulsed LOW. Recording starts at the next address after the previous set $\overline{EOM}$ marker. $\overline{EOM}$ goes back HIGH. (Note: if the M1 operational mode pin is also HIGH, the just previously written $\overline{EOM}$ bit is erased, and recording starts at that address.)

6) When the recording sequences are finished, the final $\overline{CE}$ pulse LOW will end the last Record cycle, leaving a set $\overline{EOM}$ marker at the message end. Recording may also be terminated by a HIGH level on PD, which will leave a set $\overline{EOM}$ marker.

Playback in Push-Button Mode

1) The PD pin should be LOW.

2) The P/$\overline{R}$ pin is taken HIGH.

3) The $\overline{CE}$ pin is pulsed LOW. Playback starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.

4) If the $\overline{CE}$ pin is pulsed LOW or an $\overline{EOM}$ marker is encountered during an operation, the part will pause. The internal address pointers are not cleared, and $\overline{EOM}$ goes back LOW. The P/$\overline{R}$ pin may be changed at this time. A subsequent Record operation would not reset the address pointers and the recording would begin where Playback ended.

5) $\overline{CE}$ is again pulsed LOW. Playback starts where it left off, with $\overline{EOM}$ going HIGH to indicate an operation in progress.

6) Playback continues as in 4) and 5) until PD is pulsed HIGH or overflow occurs.

7) If in overflow, pulling $\overline{CE}$ LOW will reset the address pointer and start Playback from the beginning. After a PD pulse, the part is reset to address 0.

Note : Push-button mode can be used in conjunction with modes M0, M1, and M3.

ISD1000A COMPATIBILITY

The ISD2500 Series of devices is designed to provide upward compatibility from the ISD1000A family. When designing with the ISD2500 Series, the following differences should be noted.

Addressing

The ISD2500-Series devices have 480 K storage cells designed to provide 60 seconds of storage at a sampling rate of 8.0 KHz. This is approximately four times the storage of the ISD1000A family. To enable the same addressing resolution, two additional address pins have been added. The address space of each device is divisible into 600 increments with valid addressing from 00 to 257 Hex. Some higher addresses are mapped into the Operational Modes. All other addresses are invalid.

Overflow

The ISD1000A family combined two functions on the $\overline{EOM}$ pin: end-of-message indication and overflow. The ISD2500 Series separates these two functions. Pin 25 remains as $\overline{EOM}$, but outputs only the $\overline{EOM}$ signal indication. Pin 22 becomes $\overline{OVF}$ and pulses LOW only when the device reaches its end of memory, or is "full." This change allows easy message cueing and addressability across device boundaries. This also means that the M2 operational mode found in the ISD1000A family is not implemented in the ISD2500 Series.

Push-Button Mode

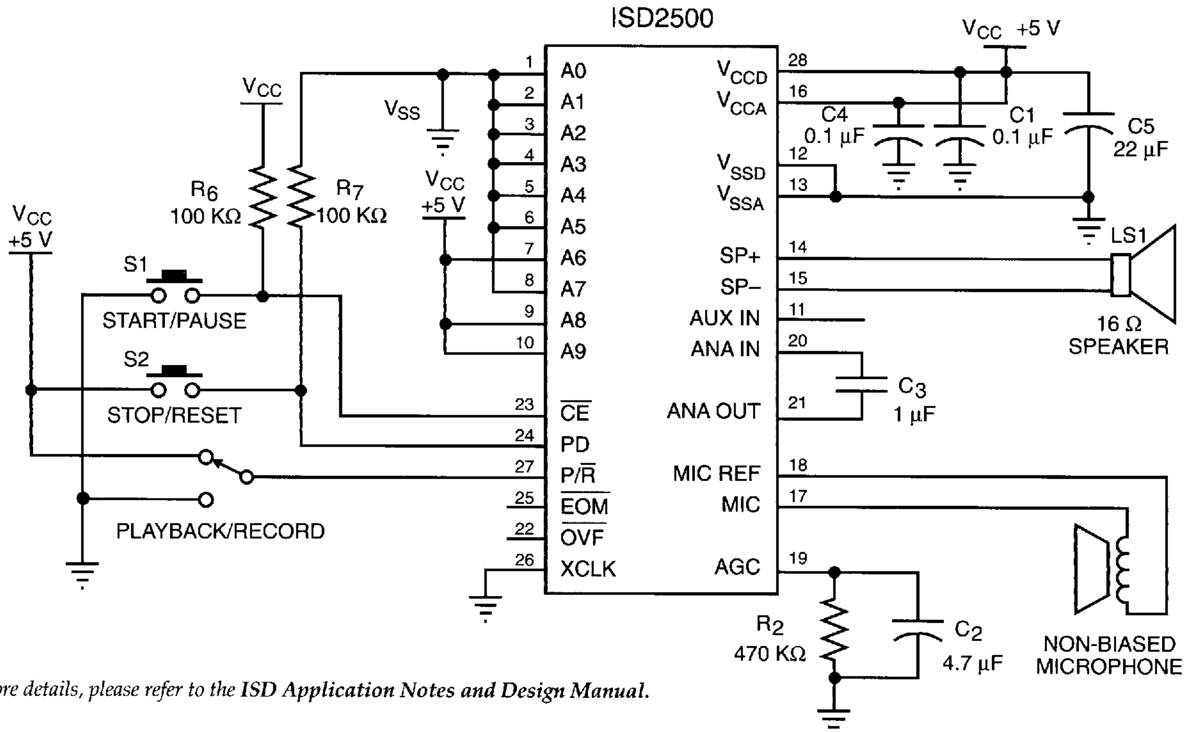
The ISD2500 Series includes an additional Operational Mode called Push-Button mode. This provides an alternative interface to the Record and Playback functions of the part. The $\overline{CE}$ and PD pins become redefined as edge-activated "push-buttons." A pulse on $\overline{CE}$ initiates a cycle, and if triggered again, pauses the current cycle without resetting the address pointer (i.e., a Start or Pause function). PD stops any current cycle and resets the address pointer to the beginning of the message space (i.e., a Stop and Reset function). Additionally, the $\overline{EOM}$ pin functions as an active-HIGH run indicator, and can be used to drive an LED indicating a Record or Playback operation is in progress. Devices in the Push-Button mode cannot be cascaded.

Looping Mode

The ISD2500 Series can loop with a message that completely fills the memory space.

Note: *Additional descriptions of ISD1000A device functionality and application examples are provided in the ISD **Application Notes and Design Manual**.*

APPLICATION EXAMPLE – PUSH-BUTTON



For more details, please refer to the ***ISD Application Notes and Design Manual.***

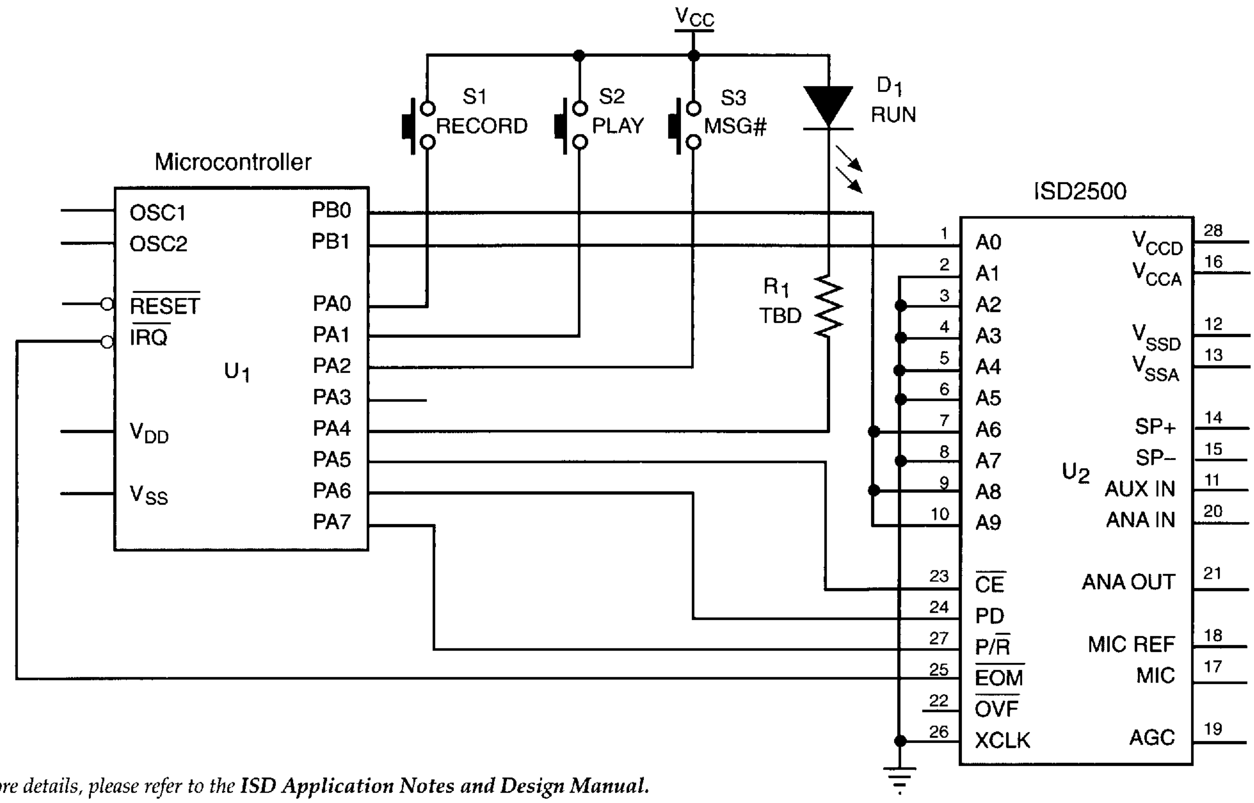
APPLICATION EXAMPLE – PUSH-BUTTON CONTROL

Control Step	Function	Action
1	Select record/playback mode	P/$\overline{R}$ = As desired
2A	Begin playback	P/$\overline{R}$ = HIGH $\overline{CE}$ = Pulsed LOW
2B	Begin record	P/$\overline{R}$ = LOW $\overline{CE}$ = Pulsed LOW
3	Pause record or playback	$\overline{CE}$ = Pulsed LOW
4A	End playback	Automatic at $\overline{EOM}$ marker or PD Pulsed HIGH
4B	End record	PD = Pulsed HIGH

APPLICATION EXAMPLE – PASSIVE COMPONENT FUNCTIONS

Part	Function	Comments
R2	Release time constant	Sets release time for AGC
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff
R6, R7	Pull-up and pull-down resistors	Defines static state of inputs
C1, C4 C5	Power supply capacitors	Filters and bypass of power supply

APPLICATION EXAMPLE – MICROCONTROLLER/ISD2500 INTERFACE

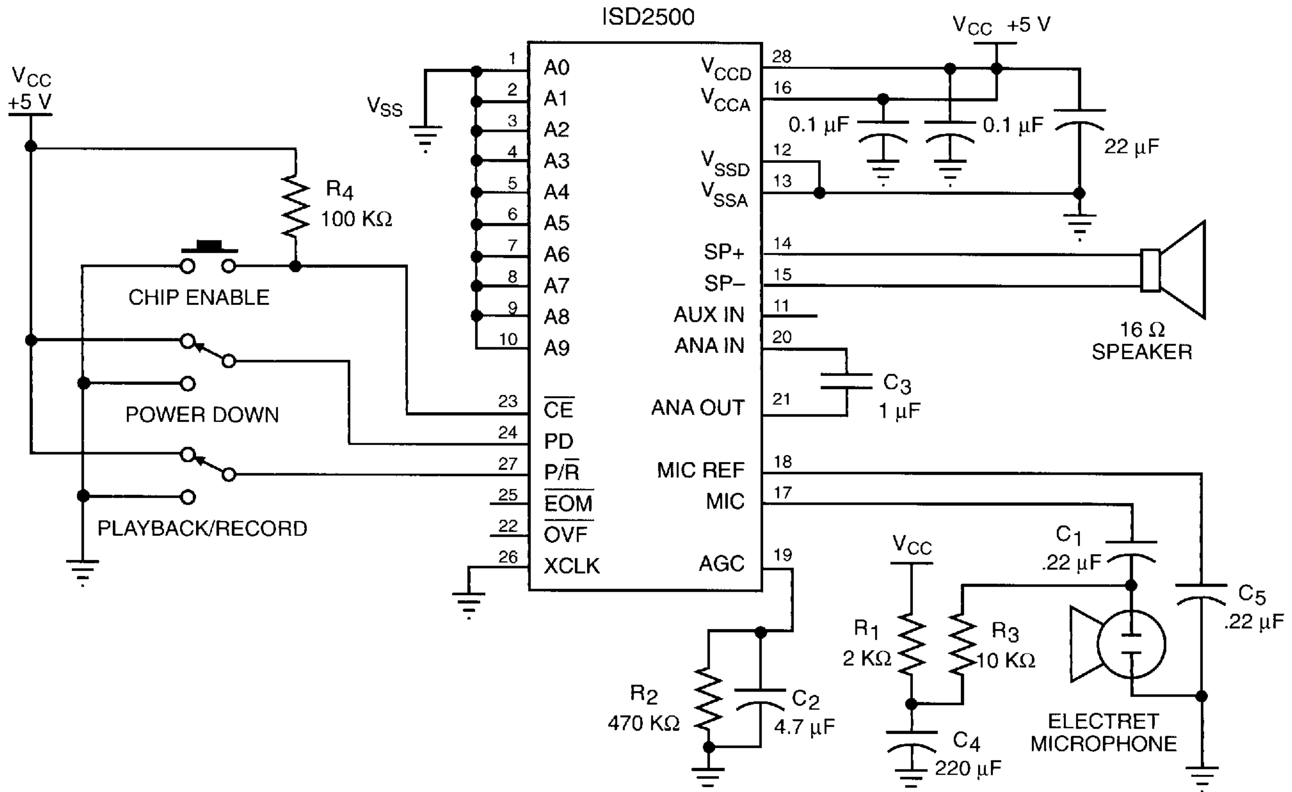


For more details, please refer to the ***ISD Application Notes and Design Manual.***

EXPLANATION

In this simplified block diagram of a microcontroller application, the Push-Button mode and message cueing are used. The microcontroller is a 16-pin version with enough port pins for buttons, an LED, and the ISD2500-Series device. The software can be written to use three buttons: one each for play and record, and one for message selection. Because the microcontroller is interpreting the buttons and commanding the ISD2500 device, software can be written for any functions desired in a particular application.

APPLICATION EXAMPLE – DESIGN SCHEMATIC



Note: If desired, pin 18 may be left unconnected (microphone preamplifier noise will be higher). In this case, pin 18 must not be tied to any other signal or voltage. For more details, please refer to the ***ISD Application Notes and Design Manual.***

APPLICATION EXAMPLE – BASIC DEVICE CONTROL

Control Step	Function	Action
1	Power up chip and select record/playback mode	1. PD = LOW 2. P/$\overline{R}$ = As desired
2	Set message address for record/playback	Set addresses A0–A7
3A	Begin playback	P/$\overline{R}$ = HIGH $\overline{CE}$ = Pulsed LOW
3B	Begin record	P/$\overline{R}$ = LOW $\overline{CE}$ = LOW
4A	End playback	Automatic
4B	End record	PD or $\overline{CE}$ = HIGH

APPLICATION EXAMPLE – PASSIVE COMPONENT FUNCTIONS

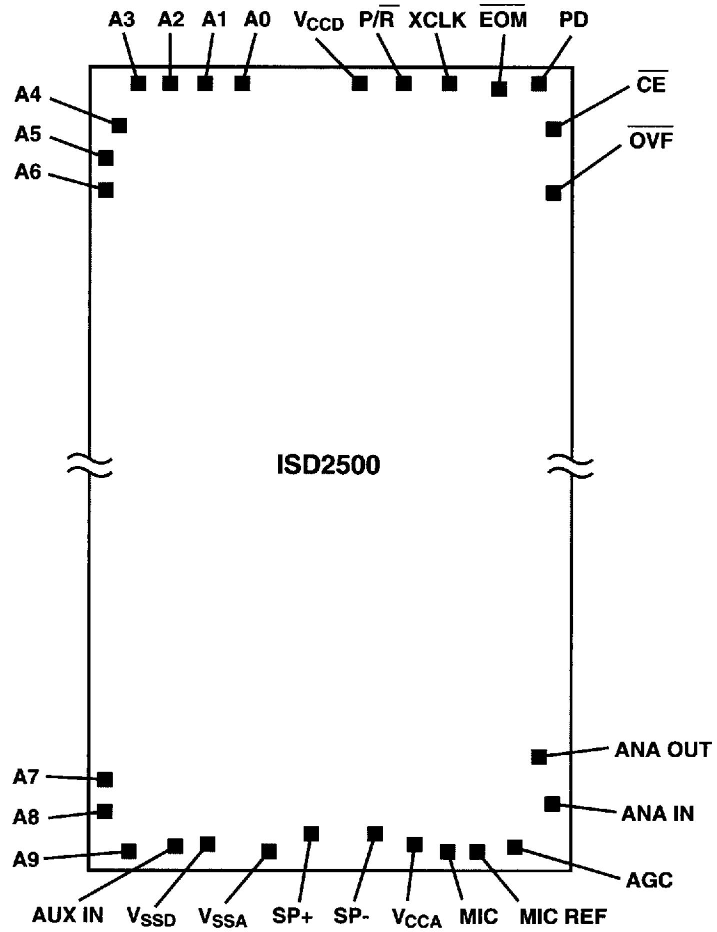
Part	Function	Comments
R1	Microphone power supply decoupling	Reduces power supply noise
R2	Release time constant	Sets release time for AGC
R3	Microphone biasing resistor	Provides biasing for microphone operation
C1	Microphone DC–blocking capacitor. Low-frequency cutoff	Decouples microphone bias from chip. Provides single-pole low-frequency cutoff
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff
C4	Microphone power supply decoupling network	Reduces power supply noise
C5	Common-mode capacitor	Provides common-mode noise rejection

DIE BONDING PHYSICAL LAYOUT

I. **Die Dimensions**
X: 187 ±1 mils
Y: 399 ±1 mils

II. **Die Thickness**
21 mils

III. **Pad Opening**
109 microns (4.3 mils)



PIN/PAD DESIGNATIONS

Pin	Pin Name	X Axis	Y Axis	Pin	Pin Name	X Axis	Y Axis
A0	Address 0	-1148.9	4898.2	SP–	Speaker Output –	425.6	-4790.8
A1	Address 1	-1406.9	4898.2	V_{CCA}	V_{CC} Analog Power Supply	865.1	-4848.3
A2	Address 2	-1661.9	4898.2	MIC	Microphone Input	1320.7	-4897.3
A3	Address 3	-1916.9	4898.2	MIC REF	Microphone Reference	1605.1	-4897.3
A4	Address 4	-2069.9	4608.2	AGC	Automatic Gain Control	1877.6	-4871.3
A5	Address 5	-2194.9	4358.2	ANA IN	Analog Input	2202.11	-4269.8
A6	Address 6	-2194.9	4108.2	ANA OUT	Analog Output	2123.1	-3910.8
A7	Address 7	-2194.9	-4212.3	$\overline{OVF}$	Overflow Output	2142.6	4154.7
A8	Address 8	-2194.9	-4456.3	$\overline{CE}$	Chip Enable Input	2202.1	4558.7
A9	Address 9	-2076.4	-4897.3	PD	Power Down Input	2048.1	4898.2
AUX IN	Auxilary Input	-1607.9	-4868.3	$\overline{EOM}$	End of Message	1648.1	4865.7
V_{SSD}	V_{SS} Digital Power Supply	-1343.9	-4850.8	XCLK	External Clock	1221.1	4898.2
V_{SSA}	V_{SS} Analog Power Supply	-551.9	-4884.8	P/$\overline{R}$	Playback/Record	965.6	4898.2
SP+	Speaker Output +	-111.4	-4790.8	V_{CCD}	V_{CC} Digital Power Supply	646.1	4895.7

ABSOLUTE MAXIMUM RATINGS

Condition	Value
Temperature under bias	–65° C to +125° C
Storage temperature range	–65° C to +150° C
Voltage applied to any pin	(V_{SS} - 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ± 20 mA)	(V_{SS} - 1.0 V) to (V_{CC} + 1.0 V)
Lead temperature (soldering – 10 seconds)	300° C
V_{CC} - V_{SS}	- 0.3 V to + 7.0 V

Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

DC PARAMETERS

Operating Conditions: T_A = 0° C to 70° C [(4)], V_{CC} = 4.5 V to 6.5 V [(5)], V_{SS} = 0 V [(6)]; unless otherwise noted

Symbol	Parameters	Min	Typ [(1)]	Max	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	V_{CC} – 0.4			V	I_{OH} = - 10 µA
V_{OH1}	$\overline{OVF}$ Output High Voltage	2.4			V	I_{OH} = - 1.6 mA
V_{OH2}	$\overline{EOM}$ Output High Voltage		V_{CC} – 1.0		V	I_{OH} = - 3.2 mA
I_{CC}	V_{CC} Current (Operating)		25	30	mA	$R_{EXT} = \infty$ [(7)]
I_{SB}	V_{CC} Current (Standby)		1	10	µA	[(7)]
I_{IL}	Input Leakage Current			±1	µA	
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance		10		KΩ	Pins 17, 18
R_{AUX}	Aux Input Resistance		10		KΩ	
$R_{ANA\ IN}$	Ana In Input Resistance		3.0		KΩ	
A_{PRE1}	Preamp Gain 1		24		dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		-15	5	dB	AGC = 2.5 V
A_{AUX}	Aux In/SP+ Gain		0.98	1.0	V/V	
A_{ARP}	Ana In to SP+/-		22		dB	
R_{AGC}	AGC Output Resistance		5		KΩ	

Notes: 1. Typical values @ T_A = 25° C and 5.0 V.
2. With 12 KΩ series resistor at ANA IN.
3. Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).
4. Case temperature.
5. $V_{CC} = V_{CCA} = V_{CCD}$.
6. $V_{SS} = V_{SSA} = V_{SSD}$.
7. V_{CCA} and V_{CCD} connected together.

AC PARAMETERS

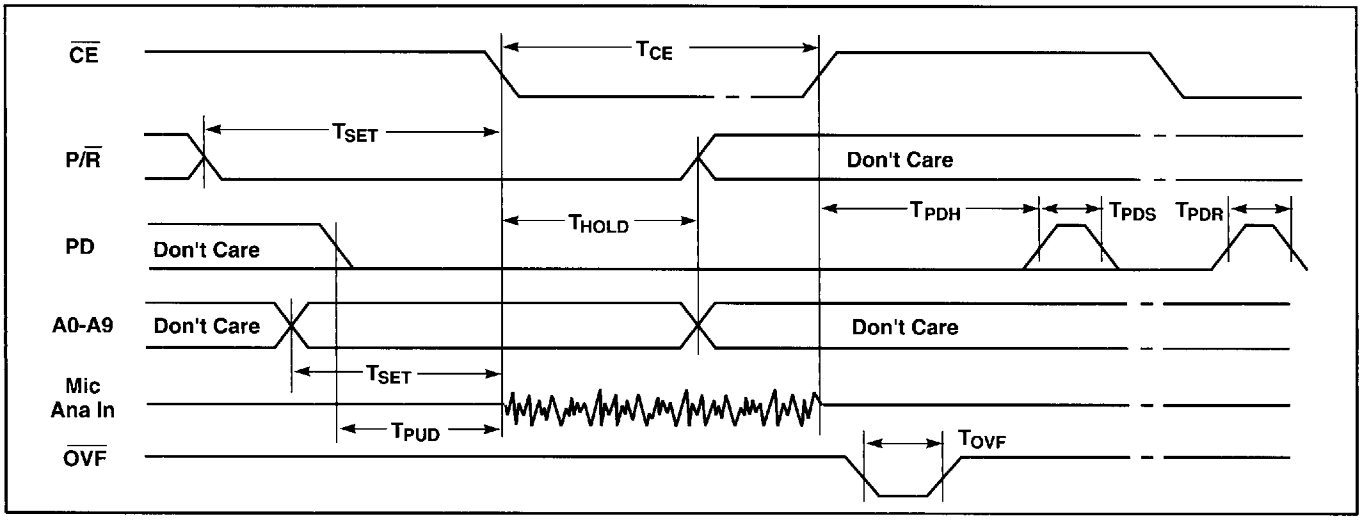
Operating Conditions: $T_A = 0°$ C to 70° C [4], $V_{CC} = 4.5$ V to 6.5 V [5], $V_{SS} = 0$ V [6]; unless otherwise noted

Symbol	Characteristic	Min	Typ [1]	Max	Units	Conditions
THD	Total Harmonic Distortion		1		%	@ 1 KHz [2]
P_{OUT}	Speaker Output Power		12.2	50	mW	$R_{EXT} = 16\ \Omega$ [8]
V_{OUT}	Voltage Across Speaker Pins			2.5	V p-p	$R_{EXT} = 600\ \Omega$
V_{IN1}	Mic Input Voltage			20	mV	Peak-to-Peak [2]
V_{IN2}	Ana In Input Voltage			50	mV	Peak-to-Peak
V_{IN3}	Aux In Input Voltage			1.25	V	Peak-to-Peak; $R_{EXT} = 16\ \Omega$
T_{SET}	Control/Address Setup Time		300		nsec	
T_{HOLD}	Control/Address Hold Time		0		nsec	
T_{CE}	$\overline{CE}$ Pulse Width		100		nsec	
T_{PUD}	Power-Up Delay – ISD2545 – ISD2560 – ISD2575 – ISD2590		18.75 25 31.25 37.5		msec msec msec msec	
T_{EOM}	$\overline{EOM}$ Pulse Width – ISD2545 – ISD2560 – ISD2575 – ISD2590		9.375 12.5 15.625 18.75		msec msec msec msec	
T_{PDR}	PD Pulse Width Record – ISD2545 – ISD2560 – ISD2575 – ISD2590		18.75 25 31.25 37.5		msec msec msec msec	
T_{PDP}	PD Pulse Width Play – ISD2545 – ISD2560 – ISD2575 – ISD2590		9.375 12.5 15.625 18.75		msec msec msec msec	
T_{PDS} [9]	PD Pulse Width Static		100		nsec	
T_{PDH}	Power Down Hold		0		nsec	
T_{OVF}	Overflow Pulse Width		10		µsec	

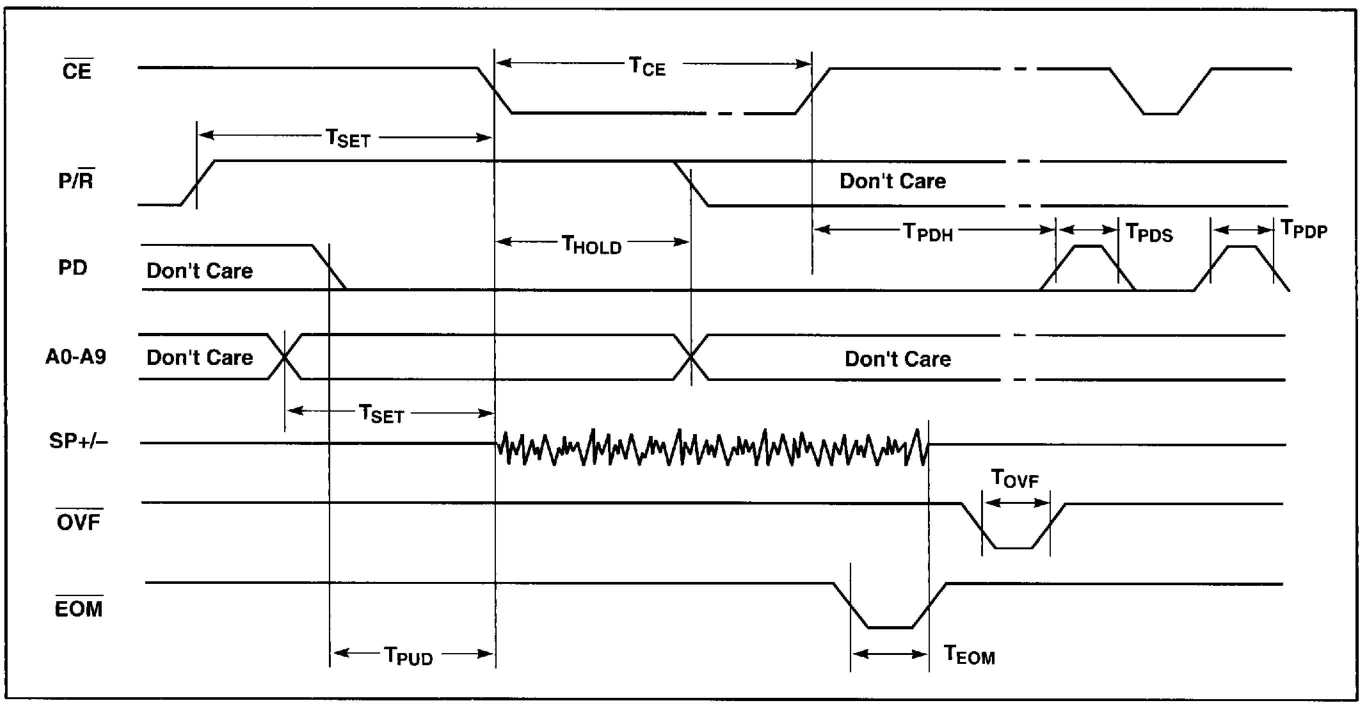
Notes: 1. Typical values @ $T_A = 25°$ C and 5.0 V.
2. With 12 KΩ series resistor at ANA IN. Required for 6.5 V operation to minimize distortion.
3. Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).
4. Case temperature.
5. $V_{CC} = V_{CCA} = V_{CCD}$.
6. $V_{SS} = V_{SSA} = V_{SSD}$.
7. V_{CCA} and V_{CCD} connected together.
8. From AUX IN; if ANA IN is driven at 50 mV p-p, the $P_{OUT} = 12.2$ mW, typical.
9. T_{PDS} is required during a static condition, typically overflow.

TIMING DIAGRAMS (ISD2500 SERIES)

RECORD



PLAYBACK



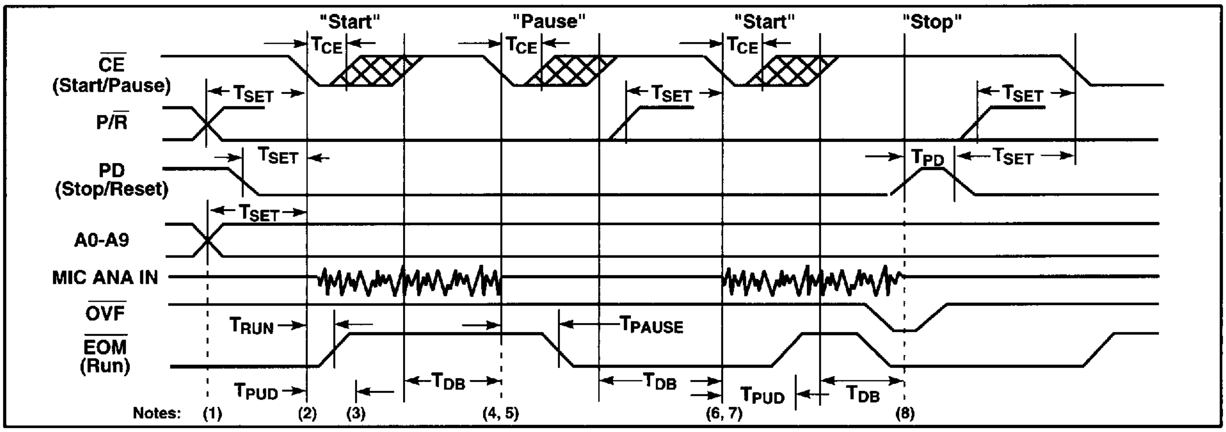
PUSH-BUTTON AC PARAMETERS

Symbol	Characteristic	Min	Typ (1)	Max	Units	Conditions
T_{CE}	$\overline{CE}$ Pulse Width [Start/Pause]		300		nsec	
T_{SET}	Control/Address Setup Time		300		nsec	
T_{PUD}	Power-Up Delay – ISD2545 – ISD2560 – ISD2575 – ISD2590		18.75 25 31.25 37.25		msec msec msec msec	
T_{PD}	PD Pulse Width [Stop/Reset]		300		nsec	
T_{RUN}	$\overline{CE}$ to $\overline{EOM}$ HIGH	25		400	nsec	
T_{PAUSE}	$\overline{CE}$ to $\overline{EOM}$ LOW	50		400	nsec	
T_{DB}	$\overline{CE}$ HIGH Debounce – ISD2545 – ISD2560 – ISD2575 – ISD2590	50 70 85 105		80 105 135 160	msec msec msec msec	

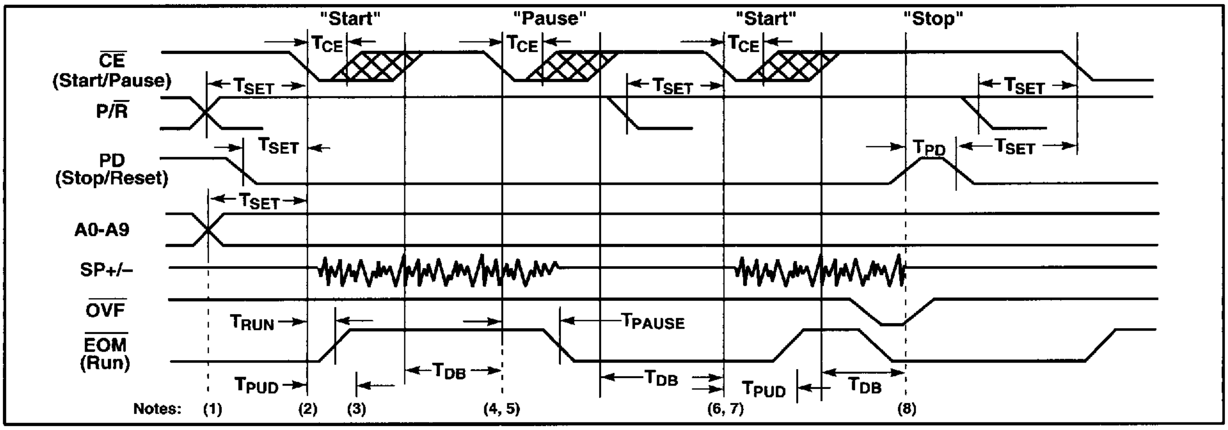
Notes: 1. Typical values @ T_A = 25° C and 5.0 V.

TIMING DIAGRAMS (ISD2500 SERIES)

PUSH-BUTTON MODE RECORD



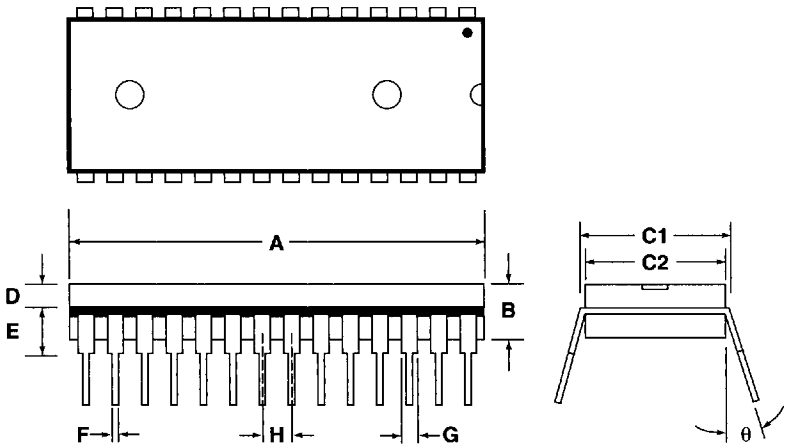
PUSH-BUTTON MODE PLAYBACK



Notes:
1. *A9, A8, and A6 = 1 for push-button operation.*
2. *The first $\overline{CE}$ LOW pulse performs a Start function.*
3. *The part will begin to play or record after a power-up delay T_{PUD}.*
4. *The part must have $\overline{CE}$ HIGH for a debounce period T_{DB} before it will recognize another falling edge of $\overline{CE}$ and pause.*
5. *The second $\overline{CE}$ LOW pulse, and every even pulse thereafter, performs a Pause function.*
6. *Again, the part must have $\overline{CE}$ HIGH for a debounce period T_{DB} before it will recognize another falling edge of $\overline{CE}$, which would restart an operation. In addition, the part will not do an internal power down until $\overline{CE}$ is HIGH for the T_{DB} time.*
7. *The third $\overline{CE}$ LOW pulse, and every odd pulse thereafter, performs a Resume function.*
8. *At any time, a HIGH level on PD will stop the current function, reset the address counter, and power down the device.*

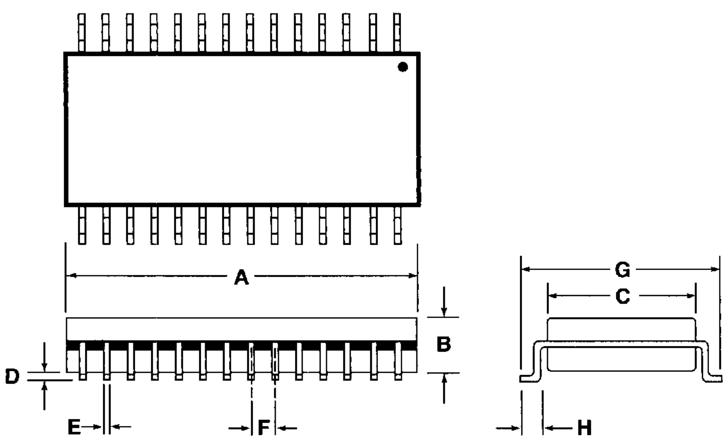
PACKAGE DIAGRAMS

28-Lead Plastic Dual In-Line Package (DIP) Type P



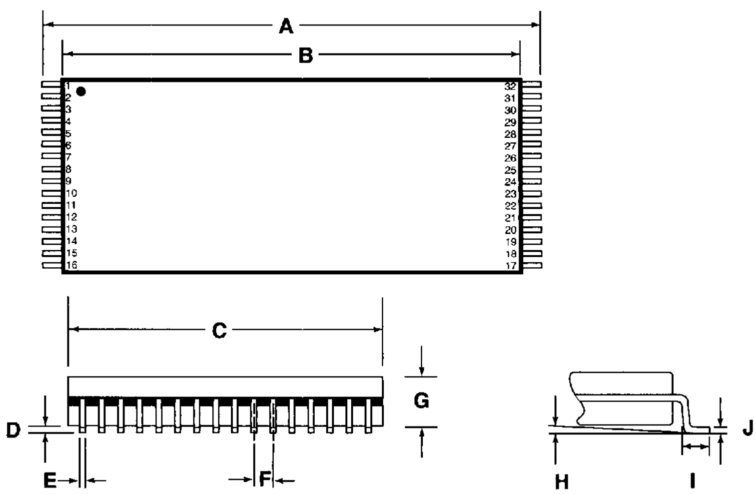
	INCHES Min	INCHES Nom	INCHES Max	MILLIMETERS Min	MILLIMETERS Nom	MILLIMETERS Max
A	1.445	1.450	1.455	36.7	36.83	36.95
B		.150			3.89	
C1	.600		.625	15.24		15.88
C2	.530	.540	.550	13.46	13.72	13.97
D	1.25	1.30	1.35	2.92	3.05	3.18
E	.125	.130	.135	3.18		3.43
F	.015	.018	.022	0.38	0.46	0.56
G	.055	.060	.065	1.40	1.52	1.65
H		.100			2.54	
θ	0°	7°	15°	0°	7°	15°

28-Lead Plastic Small Outline Package (SOIC) Type J



	INCHES Min	INCHES Nom	INCHES Max	MILLIMETERS Min	MILLIMETERS Nom	MILLIMETERS Max
A	.706	.714	.718	17.93	18.14	18.24
B	.086	.088	.090	2.18	2.24	2.29
C	.340	.346	.350	8.64	8.79	8.89
D	.004	.007	.010	.102	.178	.254
E	.014	.016	.020	.360	.410	.480
F		.050			1.27	
G	.463	.470	.477	11.76	12.00	12.12
H	.020	.031	.042	.510	.790	1.07

32-Lead Thin Plastic Small-Outine Package (TSOP) Type I



	INCHES Min	INCHES Nom	INCHES Max	MILLIMETERS Min	MILLIMETERS Nom	MILLIMETERS Max
A	.780	.790	.795	19.80	20.00	20.20
B	.720	.724	.728	18.30	18.40	18.50
C	.307	.315	.323	7.80	8.00	8.20
D	.000	.003	.006	0.00	0.08	0.15
E	.006	.008	.010	0.15	0.20	0.25
F		.0197			0.50	
G	.037	.039	.041	0.95	1.00	1.05
H	0°	3°	5°	0°	3°	5°
I	.016	.020	.024	0.40	0.50	0.60
J	.004	.006	.008	0.10	0.15	0.20

ORDERING INFORMATION

When placing an order for the ISD2500 Series devices, please refer to the following part numbers:

Part No.	Rec/Play Duration	Description
ISD2545P	45 sec.	28-pin plastic dual in-line package (DIP)
ISD2545G	45 sec.	28-lead small-outline integrated circuit (SOIC)
ISD2560P	60 sec.	28-pin plastic dual in-line package (DIP)
* ISD2560PI	60 sec.	Industrial Temperature, -40°C to 85°C (DIP)
* ISD2560PL	60 sec.	Low Voltage, 3.6 V to 4.0 V (DIP)
ISD2560G	60 sec.	28-lead small-outline integrated circuit (SOIC)
* ISD2560GI	60 sec.	Industrial Temperature, -40°C to 85°C (SOIC)
* ISD2560GL	60 sec.	Low Voltage, 3.6 V to 4.0 V (SOIC)
* ISD2560GLI	60 sec.	Low Voltage, Industrial Temperature (SOIC)
ISD2560T	60 sec.	32-lead thin small-outline package (TSOP)
* ISD2560TI	60 sec.	Industrial Temperature, -40°C to 85°C (TSOP)
* ISD2560TL	60 sec.	Low Voltage, 3.6 V to 4.0 V (TSOP)
* ISD2560TLI	60 sec.	Low Voltage, Industrial Temperature (TSOP)
ISD2560X	60 sec.	Bare unpackaged die

Part No.	Rec/Play Duration	Description
ISD2575P	75 sec.	28-pin plastic dual in-line package (DIP)
*ISD2575PI	75 sec.	Industrial Temperature, -40°C to 85°C (DIP)
*ISD2575PL	75 sec.	Low Voltage, 3.6 V to 4.0 V (DIP)
ISD2575G	75 sec.	28-lead small-outline integrated circuit (SOIC)
*ISD2575GI	75 sec.	Industrial Temperature, -40°C to 85°C (SOIC)
*ISD2575GL	75 sec.	Low Voltage, 3.6 V to 4.0 V (SOIC)
*ISD2575GLI	75 sec.	Low Voltage, Industrial Temperature (SOIC)
ISD2575T	75 sec.	32-lead thin small-outline package (TSOP)
*ISD2575TI	75 sec.	Industrial Temperature, -40°C to 85°C (TSOP)
*ISD2575TL	75 sec.	Low Voltage, 3.6 V to 4.0 V (TSOP)
*ISD2575TLI	75 sec.	Low Voltage, Industrial Temperature (TSOP)
ISD2575X	75 sec.	Bare unpackaged die
ISD2590P	90 sec.	28-pin plastic dual in-line package (DIP)
ISD2590G	90 sec.	28-lead small-outline integrated circuit (SOIC)
ISD2590X	90 sec.	Bare unpackaged die

** Please contact ISD Sales Offices or Representatives for "L" and/or "I" product availability and specifications.*

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