



14- AND 16-BIT TRACKING S/D CONVERTERS

FEATURES

DESCRIPTION

The SDC-14570/75 Series are small low cost synchro- or resolver-to-digital converters based upon a single chip monolithic. A completely self-contained 14- or 16-bit synchro converter is housed in the SDC-14570/75 Series small 1.0" x 0.8" package. The SDC-14570 is fixed at 14 bits, the SDC-14575 is pin-programmable 14 or 16 bits.

The velocity output (VEL) from the SDC-14570/75 Series, which can be used to replace a tachometer, is a 4 V signal referenced to ground with a linearity of 1% of output voltage.

SDC-14570/75 Series converters are available with operating temperature ranges of 0°C to +70°C and -55°C to +125°C, and MIL-PRF-38534 processing is available.

APPLICATIONS

With its low cost, small size, high accuracy, and versatile performance, the SDC-14570/75 Series converters are ideal for use in modern, high-performance military and industrial position control systems. Typical applications include radar antenna positioning, navigation and fire control systems, motor control, and robotics.

- Fixed 14- or 14/16-Bit Resolution
- \overline{BIT} for ERROR or LOS
- No 180° Hangup
- Small Size 1.0" X 0.8" Package
- Velocity Output Eliminates Tachometer
- High Reliability Single Chip Monolithic
- -55°C to +125°C Operating Temperature Range
- MIL-PRF-38534 Processing Available

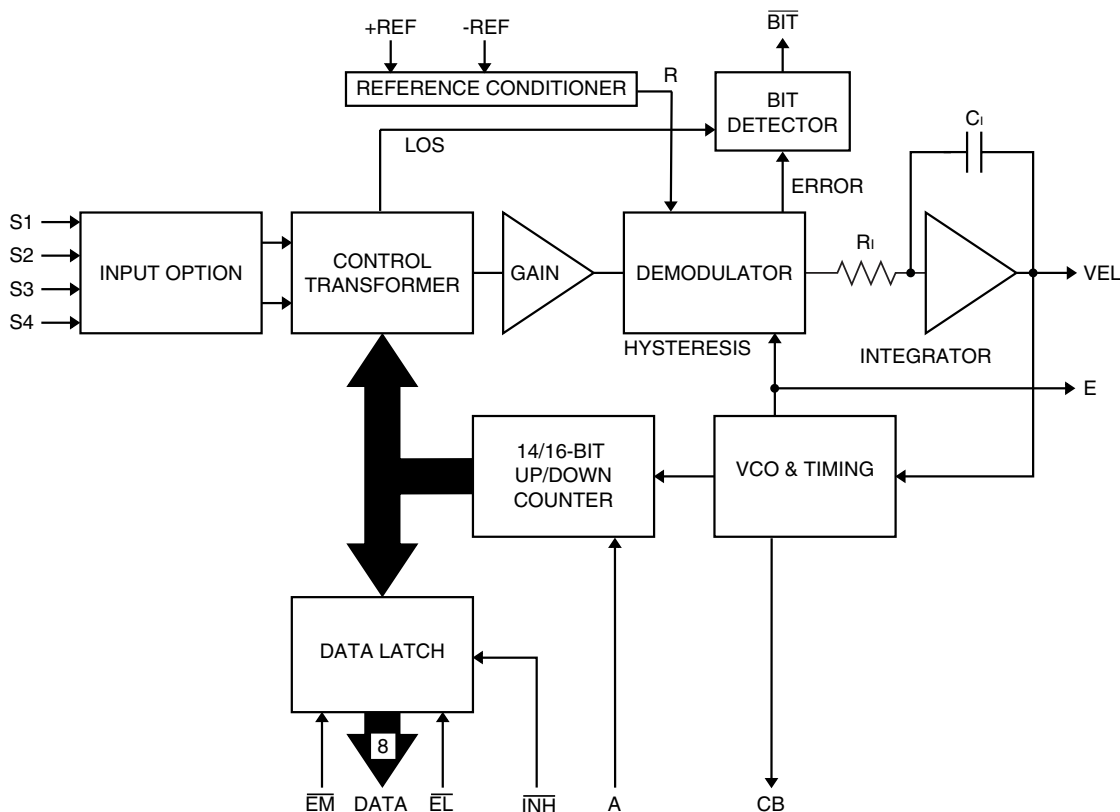


FIGURE 1. SDC-14570/75 BLOCK DIAGRAM

TABLE 1. SDC-14570/75 SPECIFICATIONS			
These specs apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation, and 10% harmonic distortion.			
PARAMETER	UNIT	VALUE	
RESOLUTION	Bits	14	16
ACCURACY	Min	4 + 1 LSB	2 + 1 LSB
REPEATABILITY	LSB	1 max	
DIFFERENTIAL LINEARITY	LSB	1 max	
REFERENCE INPUT Type		(+REF, -REF) differential	
		2 & 11.8 V UNITS	90 V unit
Voltage Range	Vrms	2-35	10-130
Frequency	Hz	360-5000	see note
Input Impedance single ended	Ohm	60k	270k min
differential	Ohm	120k	540k min
Common Mode Range	Vpeak	50,	200,
		100 transient	300 transient
SIGNAL INPUT CHARACTERISTICS			
90 V Synchro Input (L-L)			
Zin line-to-line	Ohm	123k	
Zin line-to-ground	Ohm	80k	
Common Mode Voltage	V	180 max	
11.8 V Synchro Input (L-L)			
Zin line-to-line	Ohm	52k	
Zin line-to-ground	Ohm	34k	
Common Mode Voltage	V	30 max	
11.8 V Resolver Input (L-L)			
Zin line-to-line	Ohm	140k	
Zin line-to-ground	Ohm	70k	
Common Mode Voltage	V	30 max	
2V Direct Input (L-L)			
Voltage Range	Vrms	2 nom, 2.3 max	
Max Voltage No Damage	V	25 cont, 100 pk transient	
Input Impedance	Ohm	20 M//10 pF min	
DIGITAL INPUT/OUTPUT			
Logic Type		TTL/CMOS compatible	
Inputs		Logic 0 = 0.8 V max. Logic 1 = 2.0 V min. Loading = 10 µA max P.U. current source to +5 V //5 pF max. CMOS transient protected	
Resolution Control (A)		SDC-14575 Series Only 30k pull-down to GND. Open = 14 bits; +5 V = 16 bits	
Inhibit ($\overline{\text{INH}}$)(common)		Logic 0 inhibits; Data stable within 0.5 µs	
Enable Bits 1 to 8 ($\overline{\text{EM}}$)		Logic 0 enables; Data stable within 150 ns	
Enable Bits 9 to 14(16) ($\overline{\text{EL}}$)		Logic 1 = High Impedance Data High Z within 100 ns	
Outputs			
Parallel Data (1-16)	bits	8 parallel lines; 2 bytes natural binary angle, positive logic	
Converter Busy (CB)	µs	0.3 - 1.0 positive pulse. Data valid 500 ns max after leading edge	

TABLE 1. SDC 14570/75 SPECIFICATIONS (CONTINUED)			
PARAMETER	UNIT	VALUE	
DIGITAL INPUT/OUTPUT			
OUTPUTS (continued)			
Built-In-Test (BIT)		Logic 0 = BIT condition. ± 100 LSBs of error with a filter of 500 µs or LOS.	
Drive Capability	TTL	50 pf + Logic 0; 1 TTL load, 1.6 mA at 0.4 V max Logic 1; 10 TTL loads, -0.4 mA at 2.8 V min	
	CMOS	Logic 0; 100 mV max driving Logic 1; +5 V supply minus 100 mV min driving	
DYNAMIC CHARACTERISTICS			
		Device Type	
		60 Hz	400 Hz
Input Frequency	Hz	47-5k	360-5k
Bandwidth(Closed Loop)	Hz	15	103
Ka	1/s ²	830	53k
A1	1/s	0.17	1.33
A2	1/s	5k	40k
A	1/s	29	230
B	1/s	14.5	115
Resolution	bits	14	16
Tracking Rate typical	rps	1.25	0.31
minimum	rps	1	0.25
Acceleration (1 LSB lag)	deg/s ²	18	4.5
Settling Time (179° step max)	msec	1100	2500
		140	320
VELOCITY CHARACTERISTICS			
Polarity		Positive for increasing angle	
Voltage Range(Full Scale)	±V	4.5 typ, 4 min	
Scale Factor	±%	10 typ	20 max
Scale Factor TC	ppm/°C	100 typ	200 max
Reversal Error	±%	1 typ	2 max
Linearity	±%	0.5 typ	1 max
Zero Offset	mV	5 typ	10 max
Zero Offset TC	µV/°C	15 typ	30 max
Load	kOhm		20 max
Noise	(Vp/V)%	1 typ	2 max
DC ERROR (E)	V	-1.25 per +1 LSB error filtered (± 3 LSB range)	
POWER SUPPLIES			
Nominal Voltage	V	+5	-5
Voltage Range	±%	5	10
Max Volt. w/o Damage	V	+7	-7
Current	mA	12 typ,	17 max
TEMPERATURE RANGE			
Operating			
-3XX	°C	0 to +70	
-1XX	°C	-55 to +125	
Storage	°C	-65 to +150	
PHYSICAL CHARACTERISTICS			
Size	in (mm)	0.98 x 0.78 x 0.2 (24.9 x 19.8 x 5.1)	
Weight	oz	0.66	

Note: 47 - 5k for 90 V, 60 Hz; 360 - 5k for 90 V, 400 Hz

THEORY OF OPERATION

The SDC-14570/75 Series of converters are based upon a single chip CMOS custom monolithic. They are implemented using the latest IC technology which merges precision analog circuitry with digital logic to form a complete high performance tracking resolver to digital converter.

FIGURE 1 is the Functional Block Diagram of SDC-14570/75 Series. The SDC-14570 Series is fixed at 14 bits. The SDC-14575 is pin programmable for 14- or 16-bit operation using resolution control line "A." A logic 0 (open line) will select 14 bits; a logic 1 will select 16-bit operation. The converter operates with ± 5 V dc power supplies. Analog signals are referenced to analog ground, which is at ground potential. The converter is made up of three main sections; an input front-end, a converter, and a digital interface. The converter front-end differs for synchro, resolver and direct inputs. An electronic Scott-T is used for synchro inputs, a resolver conditioner for resolver inputs and a sine and cosine voltage follower for direct inputs. These amplifiers feed the high accuracy Control Transformer (CT). Its other input is the 14-bit digital angle ϕ . Its output is an analog error angle, or difference angle, between the two inputs. The CT performs the ratiometric trigonometric computation of $\sin\theta\cos\phi - \cos\theta\sin\phi = \sin(\theta-\phi)$ using amplifiers, switches, logic and capacitors in precision ratios.

The converter accuracy is limited by the precision of the computing elements in the CT. In these converters ratioed capacitors are used in the CT, instead of the more conventional precision ratioed resistors. Capacitors used as computing elements with op-amps need to be sampled to eliminate voltage drifting. Therefore, the circuits are sampled at a high rate to eliminate this drifting and at the same time to cancel out the op-amp offsets.

The error processing is performed using the industry standard technique for type II tracking R/D converters. The dc error is integrated yielding a velocity voltage which in turn drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which together with the velocity integrator forms a type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above.

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Functional Block Diagram and its Bode Plots (open and closed loop); These are shown in FIGURES 1 and 2.

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2 \left(\frac{S}{B} + 1 \right)}{S^2 \left(\frac{S}{10B} + 1 \right)}$$

where A is the gain coefficient
and B is the frequency of lead compensation

The components of gain coefficient are error gradient, integrator gain, and VCO gain. These can be broken down as follows:

- Error Gradient = 0.011 volts per LSB (CT+Error Amp+Demod)
- Integrator gain = $\frac{1}{R_i C_i}$ volts per second per volt
- VCO Gain = $\frac{1}{1.25 R_v C_v}$ LSBs per second per volt

GENERAL SETUP CONSIDERATIONS

The following recommendations should be considered when connecting the SDC-14570 Series converters:

- 1) Power supplies are ± 5 V dc. For lowest noise performance it is recommended that a 0.1 μ F or larger cap be connected from each supply to ground near the converter package.
- 2) Direct inputs are referenced to Analog GND.
- 3) Digital Ground should be connected to Analog Ground as close to the package as possible.

INHIBIT AND ENABLE TIMING

The Inhibit ($\overline{\text{INH}}$) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an Inhibit signal does not interfere with the continuous tracking of the converter. As shown in FIGURE 3, angular output data is valid 500 nanoseconds maximum after the application of the low-going inhibit pulse.

Output angle data is enabled onto the tri-state data bus in six bytes. The Enable MSBs ($\overline{\text{EM}}$) is used for the most significant 8 bits and Enable LSBs ($\overline{\text{EL}}$) is used for the least significant bits. As shown in FIGURE 4, output data is valid 150 nanoseconds maximum after the application of a low-going enable pulse. The tri-state data bus returns to the high impedance state 100 nanoseconds maximum after the rising edge of the enable signal.

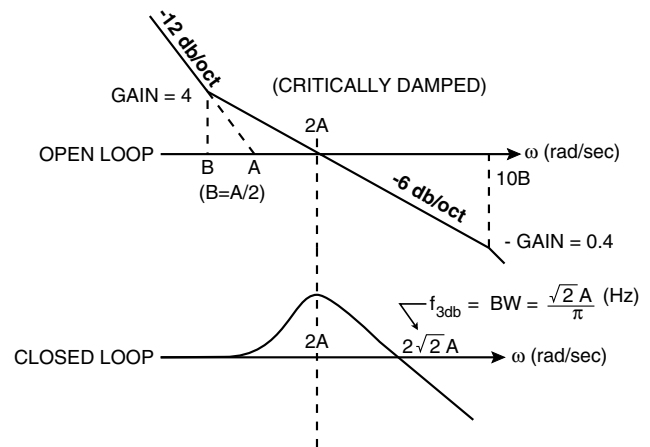


FIGURE 2. BODE PLOTS

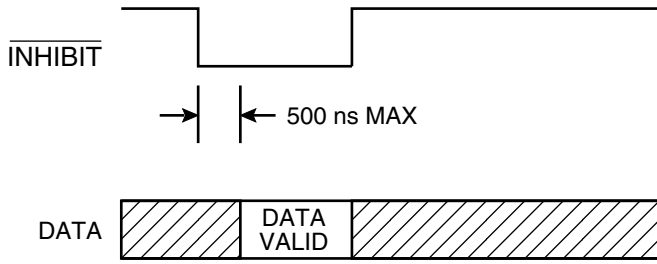


FIGURE 3. INHIBIT TIMING

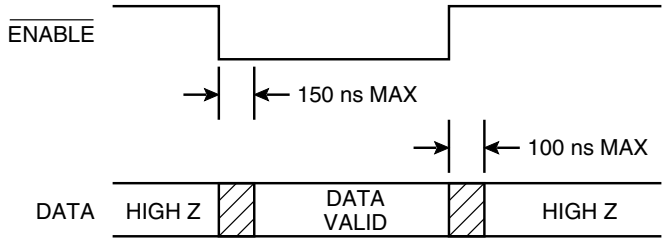


FIGURE 4. ENABLE TIMING

BIT, BUILT-IN-TEST

This output is a logic line that will flag an internal fault condition or LOS (Loss-Of-Signal). The internal fault detector monitors the internal error and, when it exceeds ± 100 LSBs, will set the line to a logic 0; this condition will occur during a large-step input and will reset to a logic 1 after the converter settles out. (The error voltage is filtered with a $500 \mu\text{s}$ filter) BIT will set for an over-velocity condition because the converter loop cannot maintain input/output sync. BIT will also set if a total LOS (loss of all signals) occurs.

NO FALSE 180° HANGUP

This feature eliminates the “false 180° reading” during instantaneous 180° step changes; this condition most often occurs when the input is “electronically switched” from a digital-to-synchro converter. If the “MSB” (or 180° bit) is “toggled” on and off, a converter without the “false 180° hangup” feature may fail to respond.

The condition is artificial, as a “real” synchro or resolver cannot change its output 180° instantaneously. The condition is most often noticed during wraparound verification tests, simulations, or troubleshooting.

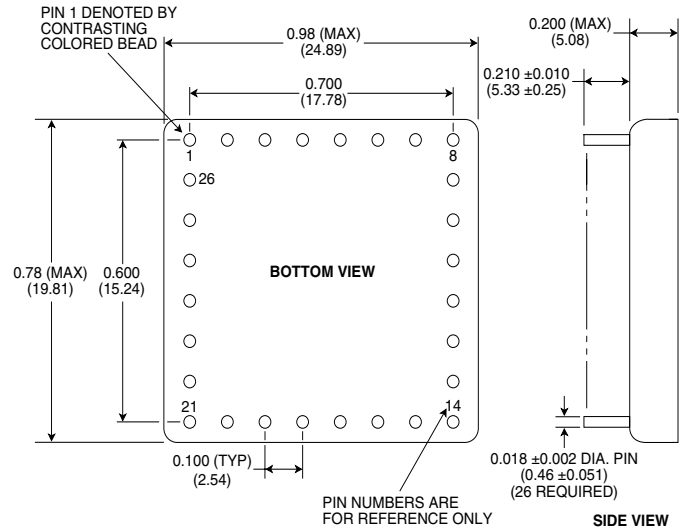


FIGURE 5. SDC-14570/75 MECHANICAL OUTLINE

TABLE 2. PINOUT (26 PIN)*

1	S1(S)	S1(R)	N.C.	26	+REF	(+Reference Input)
2	S2(S)	S2(R)	+COS(D)	25	-REF	(-Reference Input)
3	S3(S)	S3(R)	+SIN(D)	24	Analog Ground	
4	N.C.	S4(R)	N.C.	23	EM	(Enable MSBs)
5	A (Resolution Control)**			22	E	(DC Error Output)
6	Digital Ground			21	VEL	(Velocity Output)
7	-5 V (Power Supply)			20	INH	(Inhibit)
8	+5 V (Power Supply)			19	EL	(Enable LSBs)
9	Bit 1 (MSB)	/Bit 9		18	BIT	(Built-In-Test)
10	Bit 2	/Bit 10		17	CB	(Converter Busy)
11	Bit 3	/Bit 11		16	Bit 8	/Bit 16**
12	Bit 4	/Bit 12		15	Bit 7	/Bit 15**
13	Bit 5	/Bit 13		14	Bit 6	/Bit 14

* Note: (S) = Synchro; (R) = Resolver; (D) = 2 V Resolver Direct

** Note: SDC-14575 Series only

ORDERING INFORMATION

SDC-1457X - X X X

- Accuracy:**
 - 2 = 4 + 1 LSB
 - 4 = 2 minutes + 1 LSB (Not available with 14-bit units.)
- Reliability Grade:**
 - 0 = Standard DDC procedures
 - 1 = Fully Compliant with MIL-PRF-38534*
 - 2 = Screened to MIL-PRF-38534 but without QCI testing*
 - 3 = Fully Compliant with MIL-PRF-38534 + PIND Testing*
 - 4 = Fully Compliant with MIL-PRF-38534 + Solder Dip*
 - 5 = Fully Compliant with MIL-PRF-38534 + PIND Testing + Solder Dip*
 - 6 = Screened to MIL-PRF-38534 + PIND Testing but without QCI Testing*
 - 7 = Screened to MIL-PRF-38534 + Solder Dip but without QCI Testing*
 - 8 = Screened to MIL-PRF-38534 + PIND Testing + Solder Dip but without QCI testing*
- Operating Temperature Range:**
 - 1 = -55 to +125°C
 - 3 = 0 to +70°C
 - 4 = -55 to +125°C + Variables Data
 - 8 = 0 to +70°C + Variables Data
- Input Option:**
 - 0 = 11.8 V, Synchro, 14 bit, 400 Hz
 - 1 = 11.8 V, Resolver, 14 bit, 400 Hz
 - 2 = 90 V, Synchro, 14 bit, 400 Hz
 - 3 = 2 V, Direct, 14 bit, 400 Hz
 - 4 = 90 V, Synchro, 14 bit, 60 Hz
 - 5 = 11.8 V, Synchro, 14/16 bit, 400 Hz
 - 6 = 11.8 V, Resolver, 14/16 bit, 400 Hz
 - 7 = 90 V, Synchro, 14/16 bit, 400 Hz
 - 8 = 2 V, Direct 14/16 bit, 400 Hz
 - 9 = 90 V, Synchro, 14/16 bit, 60 Hz

These products contain tin-lead solder finish as applicable to solder dip requirements.

Notes:

- * MIL-PRF-38534 product grading is designated with the following dash numbers:
 - Class H is a -11X, 13X, 14X, 15X, 41X, 43X, 44X, 45X
 - Class G is a -21X, 23X, 24X, 25X, 51X, 53X, 54X, 55X
 - Class D is a -31X, 33X, 34X, 35X, 81X, 83X, 84X, 85X

STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	3000g
BURN-IN	1015 ^(Note 1) 1030 ^(Note 2)	TABLE 1

Notes:

1. For Process Requirement "B"* (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.
2. When applicable.

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