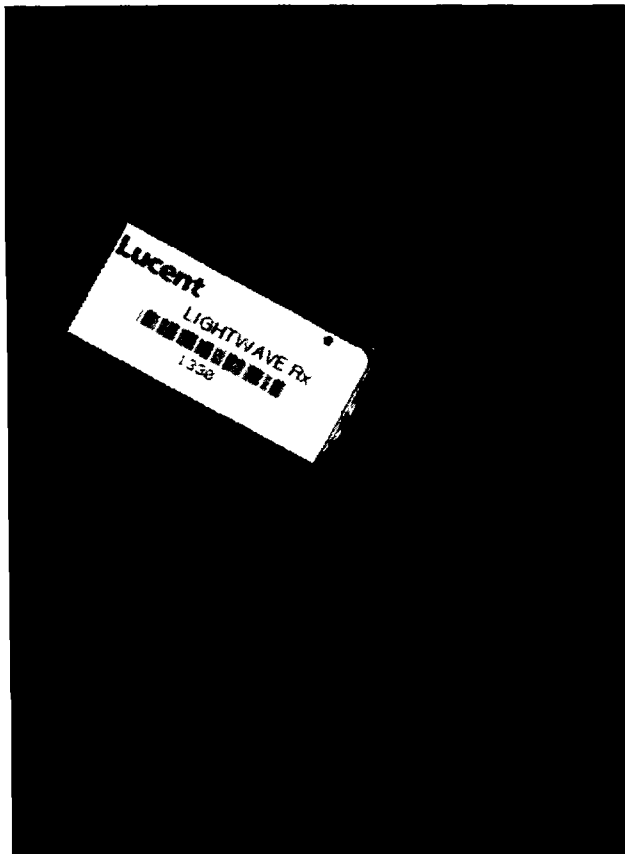




## 1330-Type Lightwave Receiver with Clock Recovery and Data Retiming



The 1330-Type Lightwave Receiver is manufactured in a 20-pin DIP with a multimode fiber pigtail.

### Features

- Clocked decision circuit
- Regenerated differential clock signal
- Wide dynamic range: 1330B, 40 dB @ OC-3; 1330D, 25 dB @ OC-12
- Exceeds all SONET (GR-253-CORE) and ITU-T G.958 jitter requirements
- Space-saving, self-contained, 20-pin DIP
- Lucent Technologies Microelectronics Group Reliability and Qualification Program for built-in quality
- Operation at 1.3  $\mu\text{m}$  or 1.55  $\mu\text{m}$  wavelengths

- Positive ECL-level outputs
- CMOS (TTL) link-status flag output
- Operating case temperature range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- 5 V power supply

### Applications

- Telecommunications
  - Inter- and intraoffice SONET/ITU-T SDH
  - Subscriber loop
  - Metropolitan area networks
- High-speed data communications

### Description

The 1330-Type fiber-optic receiver is designed for use in transmission systems or medium- to high-speed data communication applications. Used in intermediate- and long-reach applications, the receiver operates at the SONET OC-3 or OC-12 data rate as well as the ITU-T Synchronous Digital Hierarchy (SDH) rate of STM-1 or STM-4, depending on the receiver model chosen. The receiver meets all present Bellcore GR-253-CORE requirements, the current ANSI T1X1.5 intraoffice specifications, and the ITU-T G.957 and G.958 recommendations. Compact packaging, a high level of integration, and a wide dynamic range make these receivers ideal for data communications.

Manufactured in a 20-pin DIP, the receiver consists of a planar InGaAs PIN photodetector, a GaAs preamplifier, a silicon bipolar limiting amplifier that converts the small signal to ECL levels, a timing recovery unit to recover the clock, and a silicon bipolar decision circuit.

**Description** (continued)

The receiver converts optical signals in the range of 1.2  $\mu\text{m}$  to 1.6  $\mu\text{m}$  into retimed clock and data signals. The clock and data outputs are raised-ECL (PECL) logic levels. A CMOS-level flag output indicates when there is a loss of optical signal. When the flag is asserted (loss of optical input), the data and clock outputs are squelched.

The receiver requires a 5 V power supply for the amplifier, logic, and PLL CRC circuits. The operating case temperature range is  $-40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ .

**V<sub>PIN</sub> (Pin 10)**

**Do not leave this pin unconnected.** This lead supplies the bias for the PIN photodetector diode. The input must be grounded or supplied with a negative bias between zero and  $-10\text{ V}$ . Applying a negative bias to this pin improves the optical overload specification. Additionally, by using a negative power supply and a  $5\text{ k}\Omega$  to  $10\text{ k}\Omega$  resistor in series with the V<sub>PIN</sub> lead, it is possible to measure the PIN photocurrent generated in response to the incoming optical signal. This provides a means to create optical power alarm circuits.

**Flag Output**

When the optical input falls below the Link Status Flag switching threshold, the Link Status Flag is deactivated and its output logic level changes from a CMOS logic HIGH to a CMOS logic LOW.

**Squelched Data and Clock Outputs**

In some version of the 1330 receiver (see Table 3), when the Link Status Flag is deactivated, the data and clock outputs are squelched (stop outputting a signal).

When this occurs, the DATA,  $\overline{\text{DATA}}$ , CLOCK, and  $\overline{\text{CLOCK}}$  outputs switch to a constant dc output voltage level of 1.3 V.

**Nonsquelched Data and Clock Outputs**

Lucent Technologies also manufactures a nonsquelching version of the 1330 receiver for those applications that require that the data and clock outputs continue to function after the Link Status Flag is deactivated. In those versions of the receiver, when the Link Status Flag is deactivated, a signal will continue to appear at the DATA,  $\overline{\text{DATA}}$ , CLOCK, and  $\overline{\text{CLOCK}}$  outputs. See Table 3 for nonsquelching codes.

**Pin Information**

Pin	Name	Pin	Name
1	Ground	20	No User Connection*
2	Ground	19	No User Connection*
3	Ground	18	No User Connection*
4	CLOCK	17	No User Connection*
5	$\overline{\text{CLOCK}}$	16	Ground
6	Ground	15	Ground
7	DATA	14	$\overline{\text{FLAG}}^\dagger$
8	Ground	13	Ground
9	$\overline{\text{DATA}}$	12	$\text{FLAG}^\dagger$
10	V <sub>PIN</sub>	11	V <sub>CC</sub>

\* Pins designated as No User Connection are not connected internally. However, to allow for future functional upgrades, it is recommended that the user not make any connections to these pins.

† The link status flag is a logic flag that indicates the presence or absence of a minimum acceptable level of optical input. A logic high on the FLAG output indicates the presence of a valid optical signal.

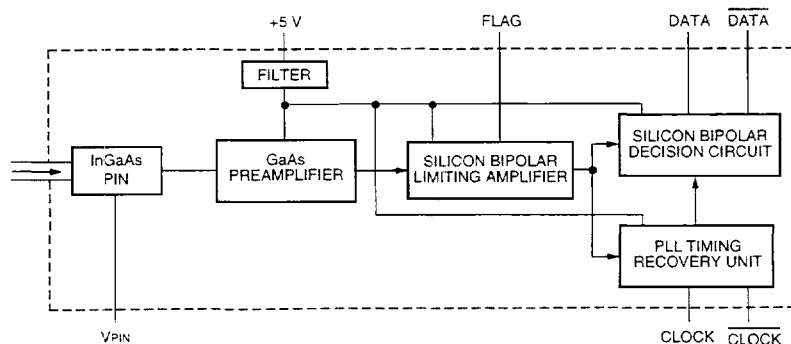


Figure 1. Block Diagram

## Handling Precautions

The pigtail consists of a 39 in.  $\pm$  4 in. (1 m  $\pm$  10 cm), 62.5  $\mu$ m, multimode fiber. The sheathed fiber has a nominal outside diameter of 900  $\mu$ m and can be terminated with an FC-PC, ST<sup>®</sup>, or SC connector. The minimum fiber-bending radius during operation is 1.25 in. (32 mm).

Other connector options are available on special order. Please contact a Lucent Account Manager for availability and ordering information.

## Electrostatic Discharge

**CAUTION: This device is susceptible to damage as a result of electrostatic discharge (ESD). Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).**

Although protection circuitry is designed into the device, take proper precautions to avoid exposure to ESD.

Lucent employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection-design evaluation. The HBM withstand voltage established for the 1330 receiver is  $\pm$ 1500 V and the CDM withstand voltage is  $\pm$ 1000 V.

## Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	T <sub>c</sub>	-40	85	°C
Storage Temperature	T <sub>stg</sub>	-40	85	°C
Operating Wavelength Range	$\lambda$	1.1	1.57	$\mu$ m
Supply Voltage	V <sub>CC</sub>	0	5.5	V
	V <sub>PIN</sub>	0	-15	V
Lead Soldering Temperature/Time	—	—	250/10	°C/s

## Receiver Processing

The 1330-Type Receiver devices can withstand normal wave-soldering processes. The complete receiver module is not hermetically sealed; therefore, it should not be immersed in or sprayed with any solutions. The process cap and fiber pigtail jacket deformation temperature is 85 °C. The receiver pins can be wave-soldered at 250 °C for 10 seconds.

## Installation Considerations

Although the receiver has been designed with ruggedness in mind, care should be used during handling. The optical connector should be kept free from dust, and the process cap should be kept in place as a dust cover when the device is not connected to a cable. If contamination is present on the optical connector, the use of canned air with an extension tube should remove any debris. Other cleaning procedures are identified in the *Cleaning Fiber-Optic Assemblies* Technical Note (TN95-010LWP).

The 1330-Type Receiver has been subjected to a fiber-pull mechanical strength test as part of device qualification (see Qualification Testing section). However, the cable should be handled conservatively with no excessive axial pulling or lateral tugging.

## Characteristics

Table 1. Electrical Characteristics

Parameter	Symbol	Min	Typ*	Max	Unit
Bit Rates	—	155.504 622.020	155.520 622.080	155.536 622.140	Mbits/s Mbits/s
dc Power Supply Voltages	V <sub>CC</sub> V <sub>PIN</sub> †	4.75 0	5.0 -5.0	5.25 -10.0	V V
dc Power Supply Current Requirements:‡	I <sub>PIN</sub> I <sub>CC</sub> I <sub>CC</sub>	0 110 150	— 125 200	1 200 250	mA mA mA
Output Data/Clock Voltage:§,**					
Low	V <sub>OL</sub>	V <sub>CC</sub> - 1.95	—	V <sub>CC</sub> - 1.63	V
High	V <sub>OH</sub>	V <sub>CC</sub> - 1.03	—	V <sub>CC</sub> - 0.88	V
Output Data/Clock Rise and Fall Time:					
OC-3 Version	t <sub>R</sub> /t <sub>F</sub>	1100	1300	1700	ps
OC-12 Version	t <sub>R</sub> /t <sub>F</sub>	320	360	500	ps
Output Flag Voltage:					
Low	V <sub>FOL</sub>	0	—	0.6	V
High	V <sub>FoH</sub>	V <sub>CC</sub> - 1.0	—	V <sub>CC</sub>	V
Clock/Data Alignment:††					
OC-3 Version	T <sub>CDA</sub>	-800	—	800	ps
OC-12 Version	T <sub>CDA</sub>	-300	—	300	ps
Clock Duty Cycle	—	45	—	55	%
Output Clock Random Jitter:‡‡					
OC-3 Version	J <sub>c</sub>	—	1.2	3.6	°RMS
OC-12 Version	J <sub>c</sub>	—	1.5	3.6	°RMS
Output Clock Jitter Peaking	J <sub>p</sub>	0.04	0.05	0.06	dB
Jitter Tolerance	Bellcore GR-253-CORE and ITU-T G.958 Compliant				
Jitter Transfer	Bellcore GR-253-CORE and ITU-T G.958 Compliant				

\* Typical values are measured at room temperature and nominal supply voltage.

† V<sub>PIN</sub> is an optional bias voltage that can be applied to pin 10. If not biased, pin 10 must be grounded.

‡ Includes approximately 50 mA of DATA and CLOCK output termination current.

§ Measured with 50 Ω load terminated to (V<sub>CC</sub> - 2.00) V.

\*\* DATA and CLOCK outputs are 10K ECL compatible.

†† Measured as shown in Figure 2.

‡‡ Measured with an input data pseudorandom word 2<sup>23</sup> - 1.

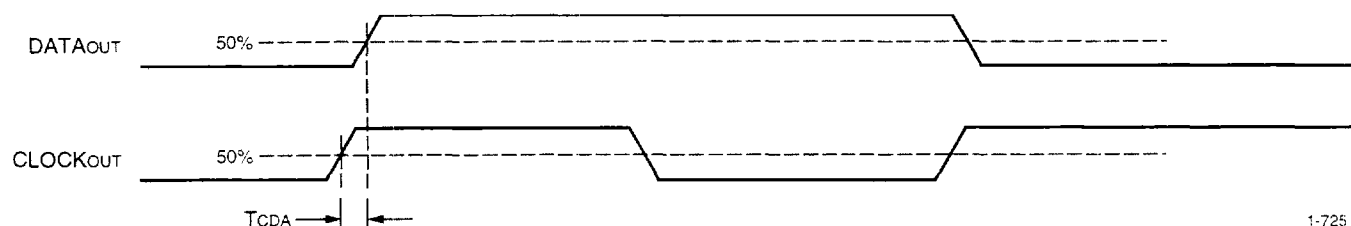


Figure 2. Clock/Data Alignment

**Characteristics** (continued)

**Table 2. Optical Characteristics**

Parameter	Symbol	Min*	Typ†	Max*	Unit
Measured Average Sensitivity:‡§					
OC-3	P <sub>RL</sub>	-36	-38	—	dBm
OC-12	P <sub>RL</sub>	-30	-32.5	—	dBm
Maximum Input Power:‡**					
OC-3	P <sub>RH</sub>	0	+2	—	dBm
OC-12	P <sub>RH</sub>	-6	-4	—	dBm
Link Status Flag Threshold:††					
OC-3:					
Decreasing Light Input	LST <sub>D</sub>	-50	-41	-37.5	dBm
Increasing Light Input	LST <sub>I</sub>	-50	-38	-36.0	dBm
OC-12:					
Decreasing Light Input	LST <sub>D</sub>	-50	-38.8	-32.5	dBm
Increasing Light Input	LST <sub>I</sub>	-50	-35	-31.0	dBm
Flag Hysteresis	HYS	0.5	3	—	dB
Flag Response Time	t <sub>FLAG</sub>	3	—	100	μs

\* Over operating temperature range and at end of life (EOL).

† Typical values at room temperature and beginning of life (BOL).

‡ For a 1e-10 BER. Measured with a 2<sup>23</sup> - 1 pseudorandom word optical input having a 50% average duty cycle.

§ Power supply noise in excess of 50 mV peak-to-peak may degrade the performance of the receiver. See User Interface section for recommended power supply filtering.

\*\* The 1330 receiver is guaranteed to meet the minimum values with pin 10 grounded. With pin 10 biased at -5 V, a typical overload input power of +2 dBm can be achieved for OC-3 version and -4 dBm for OC-12 version.

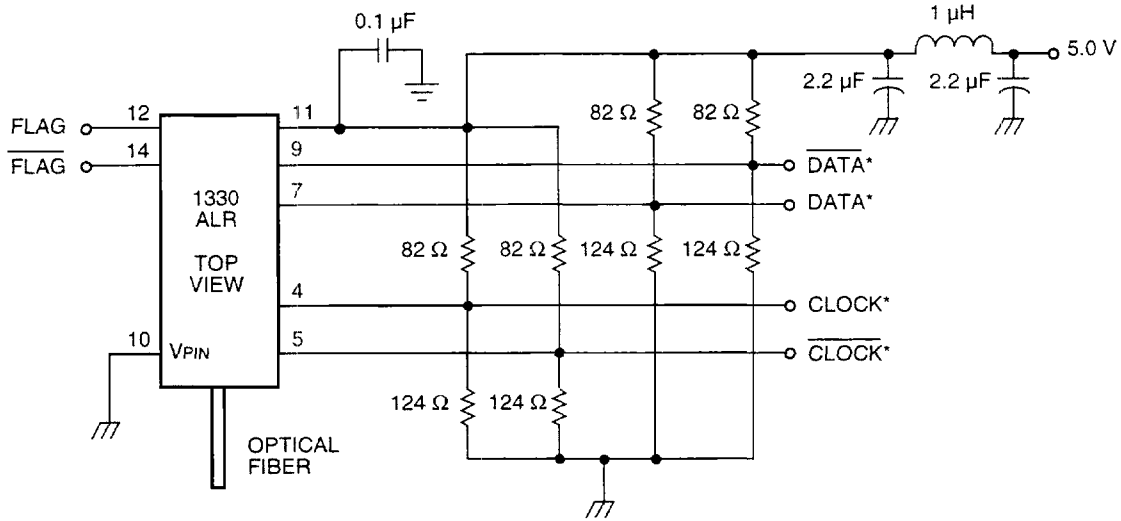
†† Whenever the flag output is deasserted (logic low), the DATA and CLOCK outputs are silenced. See the Flag Output section on page 2 for the DATA and CLOCK output signal levels.

**PWB Layout Guidelines**

- Follow high-speed ECL design rules.
- All high-speed output lines must be controlled-impedance lines, and the termination impedance must match the line impedance. Controlled-impedance interruptions should be avoided (i.e., 90° bends, etc.) and paired lines (i.e., DATA and  $\overline{\text{DATA}}$ ) should be of equal length.
- Each output line should be terminated at the end of the line and must have a bypass capacitor on the voltage side of the resistor for each termination.
- Data and clock output lines should be as short and as straight as possible and isolated from noise sources (and each other) to prevent noise from feeding back into the receiver.
- Noise that couples into the receiver through the power supply pins can degrade device performance. See Figure 3 for an example of power supply filtering for the receiver 5 V power supply pins.
- Use a multilayer board so that the ground plane surrounds the areas occupied by the receiver and directly underneath it. Directly attach all pins listed as ground pins to the ground plane with no additional lead length.

All unused outputs must be terminated as shown. All resistors are 1/8 W, thin-film, ceramic chips. All capacitors are 25 Vdc, ceramic X7R or equivalent.

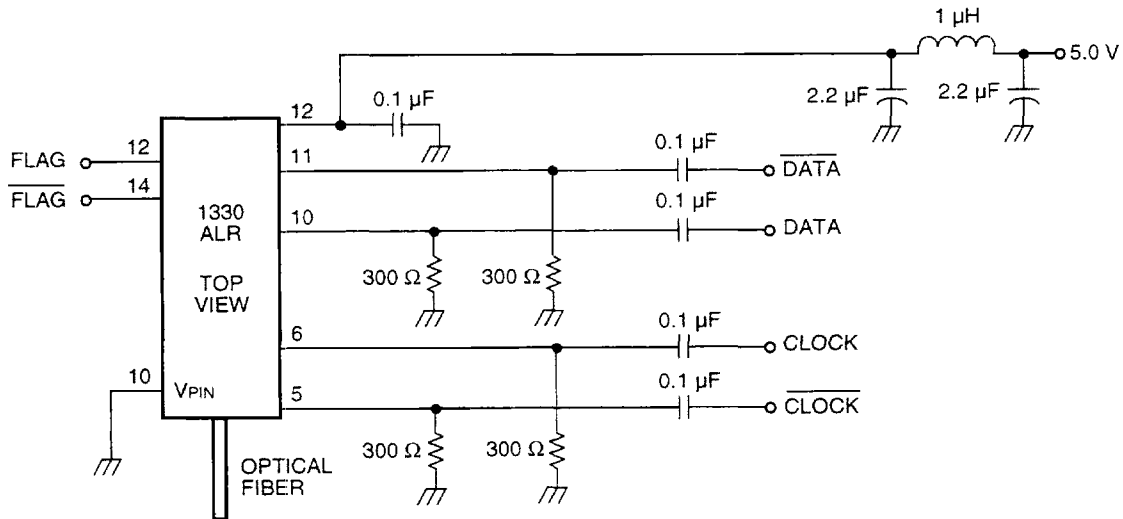
Recommended User Interfaces



1-726.b

\* DATA,  $\overline{\text{DATA}}$ , CLOCK, and  $\overline{\text{CLOCK}}$  are 50  $\Omega$  transmission lines that can be ac- or dc-coupled.

Figure 3. PECL-Compatible (5 V) Interface



1-870.b

Figure 4. ac-Coupled ECL-Compatible Interface

## Qualification Testing

To ensure high product reliability and customer satisfaction, Lucent is committed to an intensive quality program that starts in the design phase and proceeds through the manufacturing and shipping processes. Optoelectronic modules are qualified to Lucent's internal standards using MIL-STD-883 test methods and procedures and sampling techniques consistent with Bellcore requirements. The receiver will meet the specifications of Bellcore TR-NWT-000468 and TA-TSY-000983.

The 1330-Type Receiver has been subjected to the following qualifications and meets the specifications of Bellcore TR-NWT-000468 and TA-TSY-000983.

Test	Conditions	Sample Size	Failure Criteria
Physical Dimensions	MIL-STD-883-2016	90	Visual
External Visual	MIL-STD-883-2009.8	90	Visual
Impact Shock	1500G, 5 hits, 6 dir., MIL-STD-883-2002, Condition B	11	Electrical/optical
Variable Frequency Vibration	20G, 20 Hz to 2 kHz, 4 cycles, 3 directions, 4 min./cycle, MIL-STD-883-2007.1	11	Electrical/optical
Solderability	MIL-STD-883-2003.6	5	Visual
Lead Integrity	MIL-STD-883-2004.5	5	Visual
Solvent Resistance	MIL-STD-883-2015.7	5	Visual
Temperature Cycle	-40 °C to +85 °C, 500 cycles, MIL-STD-883-1010.7	11	Electrical/optical
High Temperature, High Humidity, with Bias	85 °C, 85% relative humidity, rated bias, 2000 hours	11	Electrical/optical
High Temperature with Bias	85 °C ambient, rated bias, 5000 hours, MIL-STD-883-1005.5	11	Electrical/optical
Internal Visual	MIL-STD-883-2014	10	Visual
Electrostatic Discharge	Human-body model (to determine class)	5	Electrical/optical
Fiber Pull	1 kg	11	Electrical/optical
Low-temperature Storage	-40 °C, 2000 hours	11	Electrical/optical
Voltage Stress	Maximum rated voltage	10	Electrical/optical
Power Cycling	MIL-STD-1006	5	Electrical/optical
Flammability	Fiber cable meets UL*-listed OFN	—	—

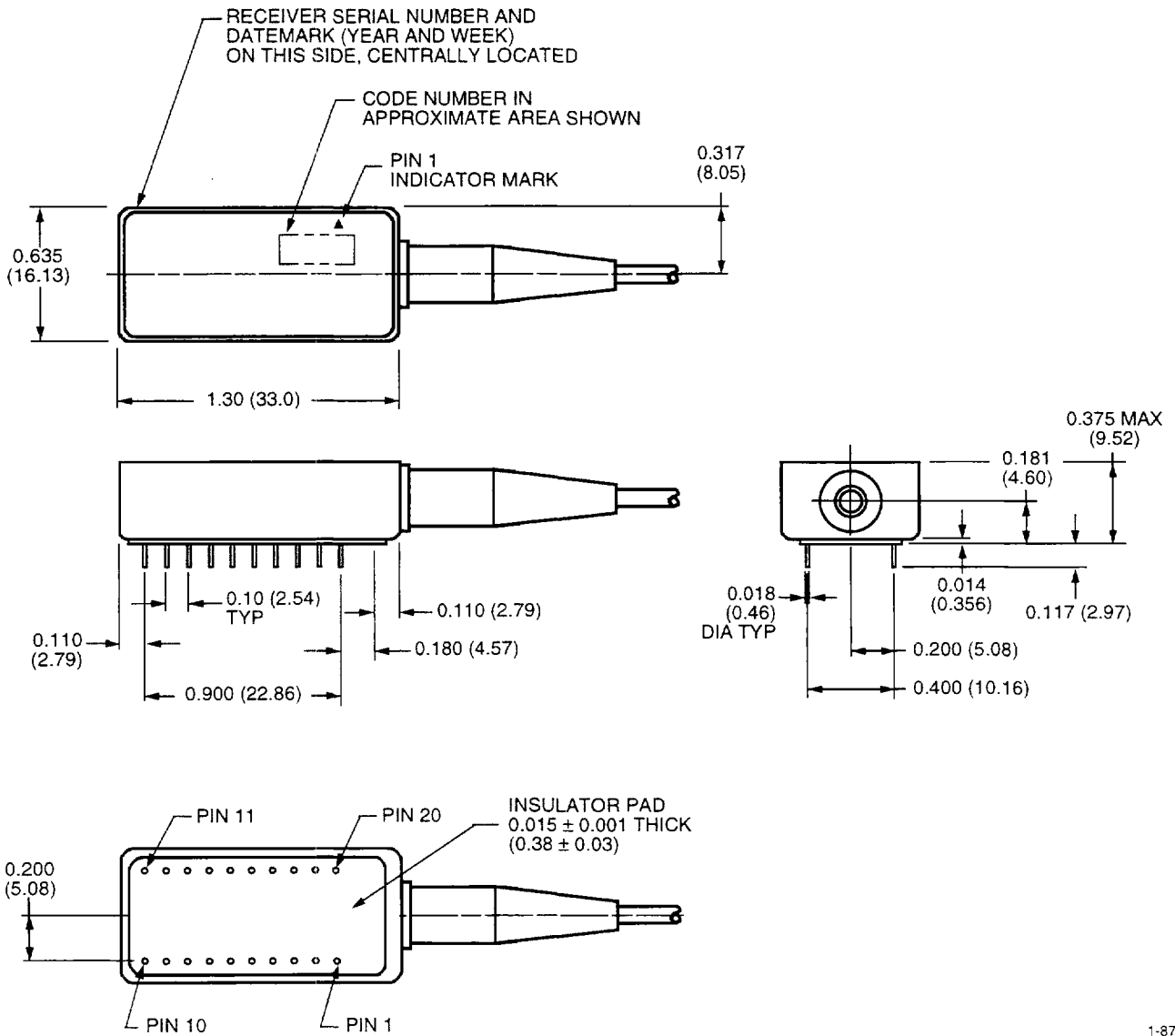
\* UL is a registered trademark of Underwriters Laboratories, Inc.

**Outline Diagram**

Dimensions are in inches and (millimeters).

Tolerances are  $\pm 0.005$  in. ( $\pm 0.127$  mm).

Weight = 2.5 oz. (70.87 g).



1-876.d

## Ordering Information

Table 3. 1330-Type Receiver Ordering Information

Product Code	Data Rate (Mbits/s)	Connector	Ordering Comcode
1330BA	155.520	FC-PC	107386286
1330BC	155.520	SC	107386302
1330BD	155.520	ST	107645764
1330BE*	155.520	FC-PC	107683443
1330BF*	155.520	SC	107683450
1330DA	622.080	FC-PC	107386310
1330DC	622.080	SC	107386336
1330DD	622.080	ST	107645756
1330DE*	622.080	FC-PC	107750457
1330DF*	622.080	SC	107750465

\* These models have nonsquelching data and clock outputs. See Nonsquelched Data and Clock Outputs section on page 2.

Table 4. Related Product Information

Product Code	Description	Document Number
1227-Type	1227-Type <i>ASTROTEC</i> <sup>®</sup> Laser Transmitter	DS96-387LWP
1229-Type	1229-Type <i>ASTROTEC</i> <sup>®</sup> Uncooled DFB Laser Transmitter	DS97-087LWP
1310-Type	1310-Type <i>ASTROTEC</i> <sup>®</sup> Receiver for OC-3/STM-1 1310-Type <i>ASTROTEC</i> <sup>®</sup> Receiver for OC-12/STM-4	DS96-368LWP

Table 5. Related Literature

Description	Document Number
Cleaning Fiber-Optic Assemblies	TN95-010LWP
Power Margin Analysis	TN95-008LWP
Selecting Lucent Fiber-Optic Transmitters and Receivers for SONET/SDH Applications	TN95-015LWP

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