Advance Product Information

VSC8164

2.488 Gbit/sec
1:16 SONET/SDH Demux

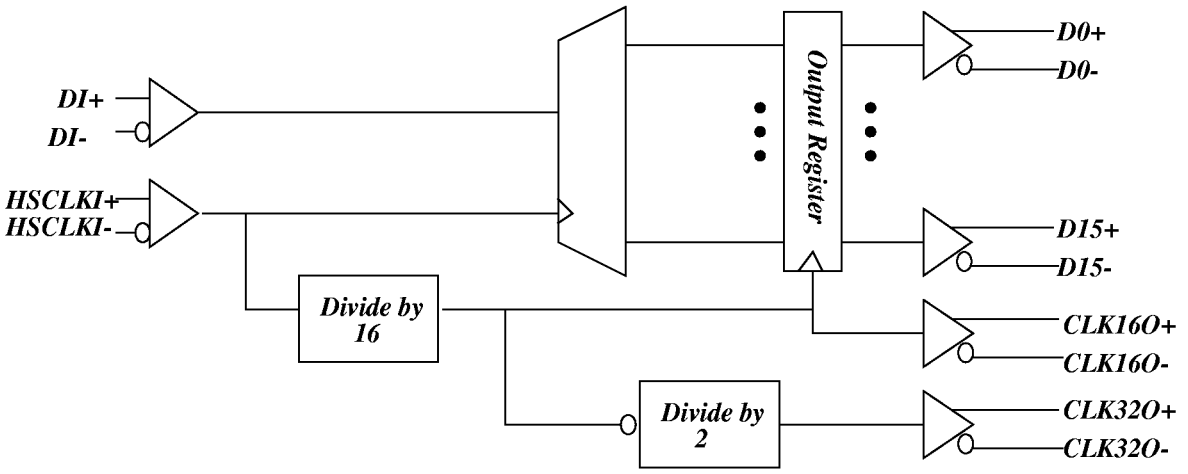
Features

- 2.488Gb/s 1:16 Demultiplexer
- Targeted for SONET OC-48 / SDH STM-16 Applications
- Differential LVPECL Low Speed Interface
- 128 Pin 14x20mm PQFP Package
- Single +3.3V Supply

General Description

The VSC8164 is a 1:16 demultiplexer for use in SONET/SDH systems operating at a 2.488Gb/s data rate. The device operates using a single 3.3V power supply, and is packaged in a thermally enhanced plastic package. The thermal performance of the 128PQFP allows the use of the VSC8164 without a heat sink under most thermal conditions.

VSC8164 Block Diagram



Functional Description

Low Speed Interface

The demultiplexed serial stream is made available by a 16 bit differential PECL interface D[15:0] with accompanying differential PECL divide by 16 clock CLK16O± and divide by 32 clock CLK32O±. These output drivers are designed to drive a 50Ω transmission line which can be DC terminated with a 50Ω resistor at the load connected to V_{CC}-2V on both the true and complement signals (see Figure 1), or appropriately AC coupled using various means (see Figure 2). The user should carefully choose the end terminating scheme such that the lowest frequencies of the D[15:0]± data stream are not below the cutoff frequency of the resulting RC network. These outputs should be biased such that 6mA is sourced from the part when the output driver is at V_{OL} (1.3V). Both outputs do not need to be terminated if the CLK16O± and D[15:0]± outputs are used single ended. The divide by 32 output can be used to provide a reference clock for the clock multiplication unit on the VSC8163.

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Figure 1: DC Termination of Low Speed PECL Outputs

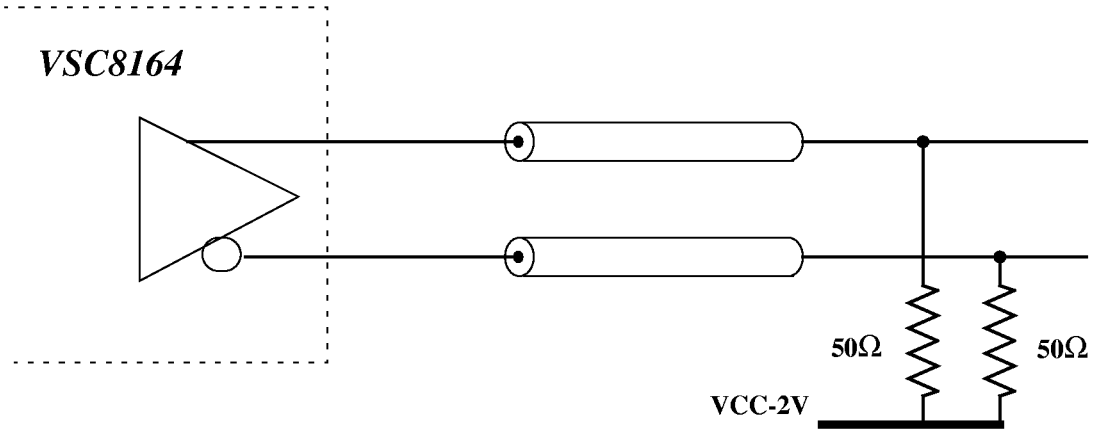
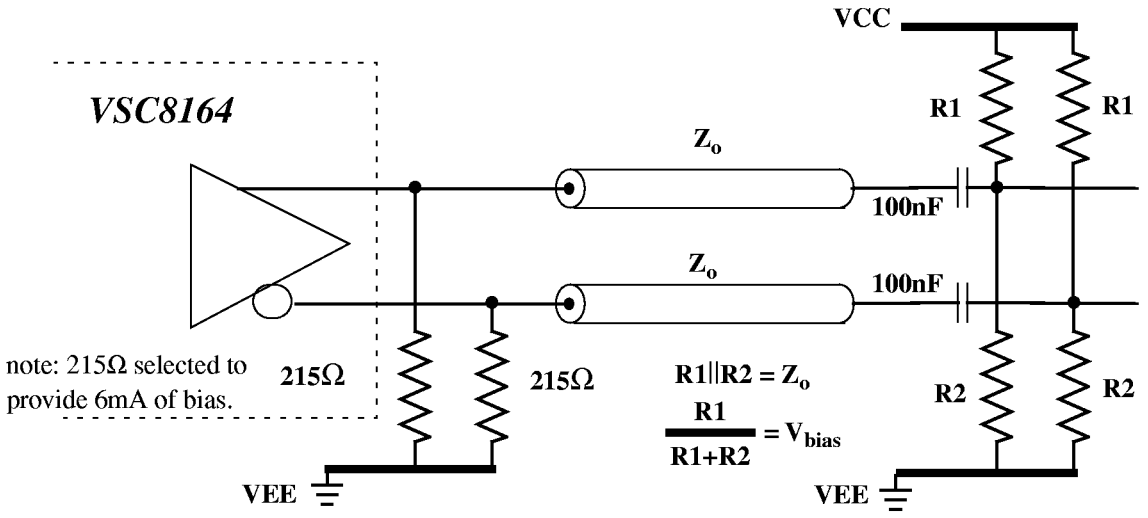


Figure 2: Suggested AC Termination of Low Speed PECL Outputs



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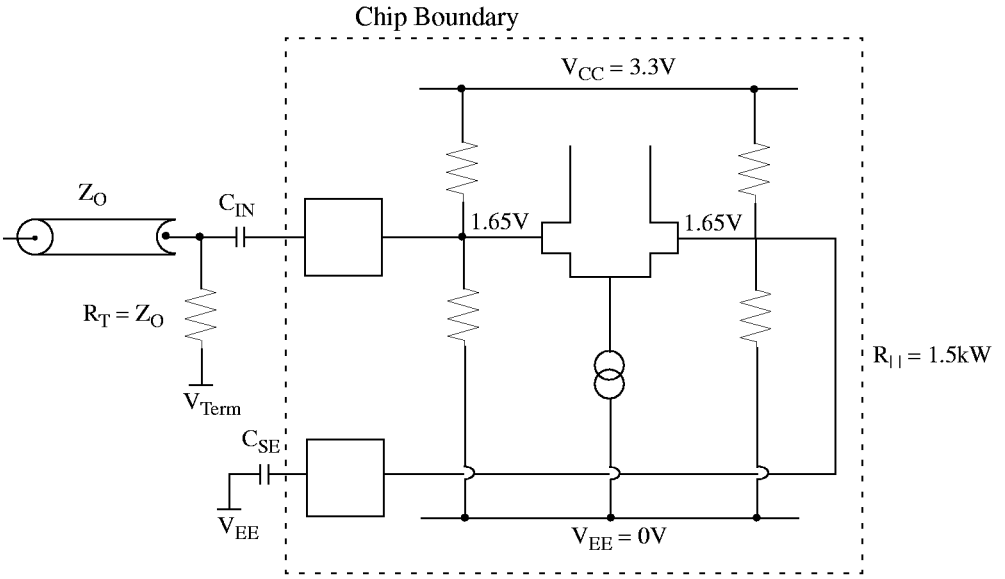
High Speed Interface

The incoming 2.488Gb/s data and input clock are received by PECL inputs DI and HSCLKI. Off-chip termination of these inputs is required, but internal biasing resistors provide a bias voltage suitable for AC coupling (see Figure 3).

In most situations these inputs will have high transition density and little DC offset. However, in cases where this does not hold, direct DC connection is possible. All serial data and clock inputs have the same circuit topology, as shown in figure 3. The reference voltage is created by a resistor divider as shown. If the input signal is driven differentially and DC-coupled to the part, the mid-point of the input signal swing should be centered about this reference voltage and not exceed the maximum allowable amplitude. For single-ended, DC-coupling operations, it is recommended that the user provides an external reference voltage which has better temperature and power supply noise rejection than the on-chip resistor divider. The external reference should have a nominal value equivalent to the common mode switch point of the DC coupled signal, and can be connected to either side of the differential gate.

Figure 3: High Speed Serial Clock and Data Inputs



C_{IN} TYP = 100 pF

C_{SE} TYP = 100 pF for single ended applications. (Capacitor values are selected for DI = 2.5Gb/s.)

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Supplies

This device is specified as a PECL device with a single positive 3.3V supply. Should the user desire to use the device in a ECL environment with a negative 3.3V supply, then VCC will be ground and VEE will be -3.3V.

Decoupling of the power supplies is a critical element in maintaining the proper operation of the part. It is recommended that the V_{CC} power supply be decoupled using a 0.1µF and 0.01µF capacitor placed in parallel on each V_{CC} power supply pin as close to the package as possible. If room permits, a 0.001µF capacitor should also be placed in parallel with the 0.1µF and 0.01µF capacitors mentioned above. Recommended capacitors are low inductance ceramic SMT X7R devices. For the 0.1µF capacitor, a 0603 package should be used. The 0.01µF and 0.001µF capacitors can be either 0603 or 0403 packages.

For low frequency decoupling, 47µF tantalum low inductance SMT caps should be sprinkled over the board's main +3.3V power supply and placed close to the C-L-C pi filter.

If the device is being used in an ECL environment with a -3.3V supply, then all references to decoupling V_{CC} must be changed to V_{EE}, and all references to decoupling 3.3V must be changed to -3.3V.

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AC Characteristics

Figure 4: AC Timing Waveforms

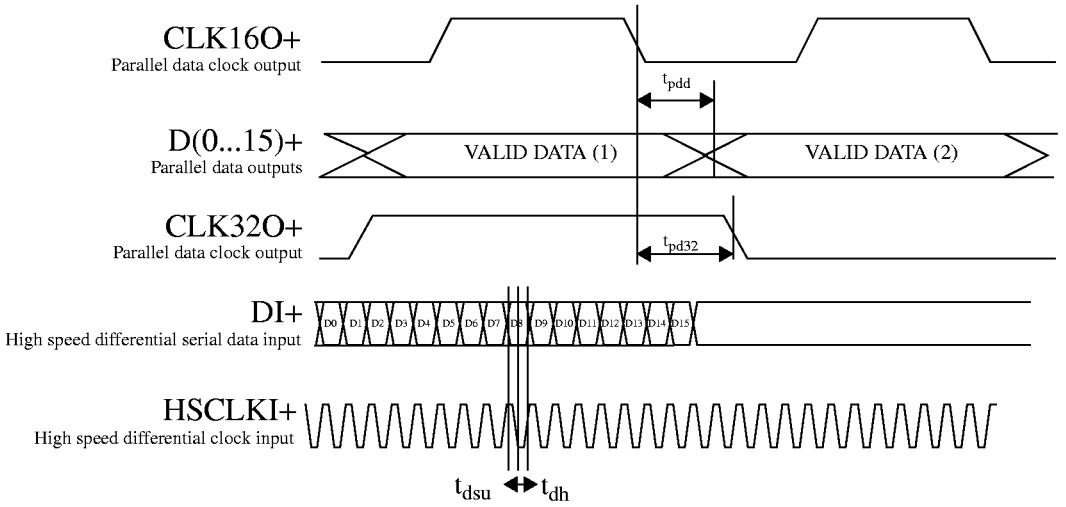


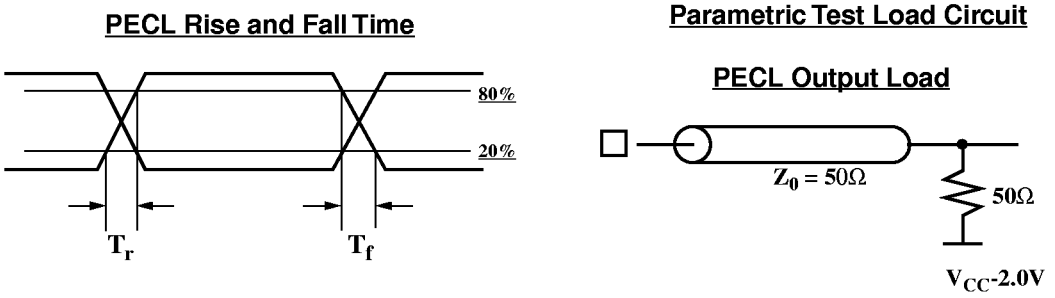
Table 1: AC Characteristics

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
t_{pdd}	Data valid from falling edge of CLK16O+	0	1.0	ns.	
t_{pd32}	CLK32O transition from falling edge of CLK16O+	0	1.0	ns.	
t_{DR}, t_{DF}	D[15:0]+/- rise and fall times		300	ps	20% to 80% into 50 Ohm load. See Figure 5
t_{CLKR}, t_{CLKF}	CLK16O+/- rise and fall times		250	ps	20% to 80% into 50 Ohm load. See Figure 5
$CLK16O_D$	CLK16O+/- duty cycle distortion	45	55	% of clock cycle	High speed clock input at 2.488GHz
t_{dsu}	DI+ setup time with respect to falling edge of HSCLKI+	100		ps	
t_{dh}	DI+ hold time with respect to falling edge of HSCLKI+	75		ps	
$HSCLKI_D$	HSCLKI+/- duty cycle distortion	40	60	% of clock cycle	

Table 2: DC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	PECL output high voltage	V_{CC}-1.02		V_{CC}-0.70	V	50Ω Termination to V_{CC} - 2.0V, See Figure 5
V_{OL}	PECL output low voltage	V_{CC}-2.00		V_{CC}-1.62	V	50Ω Termination to V_{CC} - 2.0V, See Figure 5
$\Delta V_{OLVPECL}$	Low speed output voltage single-ended, peak-to-peak swing	600		1300	mV	AC Coupled
ΔV_{IHS}	Serial input differential voltage	200			mV	AC Coupled, internally biased to VCC/2
V_{CC}	Supply voltage	3.14	—	3.47	V	3.3V± 5%
P_D	Power dissipation	—	.75	1.1	W	Outputs open, V_{CC} = 3.45V
I_{DD}	Supply Current	—	220	320	mA	Outputs open, V_{CC} = 3.45V

Figure 5: Parametric Measurement Information



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Absolute Maximum Ratings (1)

Power Supply Voltage, (V_{CC}) ..... -0.5V to +3.8V
DC Input Voltage (Differential inputs) ..... -0.5V to V_{cc}+0.5V
Output Current (Differential Outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55° to +125°C
Storage Temperature ..... -65°C to +150°C
Maximum Input ESD (Human Body Model) 1500V

Recommended Operating Conditions

Power Supply Voltage, (V_{CC}) ..... +3.3V±5%
Operating Temperature Range ..... 0°C Ambient to +85°C Case Temperature

Notes:

(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC8164 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500V.

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Package Pin Descriptions

Table 3: Package Pin Identification

Pin #	Name	I/O	Level	Description
13	D+	I	HS	High speed data input, true
14	D-	I	HS	High speed data input, complement
19	HSCLK-	I	HS	High Speed Clock Input, complement
20	HSCLK+	I	HS	High Speed Clock Input, true.
58	D15+	O	LVPECL	Low speed differential parallel data
59	D15-	O	LVPECL	Low speed differential parallel data
61	D14+	O	LVPECL	Low speed differential parallel data
62	D14-	O	LVPECL	Low speed differential parallel data
67	D13+	O	LVPECL	Low speed differential parallel data
68	D13-	O	LVPECL	Low speed differential parallel data
70	D12+	O	LVPECL	Low speed differential parallel data
71	D12-	O	LVPECL	Low speed differential parallel data
73	D11+	O	LVPECL	Low speed differential parallel data
74	D11-	O	LVPECL	Low speed differential parallel data
76	D10+	O	LVPECL	Low speed differential parallel data
77	D10-	O	LVPECL	Low speed differential parallel data
79	D9+	O	LVPECL	Low speed differential parallel data
80	D9-	O	LVPECL	Low speed differential parallel data
82	D8+	O	LVPECL	Low speed differential parallel data
83	D8-	O	LVPECL	Low speed differential parallel data
85	D7+	O	LVPECL	Low speed differential parallel data
86	D7-	O	LVPECL	Low speed differential parallel data
88	D6+	O	LVPECL	Low speed differential parallel data
89	D6-	O	LVPECL	Low speed differential parallel data
91	D5+	O	LVPECL	Low speed differential parallel data
92	D5-	O	LVPECL	Low speed differential parallel data
94	D4+	O	LVPECL	Low speed differential parallel data
95	D4-	O	LVPECL	Low speed differential parallel data
97	D3+	O	LVPECL	Low speed differential parallel data
98	D3-	O	LVPECL	Low speed differential parallel data
100	D2+	O	LVPECL	Low speed differential parallel data
101	D2-	O	LVPECL	Low speed differential parallel data
105	D1+	O	LVPECL	Low speed differential parallel data
106	D1-	O	LVPECL	Low speed differential parallel data
108	D0+	O	LVPECL	Low speed differential parallel data

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Pin #	*Name*	*I/O*	*Level*	*Description*
109	D0-	O	LVPECL	Low speed differential parallel data
111	CLK16O-	O	LVPECL	Parallel clock output, complement
112	CLK16O+	O	LVPECL	Parallel clock output, true
114	CLK32O-	O	LVPECL	Divided Parallel clock output, complement
115	CLK32O+	O	LVPECL	Divided Parallel clock output, true
15,18,21, 54,60,64, 66,72,75, 81,84,90, 93,99, 102,103, 107,113	VCC	—	+3.3V typ.	Positive power supply pins
12,16,17, 57,69,78, 87,96, 110	VEE	—	GND typ.	Negative power supply pins
1,2,3,4,5, 6,7,8,9, 10,11,22, 23,24,25, 26,27,28, 29,30,31, 32,33,34, 35,36,37, 38,39,40, 41,42,43, 44,45,46, 47,48,49, 50,51,52, 53,55,56, 63,65, 104,116, 117,118, 119,120, 121,122, 123,124, 125,126, 127,128	NC	—	—	No connect, leave unconnected

Note:No connect (NC) pins must be left unconnected, or floating. Connecting any of these pins to either the positive or negative-power supply rails may cause improper operation or failure of the device; or in extreme cases, cause permanent damage to the device.

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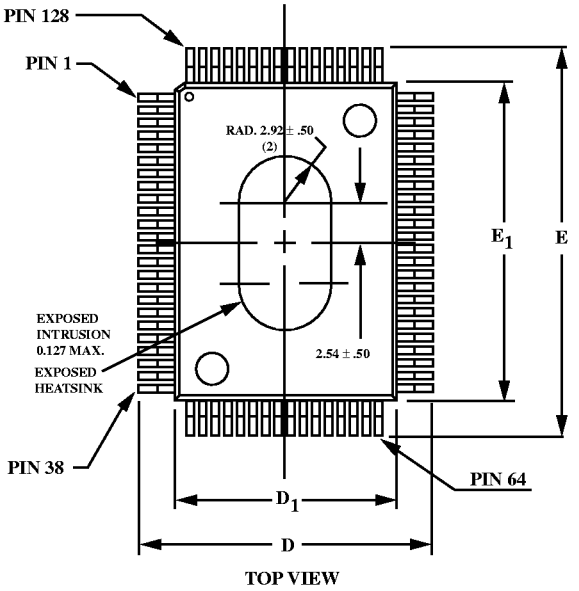
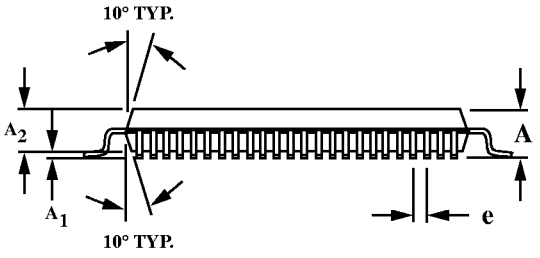
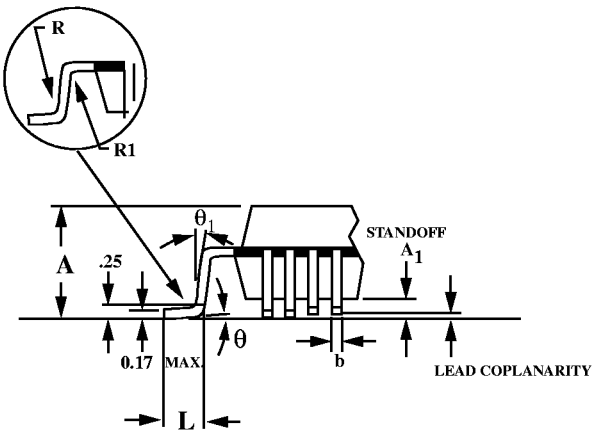
Package Information

128 PQFP Package Drawings



Key	*mm*	*Tolerance*
A	2.35	MAX
A1	0.25	MAX
A2	2.00	+.10
D	17.20	±.20
D1	14.00	±.10
E	23.20	±.20
E1	20.00	±.10
L	.88	+.15/-.10
e	.50	BASIC
b	.22	±.05
θ	0°-7°	
R	.30	TYP
R1	.20	TYP





Notes: 1) Drawing is not to scale
2) All dimensions in mm
3) Package represented is also used for the 64, 80, & 100 PQFP packages. Pin count drawn does not reflect the 128 Package.

NOTES:

Package #: 101-322-5
Issue #: 1

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Thermal Considerations

This package has been enhanced with a copper heat slug to provide a low thermal resistance path from the die to the exposed surface of the heat spreader. The thermal resistance is shown in the following table

Table 4: Thermal Resistance

Symbol	*Description*	*°C/W*
θ_{jc}	Thermal resistance from junction to case.	1.34
θ_{ca}	Thermal resistance from case to ambient with no airflow, including conduction through the leads.	25.0

Thermal Resistance with Airflow

Shown in the table below is the thermal resistance with airflow. This thermal resistance value reflects all the thermal paths including through the leads in an environment where the leads are exposed. The temperature difference between the ambient airflow temperature and the case temperature should be the worst case power of the device multiplied by the thermal resistance.

Table 5: Thermal Resistance with Airflow

Airflow	θ_{ca} (°C/W)
100 lfpm	21
200 lfpm	18
400 lfpm	16
600 lfpm	14.5

Maximum Ambient Temperature without Heatsink

The worst case ambient temperature without use of a heatsink is given by the equation:

$$T_{A(MAX)} = T_{C(MAX)} - P_{(MAX)}\theta_{CA}$$

where:

θ_{CA} Theta case to ambient at appropriate airflow
$T_{A(MAX)}$ Ambient Air temperature
$T_{C(MAX)}$ Case temperature (85°C for VSC8164)
$P_{(MAX)}$ Power (1.1 W for VSC8164)

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The results of this calculation are listed below:

Table 6: Maximum Ambient Air Temperature without Heatsink

Airflow	θ_{ca} (°C/W)
none	58
100 lfpm	62
200 lfpm	65
400 lfpm	67
600 lfpm	69

Note that ambient air temperature varies throughout the system based on the positioning and magnitude of heat sources and the direction of air flow.

Notice

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