Integrated Device Technology, Inc.

4K x 16 FourPort™ STATIC RAM MULTICHIP MODULE

PRELIMINARY
IDT70M74

FEATURES:

- High density 64K-bit FourPort™ static RAM multichip module
- High-speed access
  - — Commercial: 25, 30, 35, 45ns (max.)
  - — Military: 30, 35, 45ns (max.)
- Low-power CEMOS™ operation
- Fully asynchronous read/write operation from each of the four ports: Ports A, B, C, D
- Versatile control for write-inhibit: separate $\overline{BUSY}$ input to control write-inhibit for each of the four ports
- Battery backup operation—2V data retention
- TTL-compatible inputs/outputs
- Single 5V (±10%) power supply
- Available in 180-pin hermetic PGA
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

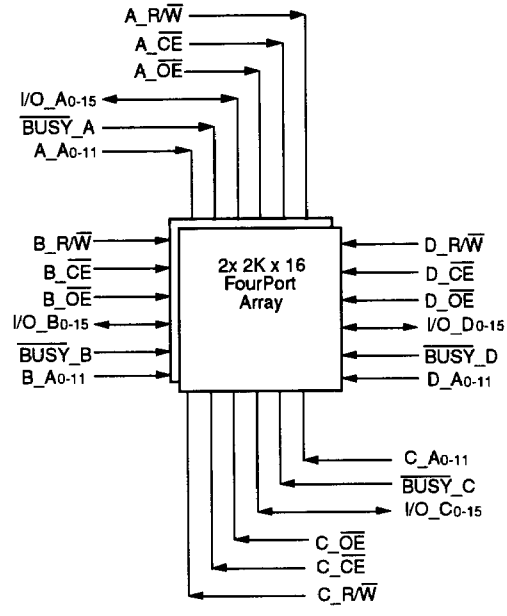
The IDT70M74 is a high-speed 4K x 16 FourPort static RAM multichip module designed to be used in systems where multiple access in a common RAM is required. This FourPort static RAM module offers increased system performance in multiprocesser systems that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

The IDT70M74 provides four independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. Arbitratation is not provided on the module; therefore, it is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from all ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low power standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, this four port RAM module typically operates on only 3W of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 0.5mW from a 2V battery.

The IDT70M74 is packaged in a ceramic, hermetically sealed 180-pin PGA. Military grade product is manufactured in compliance with the latest revision of Mil-Std-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



2817 drw 01

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PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	$\overline{BSY}$_B	R/$\overline{W}$_B(1)	R/$\overline{W}$_B(0)	GND	A_B(7)	A_B(3)	A_B(0)	Vcc	A_C(3)	A_C(7)	GND	R/$\overline{W}$_C(0)	R/$\overline{W}$_C(1)	$\overline{BSY}$_C	GND
B	$\overline{OE}$_B(0)	$\overline{OE}$_B(1)	R/$\overline{W}$_B(2)	$\overline{CE}$_B(2)	$\overline{CE}$_B(0)	A_B(8)	A_B(4)	A_B(1)	A_C(0)	A_C(4)	A_C(8)	$\overline{CE}$_C(0)	$\overline{CE}$_C(2)	R/$\overline{W}$_C(2)	$\overline{OE}$_C(1)	$\overline{OE}$_C(0)
C	$\overline{OE}$_B(2)	$\overline{OE}$_B(3)	R/$\overline{W}$_B(3)	$\overline{CE}$_B(3)	$\overline{CE}$_B(1)	A_B(9)	A_B(5)	A_B(2)	A_C(1)	A_C(5)	A_C(9)	$\overline{CE}$_C(1)	$\overline{CE}$_C(3)	R/$\overline{W}$_C(3)	$\overline{OE}$_C(3)	$\overline{OE}$_C(2)
D	A_A(0)	A_A(1)	A_A(2)			A_B(10)	A_B(6)	GND	A_C(2)	A_C(6)	A_C(10)			A_D(2)	A_D(1)	A_D(0)
E	GND	A_A(3)	A_A(4)											A_D(4)	A_D(3)	GND
F	A_A(5)	A_A(6)	A_A(7)	A_A(8)									A_D(8)	A_D(7)	A_D(6)	A_D(5)
G	A_A(9)	$\overline{CE}$_A(0)	$\overline{CE}$_A(1)	A_A(10)									A_D(10)	$\overline{CE}$_D(1)	$\overline{CE}$_D(0)	A_D(9)
H	VCC	$\overline{CE}$_A(2)	$\overline{CE}$_A(3)	GND				**TOP VIEW**					GND	$\overline{CE}$_D(3)	$\overline{CE}$_D(2)	Vcc
J	R/$\overline{W}$_A(0)	R/$\overline{W}$_A(1)	R/$\overline{W}$_A(2)	R/$\overline{W}$_A(3)									R/$\overline{W}$_D(3)	R/$\overline{W}$_D(2)	R/$\overline{W}$_D(1)	R/$\overline{W}$_D(0)
K	$\overline{OE}$_A(0)	$\overline{OE}$_A(1)	$\overline{OE}$_A(2)	$\overline{OE}$_A(3)									$\overline{OE}$_D(3)	$\overline{OE}$_D(2)	$\overline{OE}$_D(1)	$\overline{OE}$_D(0)
L	I/O_A(0)	I/O_A(1)	I/O_A(2)	$\overline{BSY}$_A									$\overline{BSY}$_D	I/O_D(2)	I/O_D(1)	I/O_D(0)
M	GND	I/O_A(3)	I/O_A(4)											I/O_D(4)	I/O_D(3)	GND
N	I/O_A(5)	I/O_A(6)	I/O_A(7)	GND		I/O_B(8)	I/O_B(12)	I/O_B(15)	GND	I/O_C(12)	I/O_C(8)			I/O_D(7)	I/O_D(6)	I/O_D(5)
P	I/O_A(8)	I/O_A(9)	I/O_A(10)	I/O_B(2)	I/O_B(4)	I/O_B(7)	I/O_B(11)	I/O_B(14)	I/O_C(15)	I/O_C(11)	I/O_C(7)	I/O_C(4)	I/O_C(2)	I/O_D(10)	I/O_D(9)	I/O_D(8)
Q	I/O_A(11)	I/O_A(12)	I/O_A(13)	I/O_B(1)	I/O_B(3)	I/O_B(6)	I/O_B(10)	I/O_B(13)	I/O_C(14)	I/O_C(10)	I/O_C(6)	I/O_C(3)	I/O_C(1)	I/O_D(13)	I/O_D(12)	I/O_D(11)
R		I/O_A(14)	I/O_A(15)	I/O_B(0)	GND	I/O_B(5)	I/O_B(9)	Vcc	I/O_C(13)	I/O_C(9)	I/O_C(5)	GND	I/O_C(0)	I/O_D(15)	I/O_D(14)	GND

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PIN NAMES

Symbol	Pin Name
A_A(0-11)	Address Inputs – Port A
A_B(0-11)	Address Inputs – Port B
A_C(0-11)	Address Inputs – Port C
A_D(0-11)	Address Inputs – Port D
I/O_A(0-15)	Data I/O – Port A
I/O_B(0-15)	Data I/O – Port B
I/O_C(0-15)	Data I/O – Port C
I/O_D(0-15)	Data I/O – Port D
R/$\overline{W}$_A(0-3)	Read/Write – Port A
R/$\overline{W}$_B(0-3)	Read/Write – Port B
R/$\overline{W}$_C(0-3)	Read/Write – Port C
R/$\overline{W}$_D(0-3)	Read/Write – Port D
$\overline{CE}$_A(0-3)	Chip Enable – Port A
$\overline{CE}$_B(0-3)	Chip Enable – Port B
$\overline{CE}$_C(0-3)	Chip Enable – Port C
$\overline{CE}$_D(0-3)	Chip Enable – Port D
$\overline{OE}$_A(0-3)	Output Enable – Port A
$\overline{OE}$_B(0-3)	Output Enable – Port B
$\overline{OE}$_C(0-3)	Output Enable – Port C
$\overline{OE}$_D(0-3)	Output Enable – Port D
$\overline{BUSY}$_A	Write Disable – Port A
$\overline{BUSY}$_B	Write Disable – Port B
$\overline{BUSY}$_C	Write Disable – Port C
$\overline{BUSY}$_D	Write Disable – Port D
VCC	Power
GND	Ground

2817 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2817 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	50	pF
COUT	Output Capacitance	VOUT = 0V	50	pF

2817 tbl 03

NOTE:
1. This parameter is guaranteed by design, but not tested

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2817 tbl 04

TRUTH TABLE

Any Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D0-15	Function
X	H	X	Z	Port Disabled and in Power Down Mode
X	H	X	Z	$\overline{CE}_{P1}$ = $\overline{CE}_{P2}$ = $\overline{CE}_{P3}$ = $\overline{CE}_{P4}$ = H Power Down Mode, ISB or ISB1
L	L	X	DATAIN	Data on port written into memory(2, 3)
H	L	L	DATAOUT	Data in memory output on port
X	X	H	Z	High impedance outputs

2817 tbl 06

NOTES:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance
2. If $\overline{BUSY}$ = LOW, data is not written.
3. For valid write operation, no more than one port can write to the same address location at the same time.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

2817 tbl 05

NOTE:
1. VIL (min.) = -3.0V for pulse width less than 20ns.

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DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A=-55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT70M74 Min.	IDT70M74 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	40	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	40	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	V

2817 tbl 07

DC ELECTRICAL CHARACTERISTICS(1, 5, 6)

(V_{CC} = 5.0V ± 10%, T_A=-55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Condition	Version	-25ns(2) Typ.	-25ns(2) Max.	-30ns Typ.	-30ns Max.	-35ns Typ.	-35ns Max.	-45ns Typ.	-45ns Max.	Unit
I_{CC1}	Operating Power Supply Current (All Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = 0(3)	Military	—	—	600	1440	600	1440	600	1440	mA
			Commercial	600	1200	600	1200	600	1200	600	1200	
I_{CC2}	Dynamic Operating Current (All Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = f_{MAX}(4)	Military	—	—	880	1600	840	1580	780	1560	mA
			Commercial	900	1400	880	1360	840	1340	780	1320	
I_{SB}	Standby Current (All Ports — TTL Level Inputs)	$\overline{CE} \ge V_{IH}$ f = f_{MAX}(4)	Military	—	—	180	460	160	440	140	420	mA
			Commercial	240	340	180	320	160	300	140	280	
I_{SB1}	Full Standby Current (All Ports — All CMOS Level Inputs)	All Ports $\overline{CE} \ge V_{CC}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V, f = 0(3)	Military	—	—	6	120	6	120	6	120	mA
			Commercial	6	60	6	60	6	60	6	60	

2817 tbl 08

NOTES:
1. V_{CC} = 5V, T_A = +25°C for Typ.
2. 0°C to +70°C temperature range only.
3. f = 0 means no address or control lines change.
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
5. For the case of one port, divide the above appropriate current by four.
6. Typical values are guaranteed by design but not tested.

DATA RETENTION CHARACTERISTICS(1)(L VERSION ONLY)

(V_{CC} = 5.0V ± 10%, T_A=-55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Condition		Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \ge V_{HC}$ $V_{IN} \ge V_{HC}$ or $\le V_{LC}$	Military	—	100	7200	µA
			Commercial	—	100	2400	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	ns

2817 tbl 09

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed by design, but not tested.

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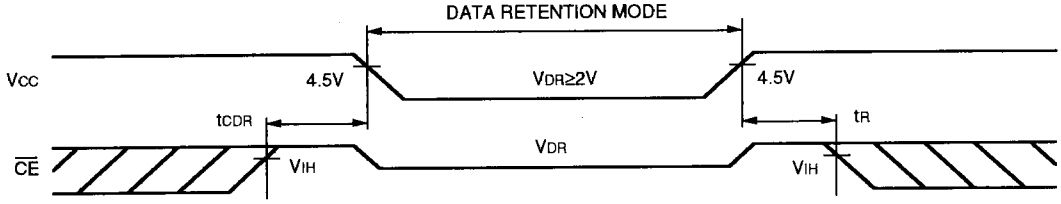
LOW Vcc DATA RETENTION WAVEFORM

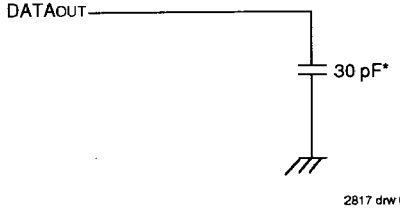


2817 drw 03

AC TEST CONDITIONS

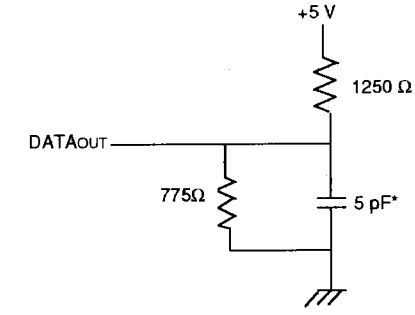
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2817 tbl 10



2817 drw 04

Figure 1. Output Load



2817 drw 05

Figure 2. Output Load (for tOLZ, tOHZ, tWHZ, tOW)

*Including scope and jig

AC ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V ± 10%, TA=-55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	-25ns(3) Min.	-25ns(3) Max.	-30ns Min.	-30ns Max.	-35ns Min.	-35ns Max.	-45ns Min.	-45ns Max.	Unit
READ CYCLE										
tRC	Read Cycle Time	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	25	—	30	—	35	—	45	ns
tACE	Chip Enable Access Time	—	25	—	30	—	35	—	45	ns
tOE	Output Enable Access Time	—	15	—	20	—	25	—	30	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	ns
tOLZ(1, 2)	$\overline{OE}$ Enable to Output in Low Z	3	—	3	—	5	—	5	—	ns
tOHZ(1, 2)	$\overline{OE}$ Disable to Output in High Z	—	15	—	15	—	15	—	20	ns
tCLZ(1, 2)	$\overline{CE}$ Enable to Output in Low Z	3	—	3	—	5	—	5	—	ns
tCHZ(1, 2)	$\overline{CE}$ Disable to Output in High Z	—	15	—	15	—	15	—	20	ns
tPU(2)	Chip Enable to Power Up Time	0	—	0	—	0	—	0	—	ns
tPD(2)	Chip Disable to Power Down Time	—	20	—	30	—	50	—	50	ns

2817 tbl 11

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed by design, but not tested.
3. 0°C to +70°C temperature range only.

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AC ELECTRICAL CHARACTERISTICS

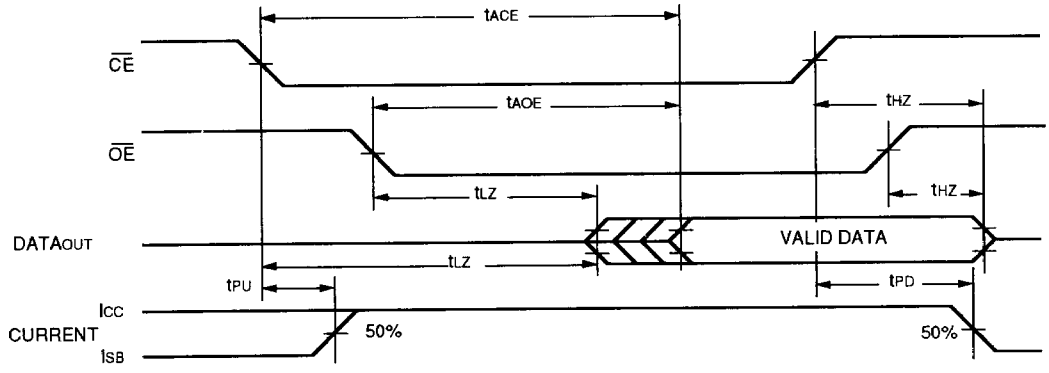
(V_{CC} = 5.0V ± 10%, T_A=-55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	-25ns[7]		-30ns		-35ns		-45ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
t_{WC}	Write Cycle Time	25	—	30	—	35	—	45	—	ns
t_{CE}	Chip Enable to End of Write	20	—	25	—	30	—	35	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}[3]	Write Pulse Width	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	5	—	ns
t_{DW}	Data Valid to End of Write	15	—	15	—	20	—	20	—	ns
t_{OHZ}[1, 2]	$\overline{OE}$ to Output in High Z	—	15	—	15	—	15	—	20	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1, 2]	Write Enabled to Output in High Z	—	15	—	15	—	15	—	20	ns
t_{OW}[1, 2]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns
t_{WDD}[4]	Write Pulse to Data Delay	—	45	—	50	—	55	—	65	ns
t_{DDD}[4]	Write Data Valid to Read Data Delay	—	35	—	40	—	45	—	55	ns
$\overline{BUSY}$ CYCLE										
t_{WB}[5]	Write to $\overline{BUSY}$	0	—	0	—	0	—	0	—	ns
t_{WH}[6]	Write Hold After $\overline{BUSY}$	15	—	20	—	20	—	20	—	ns

2817 tbl 12

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed by design, but not tested.
3. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read with Port-to-Port Delay".
5. To ensure that the write cycle is inhibited during contention.
6. To ensure that a write cycle is completed after contention.
7. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF READ CYCLE NO. 1, ANY PORT[1, 3]



2817 drw 06

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.

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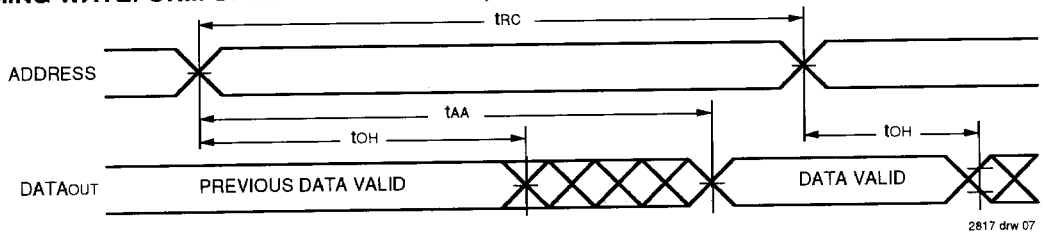
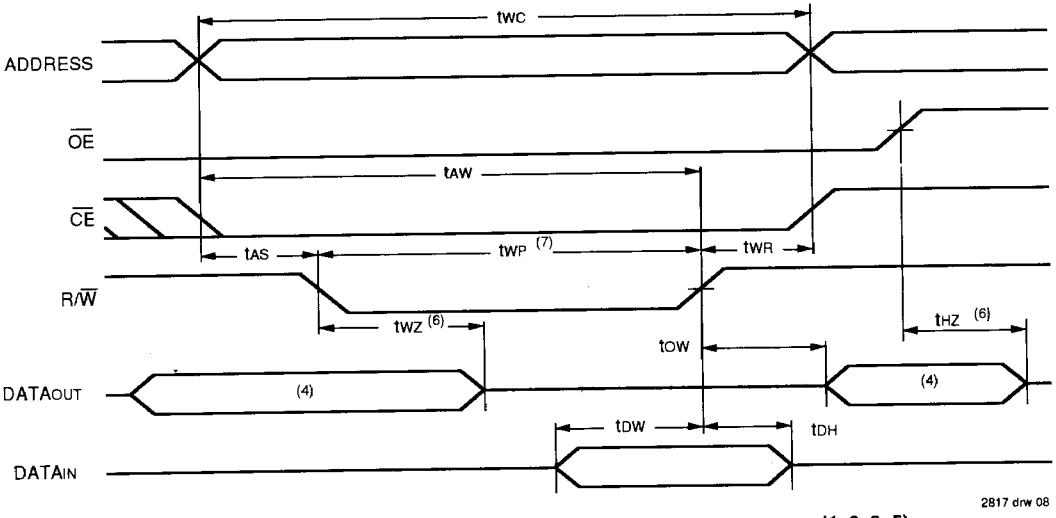
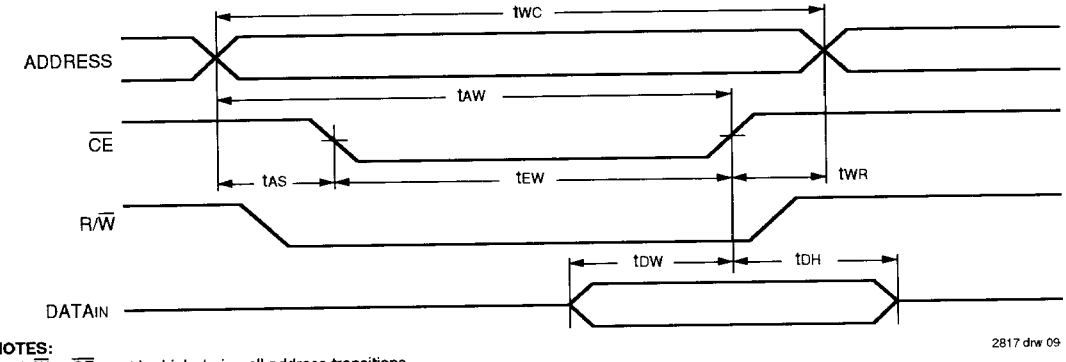
TIMING WAVEFORM OF READ CYCLE NO. 2, ANY PORT(1, 2, 4)



TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1, 2, 3, 7)

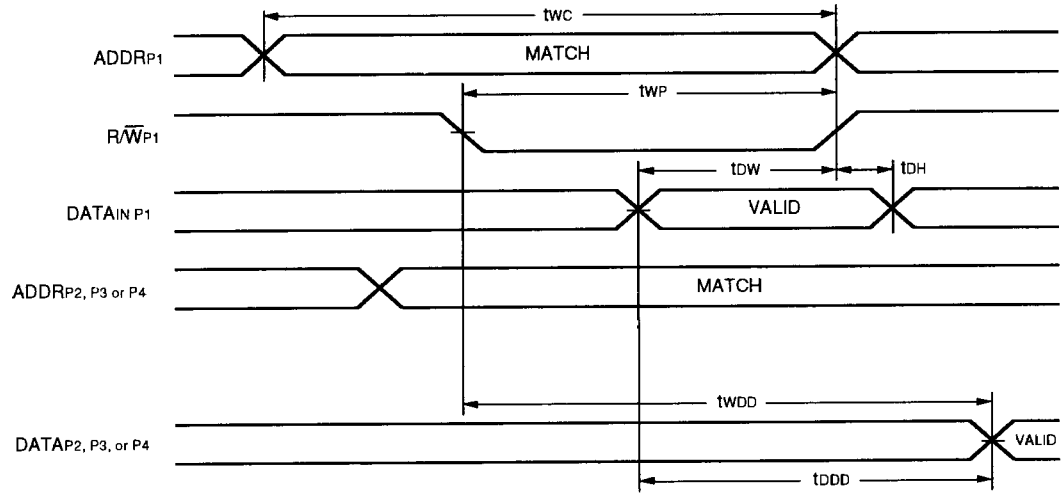


TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1, 2, 3, 5)



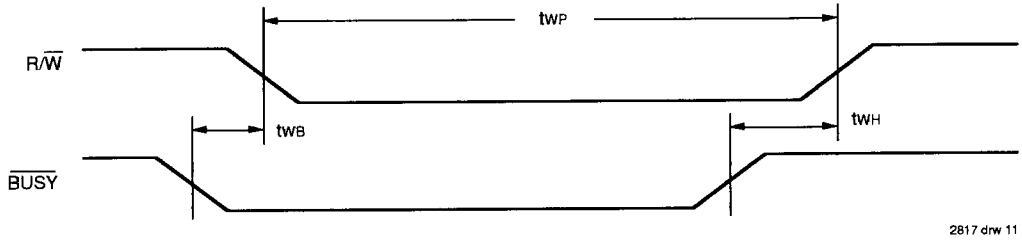
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY(1, 2, 3)



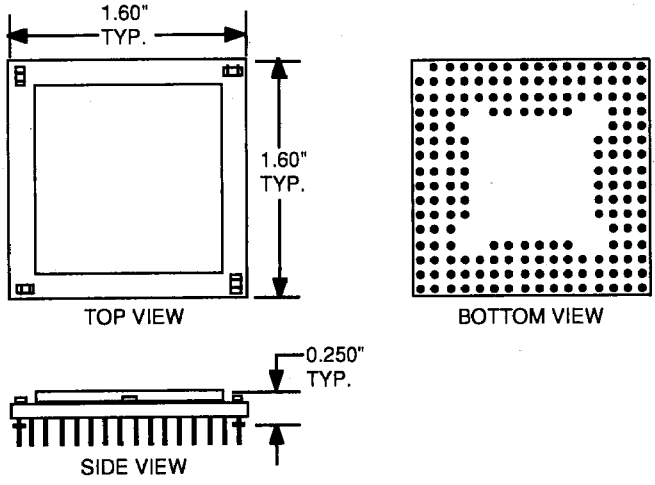
NOTES:
1. Assume $\overline{BUSY}$ input at HIGH and $\overline{CE}$ at LOW for the writing port.
2. Write cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for any of the reading ports which has its $\overline{OE}$ at LOW.

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT



7-2-8

PACKAGE DIMENSIONS



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7-29