Inphi
Think fast.

INSSTU32S868
INSSTUA32S868
INSSTUB32868
INSSTUB32868H

DDR2 Configurable Registered Buffer with Parity Checking
Data Sheet

Applications

- High Performance Workstations
- Mid and High Performance Servers
- High Reliability Systems

Features

- INSSTU32S868 meets or exceeds all JESD82-14 performance specifications up to DDR2-533 rates
- INSSTUA32S868 meets or exceeds all JESD82-16 performance specifications up to DDR2-667 rates
- INSSTUB32868 and INSSTUB32868H meets or exceeds all JESDxx-x performance specifications up to DDR2-800 rates
- INSSTUB32868H outputs drive up to 50% more load capacitance for heavily loaded RDIMMs
- Supports RDIMM modules K, L, M and P
- Complies with DDR2 SDRAM Over/Undershoot specification as defined in JESD79-2
- Single die solution for lowest input capacitance
- Available in 176-Ball TFBGA "Green" Package
- Pull-down resistors on all data and parity inputs
- Latch-up exceeds JESD78 class 2
- ESD protection exceeds JESD22

Description

This 28-bit 1:2 configurable register is designed for nominal 1.8V power supply operation. All inputs are SSTL_18 compatible except for the 1.8V LVCMOS reset ($\overline{\text{RESET}}$), chip-select gate enable (CSGEN) and control (C). The INSSTU32S868 operates with a differential clock input (CK and $\overline{CK}$). Input data is registered at the crossing point of rising CK and falling $\overline{CK}$.

The INSSTU32S868 supports low-power standby mode. When $\overline{RESET}$ is low, the clock, data, and reference voltage (V_{REF}) input receivers are disabled and floating clock, data, and reference inputs are allowed. Additionally, all registers are reset, and all outputs are forced low.

The $\overline{RESET}$ input must be held at a valid logic level. Asynchronous transitions of $\overline{RESET}$ are supported. $\overline{RESET}$ must always be held low during power-up to ensure well-defined outputs from the register before a stable clock has been supplied.

The INSSTU32S868 continually evaluates parity of the data inputs and a parity input bit generated by the memory controller (PAR_IN). Valid parity is defined as even, i.e. an even number of ones among the data inputs and PAR_IN. The DIMM-dependent DCKE0, DCKE1, $\overline{DCS0}$, $\overline{DCS1}$, DODT0 and DODT1 are omitted from parity evaluation. (The PAR_IN input is compared with the data received on the DIMM-independent D-inputs: D1-5, D7, D9-12, D17-28 when C=0; or D1-12, D17-20, D22, D24-28 when C=1.)

Parity is evaluated on the PAR_IN input, which arrives one cycle after the corresponding input data. The parity error ($\overline{QERR}$) output signal is generated three positive clock transitions after the corresponding data inputs, to which the $\overline{QERR}$ signal applies. $\overline{QERR}$ goes low if an error is detected.

Once an error occurs the $\overline{QERR}$ output is driven low for a minimum of two clock cycles or until $\overline{RESET}$ is driven low. N consecutive parity errors will cause $\overline{QERR}$ to stay low N+1 clock cycles.

The C input controls the pinout configuration from register-A configuration (C=0) to register-B configuration (C=1). The C input should not be switched during normal operation, but rather it should be hardwired to configure the register in the desired mode.

The device supports low-power active operation by monitoring both system chip select ($\overline{DCS0}$ and $\overline{DCS1}$) and CSGEN inputs and will prevent the Qn outputs from changing states when CSGEN, $\overline{DCS0}$ and $\overline{DCS1}$ inputs are all high. If any of CSGEN, $\overline{DCS0}$ or $\overline{DCS1}$ inputs is low, then Qn outputs will function normally. If both $\overline{DCS0}$ and $\overline{DCS1}$ are high, the device will prevent the $\overline{QERR}$ output from changing states. If either $\overline{DCS0}$ or $\overline{DCS1}$ is low, the $\overline{QERR}$ output will function normally.

The $\overline{RESET}$ input has priority over $\overline{DCS0}$ and $\overline{DCS1}$ inputs, and when driven low, will force the Qn outputs to be low, and the $\overline{QERR}$ to be high. If the chip-select control functionality is not desired, then the CSGEN input can be hard-wired to ground, in which case, the setup-time requirement for $\overline{DCS0}$ and $\overline{DCS1}$ would be the same as for the other Dn data inputs. To control the low-power mode with $\overline{DCS0}$ and $\overline{DCS1}$ only, the CSGEN input should be hard-wired to V_{DD} through a pull-up resistor.

The two V_{REF} pins are connected together internally with a 150 Ω resistor. However, it is necessary to connect only one of the two V_{REF} pins to the external V_{REF} power supply. An unused V_{REF} pin should be terminated with a V_{REF} coupling capacitor.

Part Number Selection Table

This register is certified for use on the Raw Cards listed below as defined in JESD21-C, DDR2 Registered DIMM Design Specification. It is guaranteed to produce over/undershoots less than indicated in the table below to comply with DDR2 SDRAM over/undershoot requirements under worst-case DRAM loading conditions (Min or Max) and DIMM operating conditions, when operated within the recommended operating conditions listed in Table 5 of the relevant JESDxx-x register definition standard.

Inphi Product Part Number	RDIMM Module	Speed Bin	Max Overshoot	Min Overshoot
INSSTU32S868	K, L, P	400, 533	0.5V	0.5V
INSSTUA32S868	K, L, P	400, 533, 667	0.5V	0.5V
INSSTUB32868	K, L, P	400, 533, 667, 800	0.5V	0.5V
INSSTUB32868H	M	400, 533, 667	0.5V	0.5V

Terminal Functions

Terminal Name	Description	Electrical Characteristics
GND	Ground	Ground
V_{DD}	Power supply	1.8 V nominal
V_{REF}	Input reference voltage	0.9 V nominal
CK	Clock input	SSTL_18 Differential input
$\overline{CK}$	Complementary clock input	SSTL_18 Differential input
C	Configuration control input – Register A or Register B	LVCMOS input
$\overline{RESET}$	Asynchronous reset input: resets registers and disables V_{REF}, data and clock input receivers	LVCMOS input
CSGEN	Chip select gate enable – When high, D1-D28[1] inputs will be latched only when at least one chip select input is low during the rising edge of the clock. When low, the D1-D28[1] inputs will be latched and re-driven on every rising edge of the clock.	LVCMOS input
D1-D28	Data inputs - clocked in on the crossing of rising edge of CK and falling edge of $\overline{CK}$	SSTL_18 inputs
$\overline{DCS0}$, $\overline{DCS1}$	Chip select inputs – These pins initiate DRAM address/command decodes, and as such at least one will be low when a valid address/command is present. The Register can be programmed to re-drive all D inputs (CSGEN = 1) only when at least one chip select input is low. If CSGEN, $\overline{DCS0}$ and $\overline{DCS1}$ inputs are high, then D-D28[1] inputs will be latched to their prior state.	SSTL_18 inputs

Terminal Functions (cont'd.)

Terminal Name	Description	Electrical Characteristics
DODT0, DODT1, DCKE0, DCKE1	The outputs of these register bits will not be suspended by the $\overline{\mathrm{DCS0}}$ & $\overline{\mathrm{DCS1}}$ controls.	SSTL_18 inputs
PAR_IN	Parity input – arrives two clock cycle after corresponding data input	SSTL_18 input
Q1-Q28[2]	Data outputs that are suspended by the $\overline{\mathrm{DCS0}}$ & $\overline{\mathrm{DCS1}}$ controls	1.8 V CMOS outputs
$\overline{\mathrm{QCS0}}$, $\overline{\mathrm{QCS1}}$	Data outputs that are not suspended by the $\overline{\mathrm{DCS0}}$ & $\overline{\mathrm{DCS1}}$ controls	1.8 V CMOS output
QODT0, DODT1, QCKE0, QCKE1	Data outputs that are not suspended by the $\overline{\mathrm{DCS0}}$ & $\overline{\mathrm{DCS1}}$ controls	1.8 V CMOS outputs
$\overline{\mathrm{QERR}}$	Parity error output – generated one clock cycle after corresponding data output	Open-drain output
NC	No connect. Ball present but no internal connection to the die.	May connect to PCB

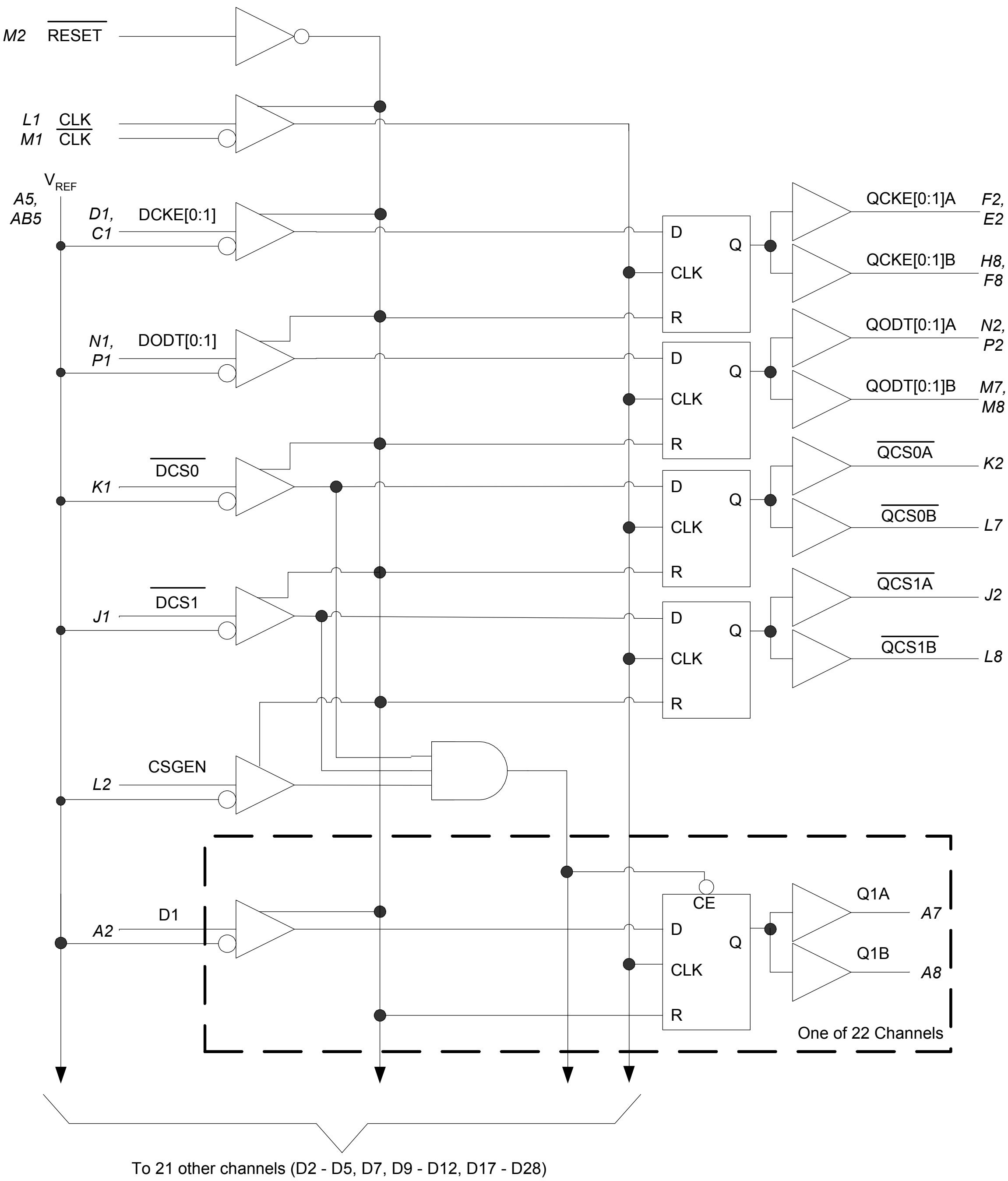
Notes:

[1] Data inputs are:
D1-5, D7, D9-12, D17-28 when C=0
D1-12, D17-20, D22, D24-28 when C=1

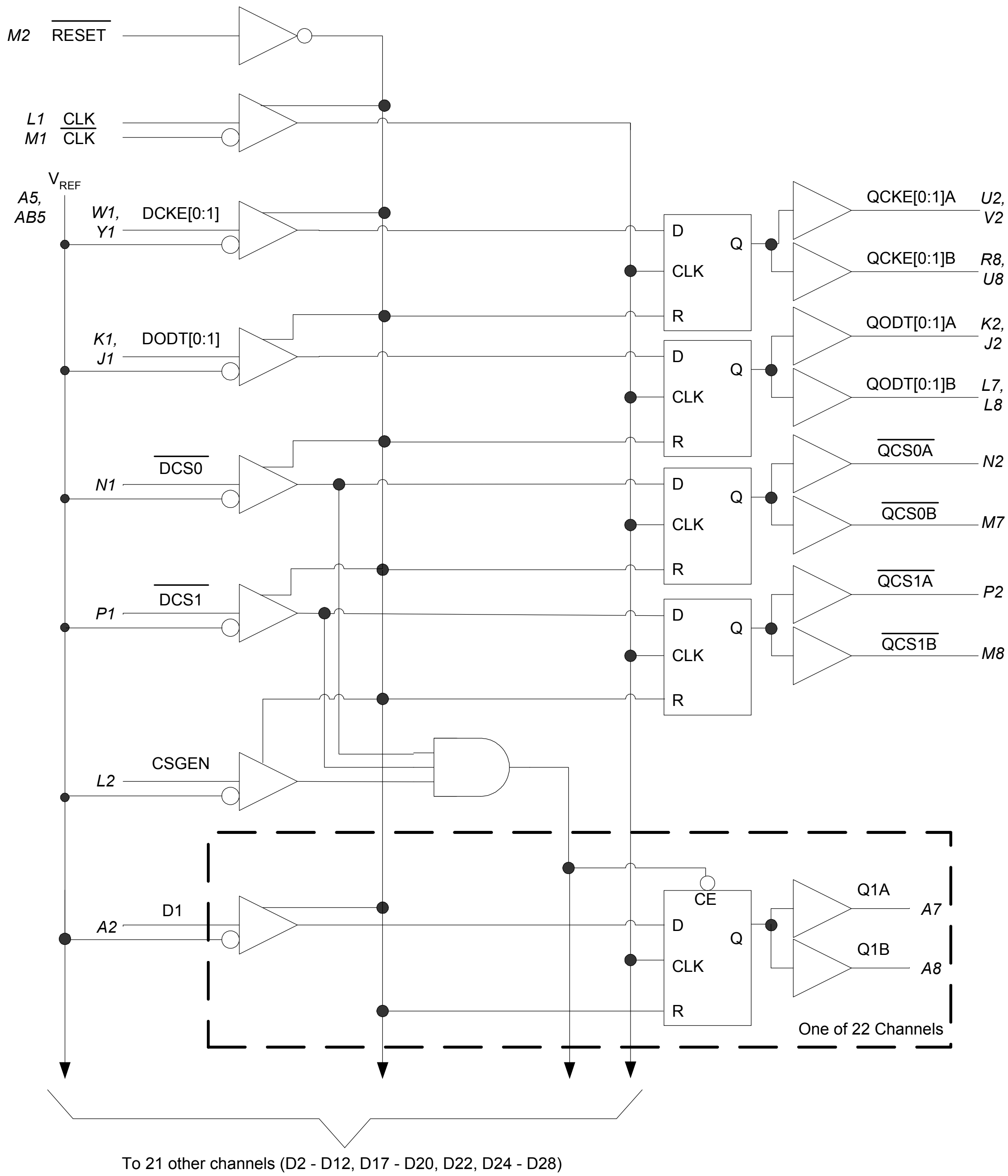
[2] Data outputs are:
Q1-5, Q7, Q9-12, Q17-28 when C=0
Q1-12, Q17-20, Q22, Q24-28 when C=1

Block Diagrams

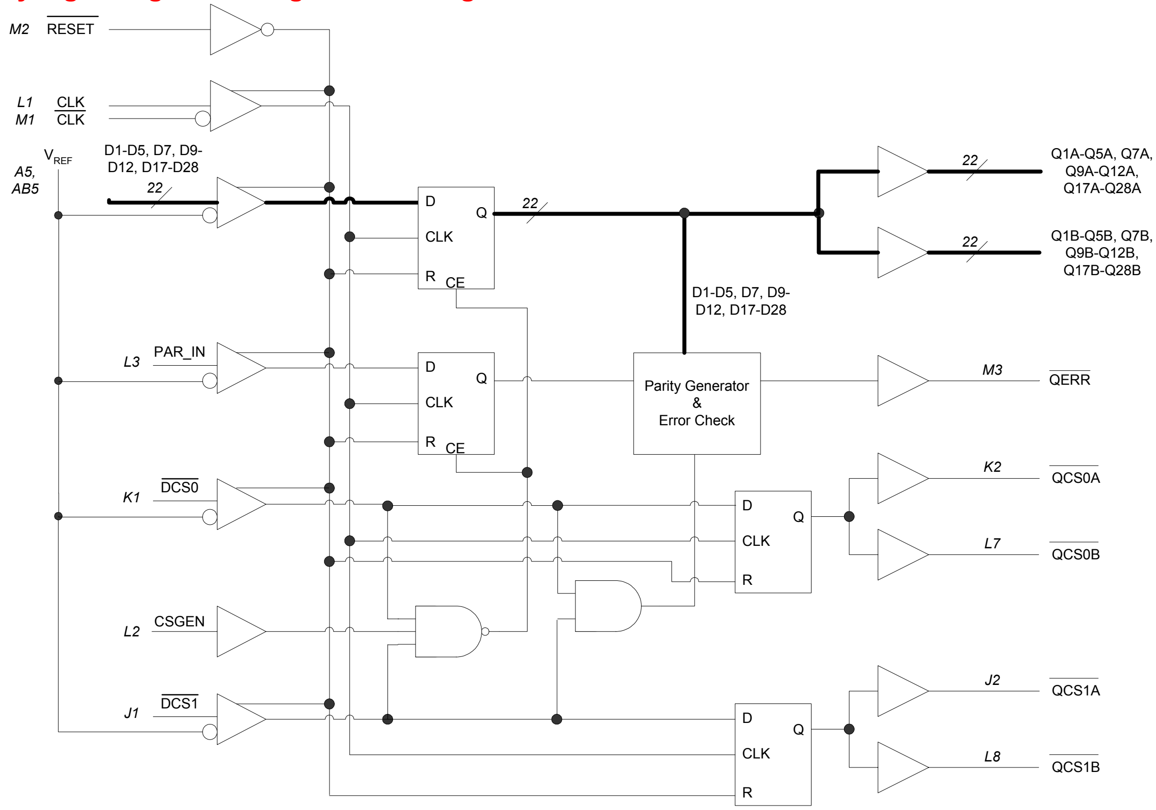
Logic diagram for register-A configuration with C=0



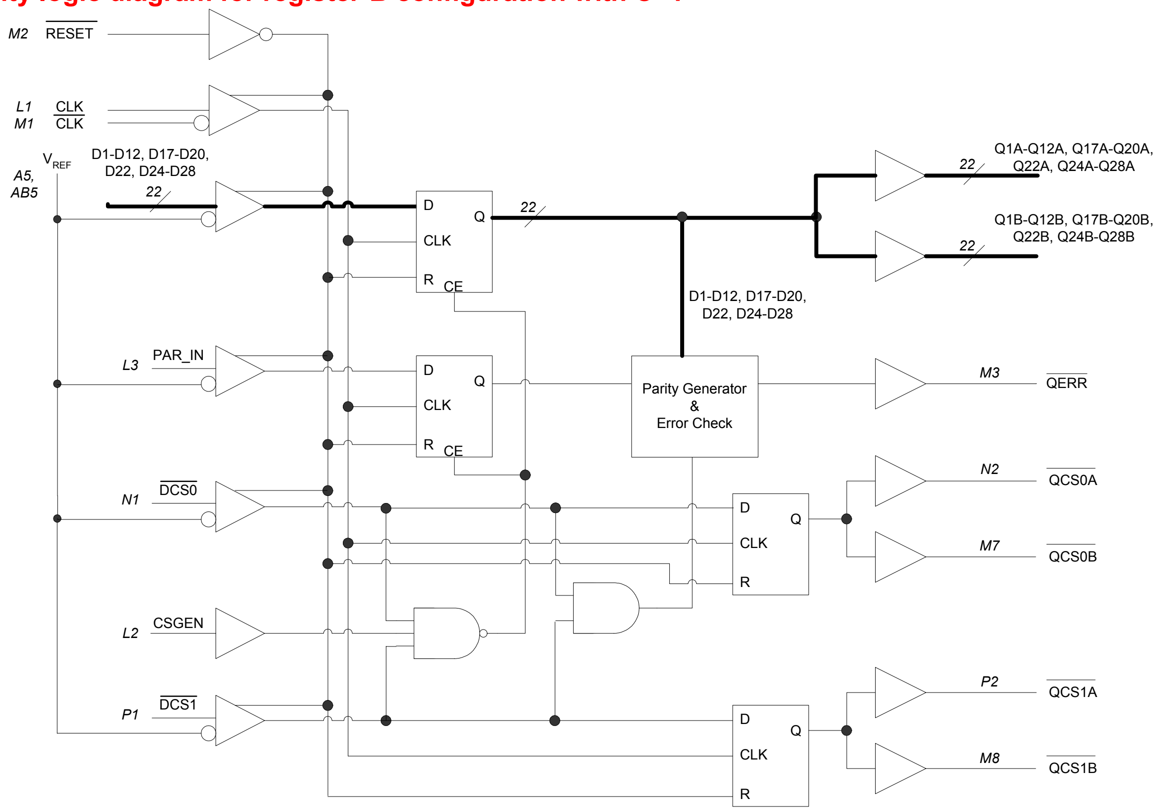
Logic diagram for register-B configuration with C=1



Parity logic diagram for register-A configuration with C=0



Parity logic diagram for register-B configuration with C=1



Function Table

Inputs							Outputs			
$\overline{\text{RESET}}$	$\overline{\text{DCS0}}$	$\overline{\text{DCS1}}$	CSGEN	CK	$\overline{\text{CK}}$	Dn, DODTn, DCKEn[1]	Qn[1]	$\overline{\text{QCS0}}$	$\overline{\text{QCS1}}$	QODT, QCKE
H	L	L	X	↑	↓	L	L	L	L	L
H	L	L	X	↑	↓	H	H	L	L	H
H	L	L	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	L	H	X	↑	↓	L	L	L	H	L
H	L	H	X	↑	↓	H	H	L	H	H
H	L	H	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	L	X	↑	↓	L	L	H	L	L
H	H	L	X	↑	↓	H	H	H	L	H
H	H	L	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	H	L	↑	↓	L	L	H	H	L
H	H	H	L	↑	↓	H	H	H	H	H
H	H	H	L	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	H	H	↑	↓	L	Q_0	H	H	L
H	H	H	H	↑	↓	H	Q_0	H	H	H
H	H	H	H	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L	L

Notes:

[1] Inputs D6, D8, D13, D14-16 (Type A) and inputs D13, D14, D15, D21, D23 (Type B) and their corresponding outputs Qn are not included in this range.

Parity and Standby Function Table

Inputs							Output
$\overline{RESET}$	$\overline{DCS0}$	$\overline{DCS1}$	CK	$\overline{CK}$	Σ of inputs = H (D1-D28)[1]	PAR_IN[2]	$\overline{QERR}$ [3]
H	L	X	↑	↓	Even	L	H
H	L	X	↑	↓	Odd	L	L
H	L	X	↑	↓	Even	H	L
H	L	X	↑	↓	Odd	H	H
H	X	L	↑	↓	Even	L	H
H	X	L	↑	↓	Odd	L	L
H	X	L	↑	↓	Even	H	L
H	X	L	↑	↓	Odd	H	H
H	H	H	↑	↓	X	X	$\overline{QERR}_0$
H	X	X	L or H	L or H	X	X	$\overline{QERR}_0$
L	X or Floating	X or Floating	X or Floating	X or Floating	X	X or Floating	H

Notes:

[1] Inputs D6, D8, D13, D14-16 (Type A) and inputs D13, D14, D15, D21, D23 (Type B) and their corresponding outputs Qn are not included in this range.

[2] PAR_IN arrives one clock cycle after the corresponding data.

[3] This output assumes that $\overline{QERR}$ is high at the rising edge of CK and falling edge of $\overline{CK}$. If $\overline{QERR}$ is low, it latches low for two clock cycles or until $\overline{RESET}$ is driven low.

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}		-0.5		+2.5	V
Input Voltage Range[1]	V_I		-0.5		+2.5	V
Output Voltage Range[1]	V_O		-0.5		V_{DD} +0.5	V
Input clamp current	I_{IK}	$V_I < 0$ or $V_I > V_{DD}$			±50	mA
Output clamp current	I_{OK}	$V_O < 0$ or $V_O > V_{DD}$			±50	mA
Continuous output current	I_O	$0 < V_O < V_{DD}$			±50	mA
Continuous current through each V_{DD} or GND pin					±100	mA
Shipping/Storage Temperature	T_{STORE}		-65		+150	°C

Note:
[1] Limited to 2.5 V

Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		1.7		1.9	V
Reference voltage	V_{REF}		0.49 * V_{DD}	0.5 * V_{DD}	0.51 * V_{DD}	V
Termination voltage	V_{TT}		V_{REF} – 40 mV	V_{REF}	V_{REF} + 40 mV	V
Input voltage	V_I		0		V_{DD}	V
AC high-level input voltage[1]	$V_{IH\ (AC)}$	SSTL_18 inputs	V_{REF} + 250 mV			V
AC low-level input voltage[1]	$V_{IL\ (AC)}$	SSTL_18 inputs			V_{REF} – 250 mV	V
DC high-level input voltage[1]	$V_{IH\ (DC)}$	SSTL_18 inputs	V_{REF} + 125 mV			V
DC low-level input voltage[1]	$V_{IL\ (DC)}$	SSTL_18 inputs			V_{REF} – 125 mV	V
High-level input voltage[2]	V_{IH}	1.8V LVCMOS inputs	0.65 * V_{DD}		V_{DD}	V
Low-level input voltage[2]	V_{IL}	1.8V LVCMOS inputs			0.35 * V_{DD}	V
Common-mode input range	V_{ICR}	CK, $\overline{CK}$ inputs	0.675		1.125	V
Differential input range	V_{ID}	CK, $\overline{CK}$ inputs	600			mV
High-level output current	I_{OH}				-6	mA
Low-level output current	I_{OL}				6	mA
QERR LOW-level output current	I_{ERROL}		25			mA
Operating free-air temperature	T_A		0		70	°C

Notes:
[1] See Figure 4 for definition.
[2] The $\overline{RESET}$ and C inputs of the device must be held at valid levels (i.e. not floating) to ensure proper device operation. The differential inputs must not be floating, unless $\overline{RESET}$ is low.

DC Specifications

Parameter	Symbol	Input Conditions	Output Condition	V_{DD}	Min	Typ	Max	Unit
High-level output voltage	V_{OH}	I_{OH} = -6 mA		1.7 V	1.2			V
Low-level output voltage	V_{OL}	I_{OL} = 6 mA		1.7 V			0.5	V
Input current, all inputs	I_I	$V_I = V_{DD}$ or GND		1.9 V			±5	µA
Static power supply current, standby	I_{DD}	$\overline{RESET}$ = GND	$I_O = 0$	1.9 V		1	50	µA
Static power supply current, active	I_{DD}	$\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$	$I_O = 0$	1.9 V		5		mA
Dynamic supply current, clock only active	I_{DDD}	$\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CK and $\overline{CK}$ switching 50% duty cycle	$I_O = 0$	1.9 V		70		µA / clock MHz
Dynamic supply current, per each active data input, 1:2 mode	I_{DDD}	$\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CK and $\overline{CK}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle	$I_O = 0$	1.9 V		28		µA / clock MHz / data input
Input capacitance, data inputs, $\overline{DCS}$	C_i	$V_I = V_{REF}$ ± 250 mV		1.8 V	2		3.5	pF
Input capacitance, CK and $\overline{CK}$	C_i	V_{ICR} = 0.9 V, V_{ID} = 600 mV		1.8 V	2		3	pF
Input capacitance, $\overline{RESET}$	C_i	$V_I = V_{DD}$ or GND		1.8 V	2		3.5	pF

Timing Requirements

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Clock Frequency	f_{CLK}	INSSTU32S868			270	MHz
		INSSTUA32S868, INSSTUB32868, INSSTUB32868H			410	MHz
Pulse duration[4]	t_W	CK, $\overline{CK}$ high or low	1			ns
Differential inputs active time[1, 3]	t_{act}				10	ns
Differential inputs inactive time[2, 3]	t_{inact}		15			ns
Setup time[5]	t_{su}	$\overline{DCS}$ before CK $\uparrow$, $\overline{CK}$ $\downarrow$, for CSGEN high CSGEN before CK $\uparrow$, $\overline{CK}$ $\downarrow$, for $\overline{DCS}$ high INSSTU32868, INSSTUA32868	0.7			ns
		$\overline{DCS}$ before CK $\uparrow$, $\overline{CK}$ $\downarrow$, for CSGEN high CSGEN before CK $\uparrow$, $\overline{CK}$ $\downarrow$, for $\overline{DCS}$ high INSSTUB32868, INSSTUB32868H	0.6			ns
		$\overline{DCS}$ before CK $\uparrow$, $\overline{CK}$ $\downarrow$, for CSGEN low	0.5			ns
		DCKE, DODT, and Dn before CK $\uparrow$, $\overline{CK}$ $\downarrow$	0.5			ns
		PAR_IN before CK $\uparrow$, $\overline{CK}$ $\downarrow$	0.5			ns
Hold time[5]	t_h	$\overline{DCS}$, DCKE, DODT, and Dn after CK $\uparrow$, $\overline{CK}$ $\downarrow$ INSSTU32868, INSSTUA32868	0.5			ns
		$\overline{DCS}$, DCKE, DODT, and Dn after CK $\uparrow$, $\overline{CK}$ $\downarrow$ INSSTUB32868, INSSTUB32868H	0.4			ns
		PAR_IN after CK $\uparrow$, $\overline{CK}$ $\downarrow$ INSSTU32868, INSSTUA32868	0.5			ns
		PAR_IN after CK $\uparrow$, $\overline{CK}$ $\downarrow$ INSSTUB32868, INSSTUB32868H	0.4			ns

Notes:

1 Data inputs must be set to valid levels (not floating) within a time t_{act} max, at most, after a $\overline{RESET}$ rising transition.

2 Data, V_{REF}, and clock inputs must be held at valid levels (not floating) for a time t_{inact} max, at least, after a $\overline{RESET}$ falling transition.

3 See Figures 1 and 2.

4 See Figures 1 and 3.

5 See Figures 1 and 6.

AC Specifications

Parameter	Symbol	From Input	To Output	Min	Typ	Max	Unit
Maximum input clock frequency, for INSSTU32S868	f_{max}			270			MHz
Maximum input clock frequency, for INSSTUA32S868, INSSTUB32868, INSSTUB32868H				410			MHz
Propagation delay, single bit switching, for INSSTU32S868	t_{pdm}[1,3]	CK, $\overline{CK}$	$\overline{QCS0}$, $\overline{QCS1}$, QCKE0, QCKE1, QODT0, QODT1, Qn	1.41		2.15	ns
Propagation delay, single bit switching, for INSSTUA32S868				1.20		1.80	ns
Propagation delay, single bit switching, for INSSTUB32868, INSSTUB32868H				1.25		1.50	ns
Low-to-high propagation delay	t_{LH}[5]	CK, $\overline{CK}$	$\overline{QERR}$	1.2		3	ns
High-to-low propagation delay	t_{HL}[5]	CK, $\overline{CK}$	$\overline{QERR}$	1		2.4	ns
Propagation delay, simultaneous switching, for INSSTU32S868	T_{PDMSS}[1,2,3]	CK, $\overline{CK}$	$\overline{QCS0}$, $\overline{QCS1}$, QCKE0, QCKE1, QODT0, QODT1, Qn			2.35	ns
Propagation delay, simultaneous switching, for INSSTUA32S868						2.00	ns
Propagation delay, simultaneous switching, for INSSTUB32868, INSSTUB32868H						1.6	ns
High-to-low propagation delay	t_{PHL}[4]	$\overline{RESET}$ ↓	$\overline{QCS0}$↓, $\overline{QCS1}$↓, QCKE0 ↓, QCKE1 ↓, QODT0 ↓, QODT1 ↓, Qn ↓			3	ns
Low-to-high propagation delay	t_{PLH}[5]	$\overline{RESET}$ ↓	$\overline{QERR}$ ↑			3	ns

Notes:

1 Includes 350 ps test load transmission line delay.
2 This parameter is not necessarily production tested.
3 See Figures 1 and 5.
4 See Figures 1 and 7.
5 See Figures 10 through 13.

Output Edge Rate Specifications

Parameter	Symbol	Conditions	Min	Max	Unit
Rising edge slew rate[2]	dV/dt_r	V_{DD} = 1.8 V ± 0.1 V	1	4	V/ns
Falling edge slew rate[1]	dV/dt_f		1	4	V/ns
Absolute rising-falling edge slew rate difference	dV/dt_Δ			0.5	V/ns

Notes:

[1] See Figure 8.

[2] See Figure 9.

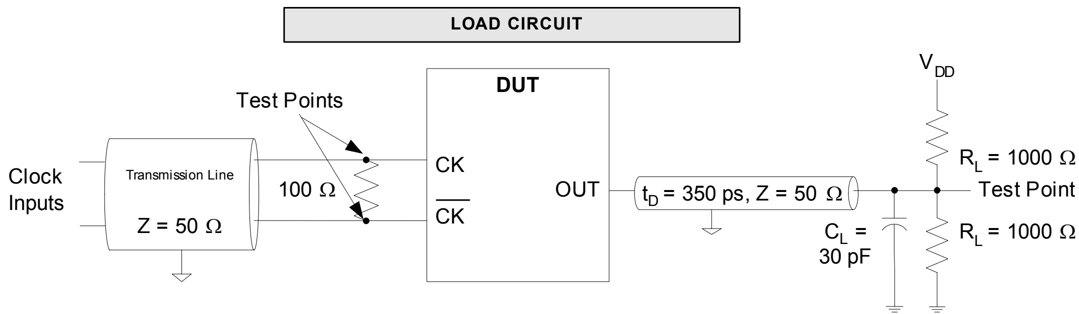
Load Circuit and Voltage Waveforms

General Measurement Notes:

All input pulses are supplied by generators having the following characteristics:

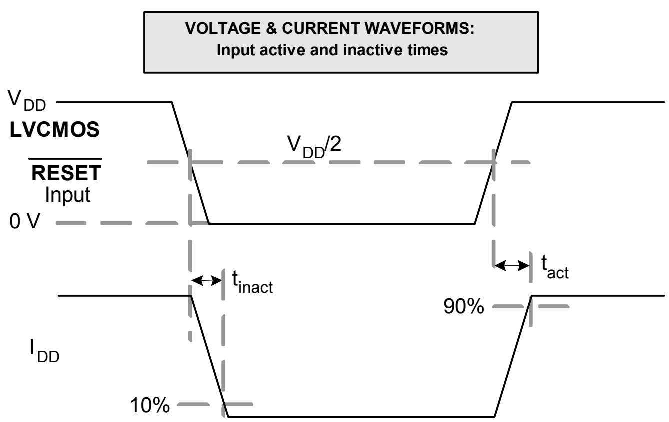
Pulse Repetition Rate ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).

The outputs are measured one at a time with one transition per measurement.



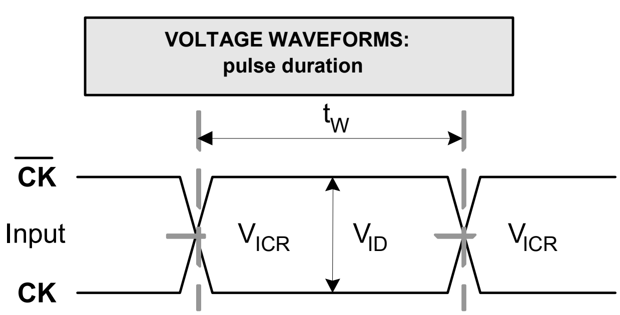
Note: CL includes probe and equipment capacitance.

Figure 1



Note: IDD tested with clock and data input held at VDD or GND, and I_O = 0mA.

Figure 2



Note: V_{ID} = 600 mV

Figure 3

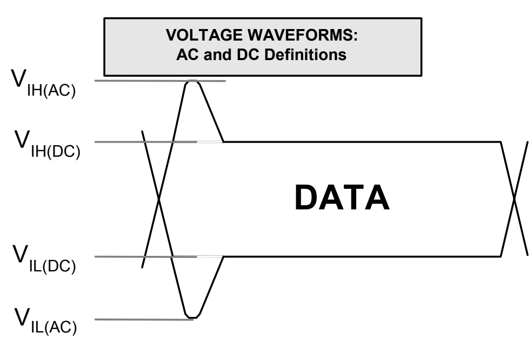
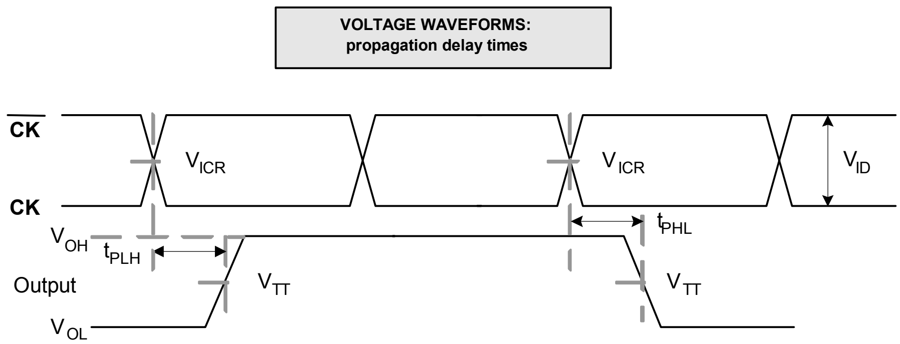
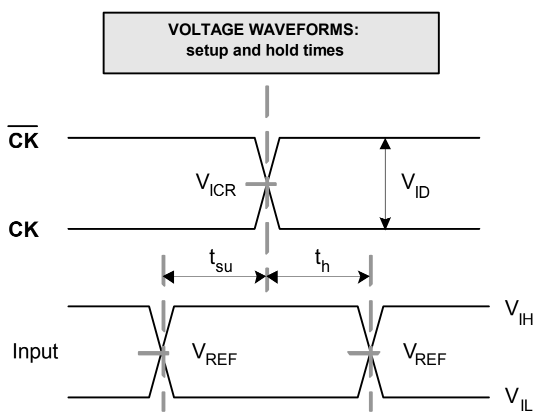


Figure 4



Note: t_{PLH} and t_{PHL} are the same as t_{pdm} , and V_{ID} = 600 mV

Figure 5



Note: $V_{REF} = V_{DD}/2$, $V_{IH} = V_{REF} + 250$ mV, $V_{IL} = V_{REF} – 250$ mV, V_{ID} = 600 mV

Figure 6

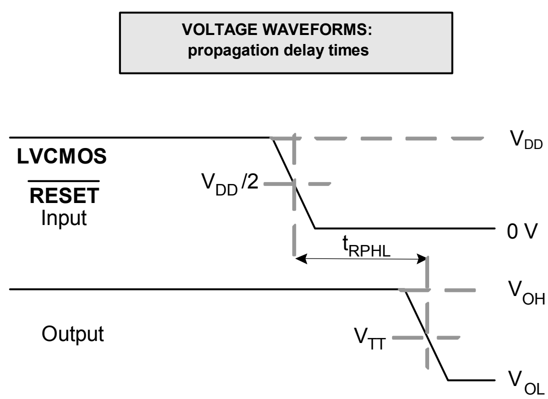


Figure 7

Output Slew Rate Measurement Information

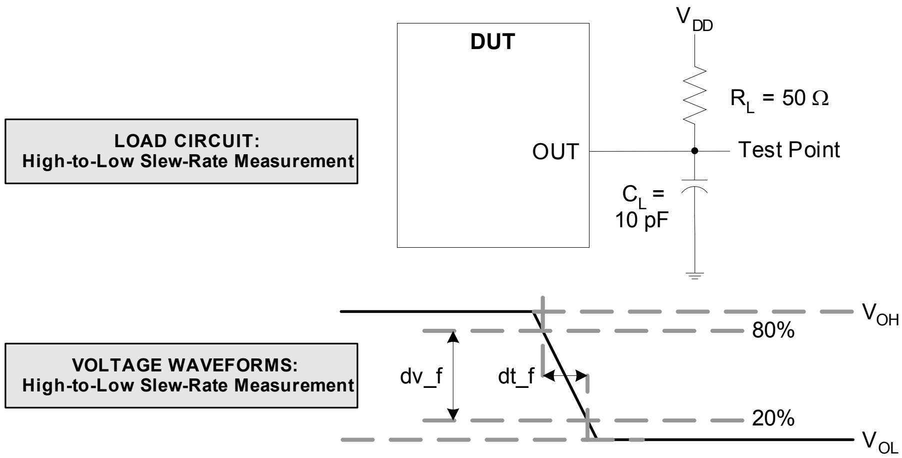


Figure 8

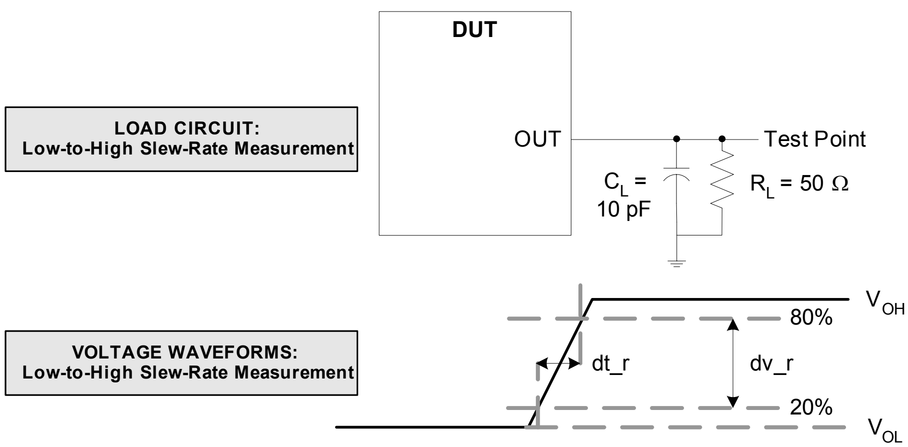


Figure 9

Parity Error Output Measurement Information

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Zo = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified. V_{DD} = 1.8 ± 0.1 V

LOAD CIRCUIT:
Parity Error Output Measurements

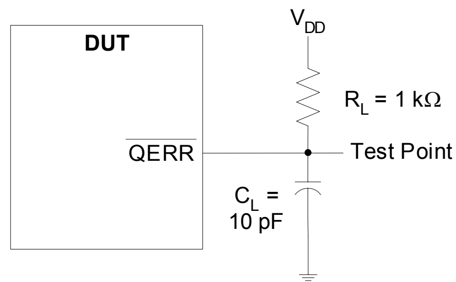


Figure 10

VOLTAGE WAVEFORMS:
open-drain output low-to-high transition time with respect to reset input

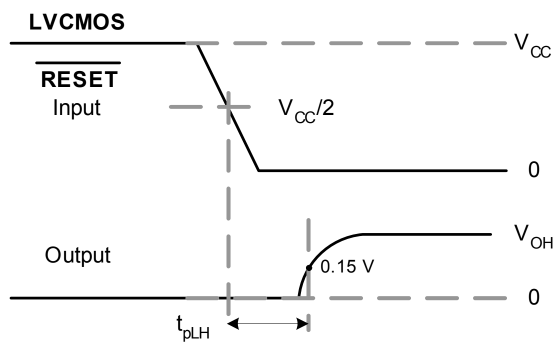


Figure 11

VOLTAGE WAVEFORMS:
open-drain output high-to-low transition time with respect to clock inputs

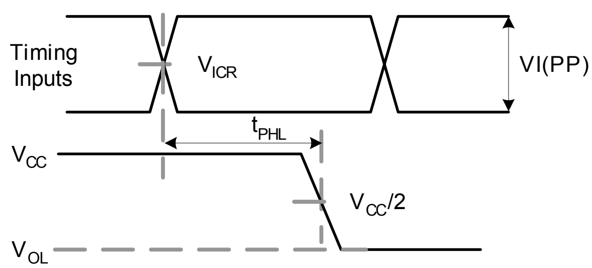


Figure 12

VOLTAGE WAVEFORMS:
open-drain output low-to-high transition time with respect to clock inputs

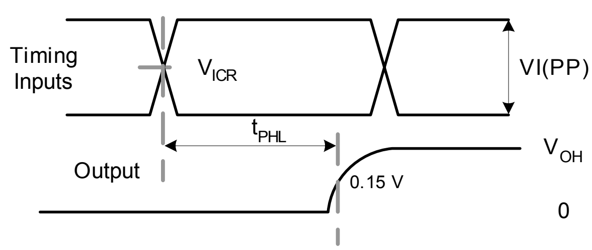


Figure 13

Register Timing with Parity Function

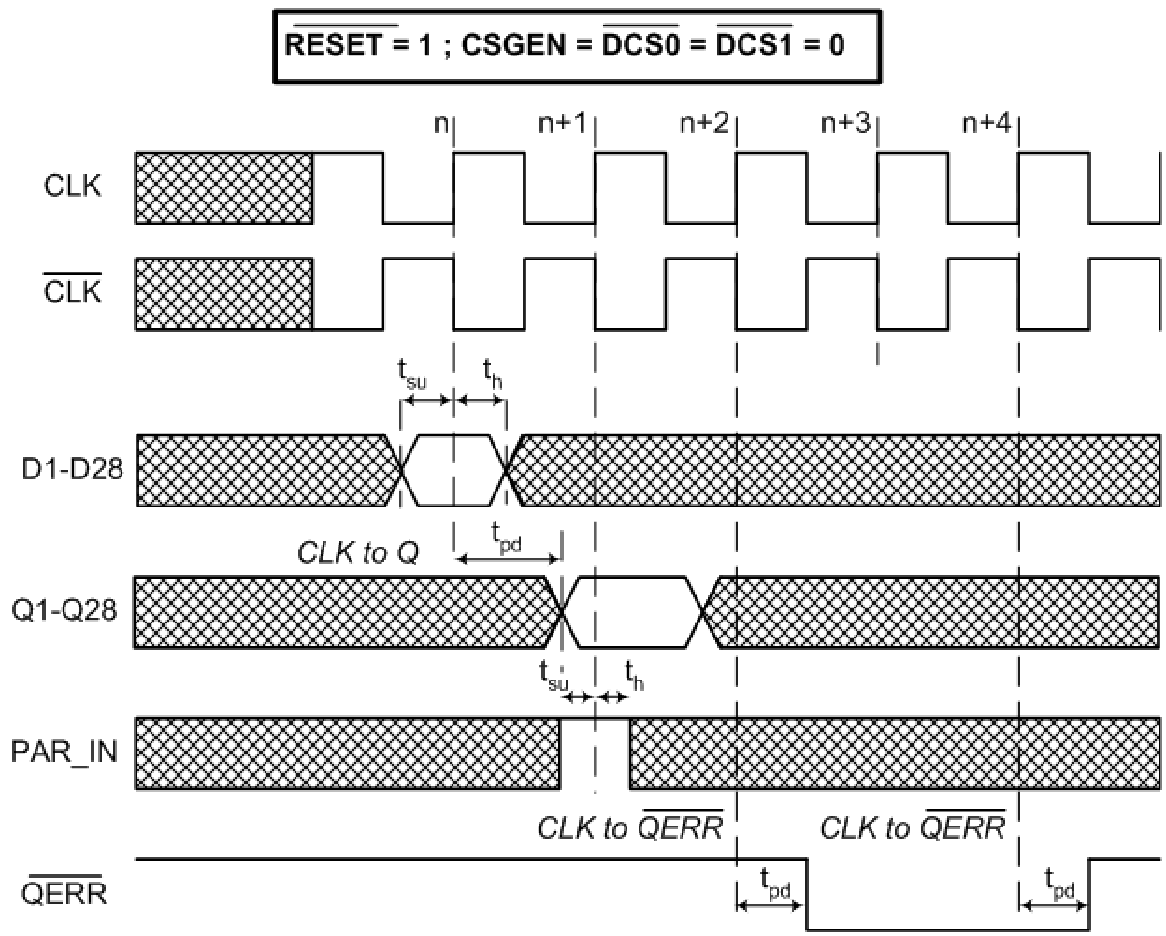
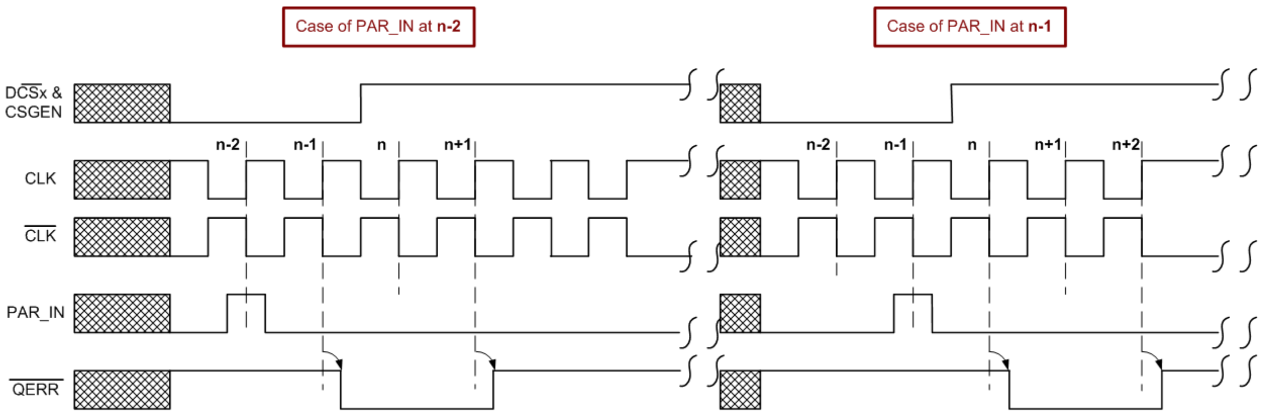
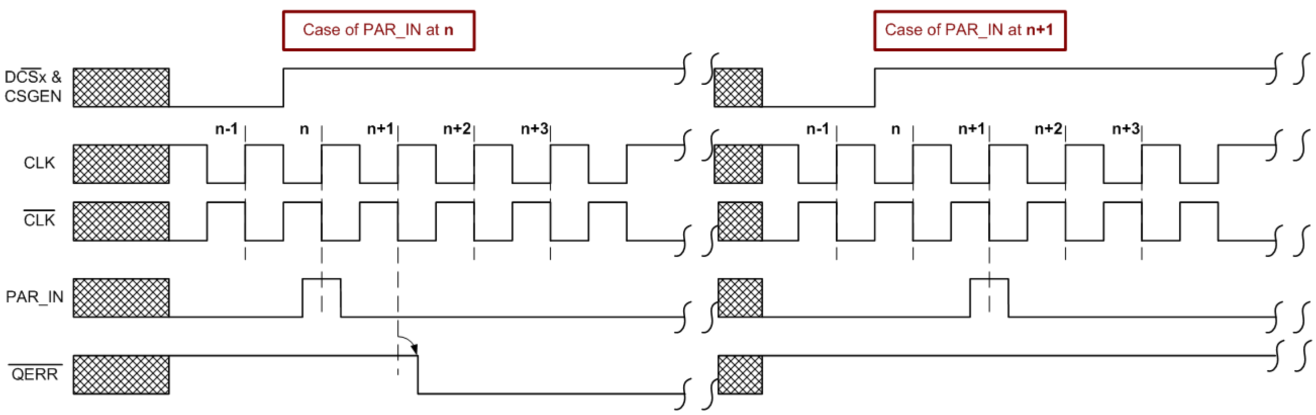
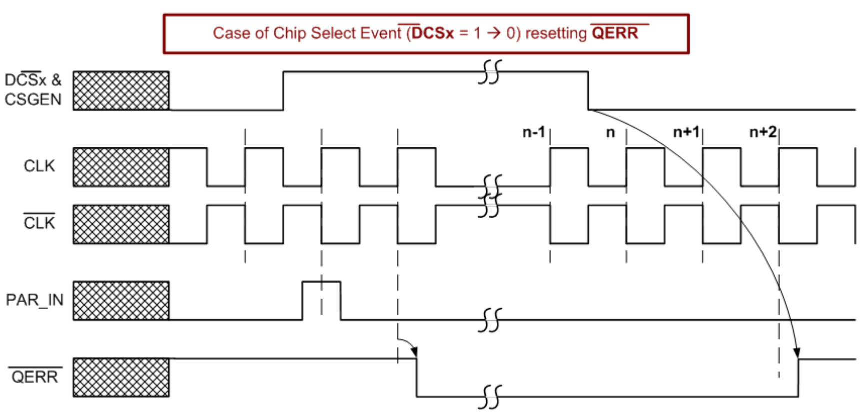


Figure 14

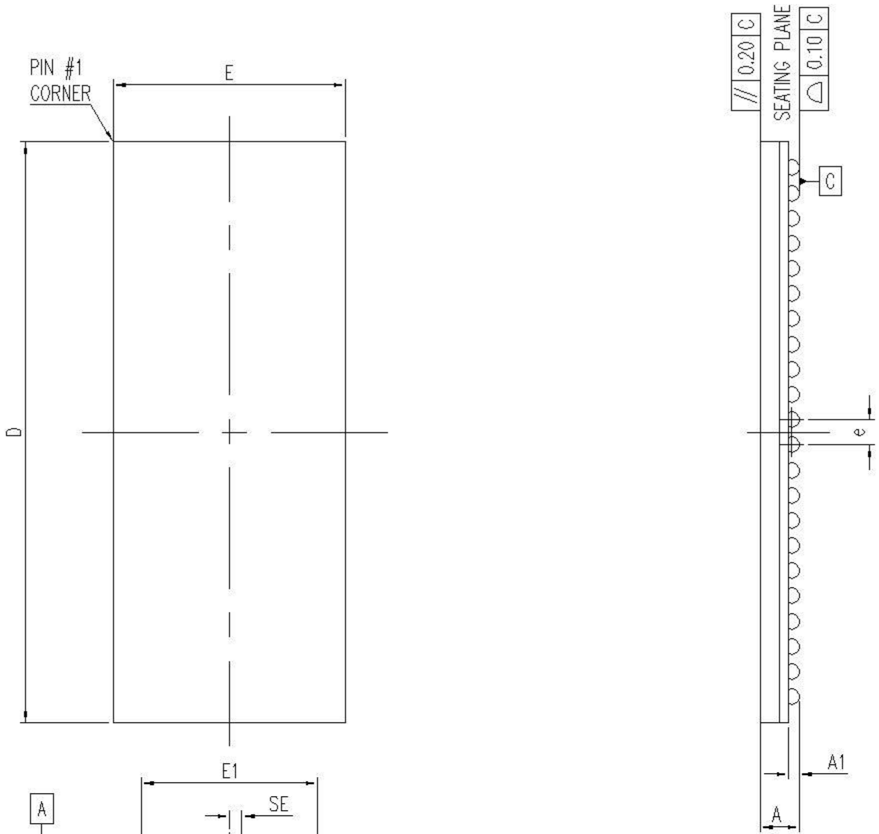
Parity Function Under Error Conditions: PAR_IN & Chip Select/Deselect Events

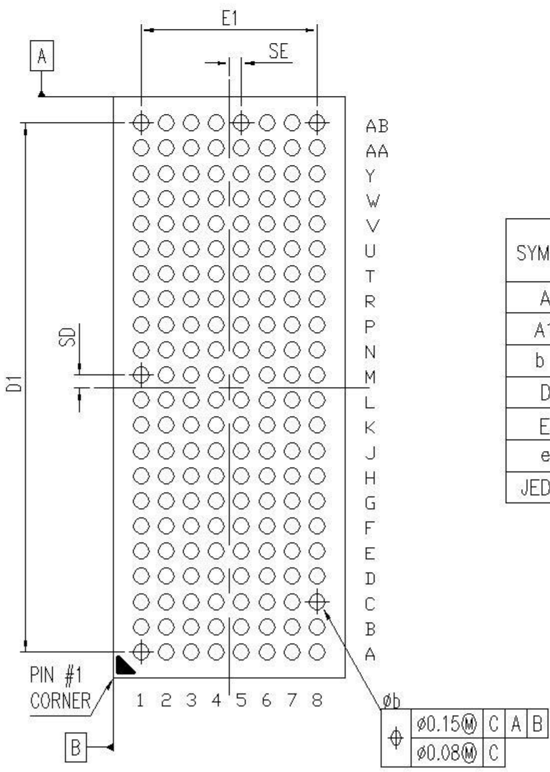






176-Ball TFBGA Package Outline Drawing





SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	–	–	1.10	–	–	0.043
A1	0.25	–	–	0.010	–	–
b	0.35	0.40	0.45	0.014	0.016	0.018
D	14.90	15.00	15.10	0.587	0.591	0.594
E	5.90	6.00	6.10	0.232	0.236	0.240
e	0.65 BSC.			0.026 BSC.		
JEDEC	MO-246					

N	SE (mm)	SD (mm)	E1 (mm)	D1 (mm)	JEDEC(Ref.)
176	0.325 BSC.	0.325 BSC.	4.55 BSC.	13.65 BSC.	MO-246B

176-Ball TFBGA Ball Out Information

176 Ball BGA for Register A (C=0)								
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
A	D2	D1	C	GND	V_{REF}	GND	Q1A	Q1B
B	D4	D3	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q2A	Q2B
C	D6 (DCKE1)	D5	GND	GND	GND	GND	Q3A	Q3B
D	D8 (DCKE0)	D7	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q4A	Q4B
E	D9	Q6A (QCKE1A)	GND	GND	GND	GND	Q5A	Q5B
F	D10	Q8A (QCKE0A)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q7A	Q6B (QCKE1B)
G	D11	Q10A	GND	GND	GND	GND	Q9A	Q7B
H	D12	Q12A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q11A	Q8B (QCKE0B)
J	$\overline{\text{DCS1}}$	$\overline{\text{QCS1A}}$	GND	GND	GND	GND	Q10B	Q9B
K	$\overline{\text{DCS0}}$	$\overline{\text{QCS0A}}$	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q12B	Q11B
L	CK	CSGEN	PAR_IN	GND	GND	GND	Q14B ($\overline{\text{QCS0B}}$)	Q13B ($\overline{\text{QCS1B}}$)
M	$\overline{\text{CK}}$	$\overline{\text{RESET}}$	$\overline{\text{QERR}}$	V_{DD}	V_{DD}	V_{DD}	Q15B (QODT0B)	Q16B (QODT1B)
N	D15 (DODT0)	Q15A (QODT0A)	GND	GND	GND	GND	Q17B	Q18B
P	D16 (DODT1)	Q16A (QODT1A)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q19B	Q20B
R	D17	Q17A	GND	GND	GND	GND	Q18A	Q21B
T	D18	Q19A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q20A	Q22B
U	D19	Q21A	GND	GND	GND	GND	Q22A	Q23B
V	D20	Q23A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q24A	Q24B
W	D21	D22	GND	GND	GND	GND	Q25A	Q25B
Y	D23	D24	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q26A	Q26B
AA	D25	D26	GND	GND	GND	GND	Q27A	Q27B
AB	D27	D28	NC	V_{DD}	V_{REF}	V_{DD}	Q28A	Q28B

176-Ball TFBGA Ball Out Information (cont'd)

176 Ball BGA for Register B (C=1)								
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
A	D2	D1	C	GND	V_{REF}	GND	Q1A	Q1B
B	D4	D3	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q2A	Q2B
C	D6	D5	GND	GND	GND	GND	Q3A	Q3B
D	D8	D7	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q4A	Q4B
E	D9	Q6A	GND	GND	GND	GND	Q5A	Q5B
F	D10	Q8A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q7A	Q6B
G	D11	Q10A	GND	GND	GND	GND	Q9A	Q7B
H	D12	Q12A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q11A	Q8B
J	D13 (DODT1)	Q13A (QODT1A)	GND	GND	GND	GND	Q10B	Q9B
K	D14 (DODT0)	Q14A (QODT0A)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q12B	Q11B
L	CK	CSGEN	PAR_IN	GND	GND	GND	Q14B (QODT0B)	Q13B (QODT1B)
M	$\overline{CK}$	$\overline{RESET}$	$\overline{QERR}$	V_{DD}	V_{DD}	V_{DD}	Q15B ($\overline{QCS0B}$)	Q16B ($\overline{QCS1B}$)
N	D15 ($\overline{DCS0}$)	Q15A ($\overline{QCS0A}$)	GND	GND	GND	GND	Q17B	Q18B
P	D16 ($\overline{DCS1}$)	Q16A ($\overline{QCS1A}$)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q19B	Q20B
R	D17	Q17A	GND	GND	GND	GND	Q18A	Q21B (QCKE0B)
T	D18	Q19A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q20A	Q22B
U	D19	Q21A (QCKE0A)	GND	GND	GND	GND	Q22A	Q23B (QCKE1B)
V	D20	Q23A (QCKE1A)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q24A	Q24B
W	D21 (DCKE0)	D22	GND	GND	GND	GND	Q25A	Q25B
Y	D23 (DCKE1)	D24	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q26A	Q26B
AA	D25	D26	GND	GND	GND	GND	Q27A	Q27B
AB	D27	D28	NC	V_{DD}	V_{REF}	V_{DD}	Q28A	Q28B

Solder Reflow Profile

These products will meet the specifications in this data sheet when manufactured in accordance with JESD22-A113D. JESD22-A113D defines the solder profile for both leaded and lead-free package versions. The green version of this product must be manufactured using the lead-free solder reflow profile.

Patent Notification

These products include technology that is covered by one or more Inphi patents or patent applications including issued US Patent Nos. 6,980,021 and 6,859,075.

Ordering Information

Part No.	Description
INSSTUA32S868-GS05	DDR2-400, 533, 667, Configurable Registered Buffer with Parity, Module K, L, P in green (G) package
INSSTUB32868-GS02	DDR2-400, 533, 667, 800 Configurable Registered Buffer with Parity, Module K, L, P in green (G) package
INSSTUB32868H-GS01	DDR2-400, 533, 667, 800 Configurable Registered Buffer with Parity, Module M in green (G) package
All versions of the '868 register are available in a "Green" package type: G = Green (lead and halogen-free) 176 Ball TFBGA	
For each customer application, customer's technical experts must validate all parameters. Inphi Corporation reserves the right to change product specifications contained herein without prior notice. No liability is assumed as a result of the use or application of this product. No circuit patent licenses are implied. Contact Inphi Corporation's marketing department for the latest information regarding this product.	

Contact Information

Inphi Corporation
2393 Townsgate Road, Suite 101
Westlake Village, CA 91361

- Phone: (805) 446-5100
- Fax: (805) 446-5189
- E-mail: products@inphi-corp.com

Visit us on the Internet at: http://www.inphi-corp.com

Qualification Notification

The INSSTU32S868 has passed all qualification tests required by JESD47.

Inphi Corporation will honor the full warranty as outlined in Section 5 of Inphi's Standard Customer Purchase Order Terms and Conditions.

Version Updates

From Version 1.6 to 1.7 (dated 2006-06-29):

1. Updated footer to correct data and revision.
2. Changes to Ordering Information section (page 20):
    a. Both the normal/standard (leaded) and the lead-free package types were deleted.
    b. The proper dash number is added to each part version.

From Version 1.7 to 2.0 (dated 2006-10-24):

1. Change to the title (page 1): INSSTUB32868H is added.
2. Changes to the Features section (page 1):
    a. INSSTUB32868H is added.
    b. RDIMM modules L & P supported.
    c. References to Leaded and Lead-Free package versions deleted.
3. Changes to the Part Number Selection Table section (page 3):
    a. INSSTUB32868H is added.
    b. RDIMM module P supported.
4. Change to the Timing Requirements table (page 12): Added INSSTUB32868H reference to the appropriate parameters.
5. Change to the AC Specifications table (page 13): Added INSSTUB32868H reference to the appropriate parameters.
6. Change to Ordering Information section (page 24):
    a. INSSTUA32S868-GS04 changed to INSSTUA32S868-GS05.
    b. INSSTUB32868-GS01 changed to INSSTUB32868-GS02.
    c. INSSTUB32868H-GS01 is added.
7. Extended Parity Function was added to support AMD parity operation.

From Version 2.0 to 2.1 (dated 2007-05-09):

1. Change to DC Specifications section (page 11):
    a. Changed Input Capacitance data inputs (symbol = C_i), Min specification from 2.5 pF to 2.0 pF.

From Version 2.1 to 2.2 (dated 2007-07-18):

1. Updated DC Specifications (page 11):
    a. Added "$\overline{\text{DCS}}$" to Input Capacitance, data inputs parameter
    b. Updated Input capacitance, CK and $\overline{\text{CK}}$ parameter:
        i. Changed 2nd half of conditions from "V_I = 600 mVp-p" to "V_{ID} = 600 mV"
    c. Updated Input capacitance, $\overline{\text{RESET}}$ parameter in DC Specifications (page 11):
        i. Min from 1.6 pF to 2 pF
        ii. Max from 2 pF to 3.5 pF
2. Updated 176-Ball TFBGA Package Outline Drawing dimensions table (page 21):
    a. For symbol "A": Removed minimum and nominal dimensions (in mm and inches).
    b. For symbol "A1": Removed nominal and maximum dimensions (in mm and inches).
    c. Removed symbol "A2" and its dimensions.

Inphi Corporation is an ISO-9001:2000 Certified Manufacturer