SHM-LM-2
Low Cost Monolithic Sample-Hold

FEATURES

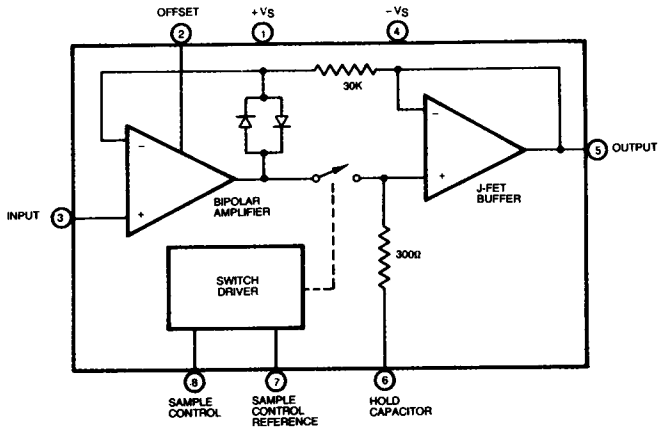
- **5 Microseconds acquisition time**
- **0.01% Gain accuracy**
- **TTL/CMOS-compatible**
- **±5V to ±18V supplies**
- **TO-99 package**
- **Low cost**

GENERAL DESCRIPTION

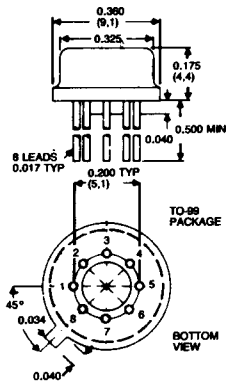
The SHM-LM-2 is a low cost monolithic sample-hold circuit with excellent performance features. It is self-contained requiring only an external hold capacitor with the value selected by the user for desired speed and accuracy characteristics. Acquisition time is 6 microseconds for a 10V change to 0.01% using a 1000 pF capacitor and 25 microseconds using a 0.01 μF capacitor. It is 5 microseconds and 20 microseconds respectively for a 10V change to 0.l%. This device is internally configured as a unity gain follower with a gain error of less than 0.01% in the sample mode.

The circuit consists of a bipolar input amplifier, a low leakage electronic switch, and an FET output amplifier. The monolithic fabrication process combines P channel junction FET's with bipolar transistors to achieve a low noise, high input impedance output amplifier. Other important specifications include 10^{10} ohms input impedance and 1 MHz bandwidth. Aperture time is less than 100 nanoseconds and hold mode feedthrough is less than 0.005%. Hold mode droop is 200 μV/mseconds maximum with a 1000 pF hold capacitor and 20 μV/mseconds maximum with a 0.01 μF capacitor. The SHM-LM-2 can operate over a power supply range of ±5V to ±18V.

Applications include sampling for A/D conversion, deglitching circuits, automatic zeroing circuits, and analog demultiplexing circuits. It is recommended that the holding capacitor (C_H) be a teflon, polystyrene, or polypropylene type for best results. Operating temperature range is 0°C to +70°C for SHM-LM-2 and −55°C to +125°C for SHM-LM-2M.



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: ALL LEADS GOLD PLATED KOVAR

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	+POWER SUPPLY
2	OFFSET ADJUST
3	INPUT
4	−POWER INPUT
5	OUTPUT
6	HOLD CAPACITOR (C_H)
7	SAMPLE CONTROL REF.
8	SAMPLE CONTROL

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage, pins 1 and 4	±18V
Input Voltage, pin 3	±Supply
Sample Control to Sample Reference, pin 8 to pin 7	+7, −30V
Hold Capacitor Short Circuit	10 seconds

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V supplies and C_H = 0.01 µF unless otherwise stated.

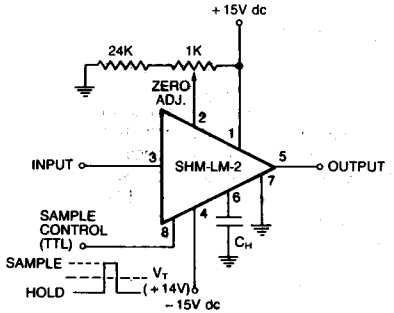
INPUTS	
Input Voltage Range	±11.5V minimum
Input Overvoltage, no damage	±Supply
Input Impedance	10^{10} ohms
Input Bias Current	10 nA typical, 50 nA maximum
Sample Control	TTL or CMOS
Sample Control Input Current[1]	10 µA maximum
OUTPUT	
Output Voltage Range	±11.5V minimum
Output Current, S.C. protected	±5 mA
Output Impedance	0.5 ohm
PERFORMANCE	
Gain	+1.000, +0, −0.01%
Output Offset Voltage, adj. to zero	±7 mV maximum
Offset Voltage Drift, SHM-LM-2	20 µV/°C
Offset Voltage Drift, SHM-LM-2M	10 µV/°C[2]
Sample to Hold Offset	2.5 mV maximum
Hold Mode Feedthrough	0.01% maximum
Power Supply Rejection Ratio	80 dB minimum
Output Noise, hold mode (10 Hz-100 kHz)	8.5 µV RMS
Hold Mode Droop, C_H = 1000 pF	200 µV/mseconds maximum
C_H = 0.01 µF	20 µV/mseconds maximum
DYNAMIC RESPONSE	
Acquisition Time	
10V Change, C_H = 1000 pF	5 microseconds to 0.1%
10V Change, C_H = 1000 pF	6 microseconds to 0.01%
20V Change, C_H = 1000 pF	7 microseconds to 0.1%
20V Change, C_H = 1000 pF	8 microseconds to 0.01%
10V Change, C_H = 0.01 µF	20 microseconds to 0.1%
10V Change, C_H = 0.01 µF	25 microseconds to 0.01%
Aperture Delay Time	100 nanoseconds
Hold Mode Settling Time[3]	800 nanoseconds
Bandwidth, Sample Mode, −3 dB	1 MHz
POWER REQUIREMENTS	
Voltage, rated performance	±15V dc
Voltage Range, operating	±5V to ±18V dc
Quiescent Current	6 mA
PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range, SHM-LM-2	0°C to +70°C
SHM-LM-2M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Case	8 pin TO-99

FOOTNOTES:
1. For either Sample Control or Sample Control Reference inputs
2. 28 µV/°C maximum
3. The time for the output to settle within 1 mV of final value after the logic command to switch into hold mode.

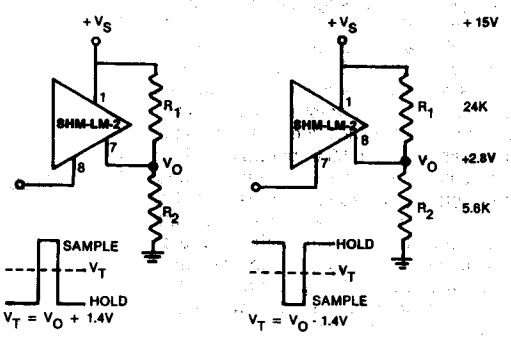
TECHNICAL NOTES

1. The sample to hold offset can be adversely affected by stray capacitive coupling from input sample control signals to the hold capacitor. It is recommended that a guard ring connected to the output be put around pin 6 in a circuit board layout in order to minimize this effect.
2. For various types of logic inputs, the logic threshold (V_T) is set by two biasing resistors as shown in the diagram. Inverted or non-inverted pulses may be used by using either pin 7 or pin 8 as the sample control input.

CONNECTION DIAGRAM



SAMPLE-CONTROL CONNECTIONS



FOR TTL CONNECT PIN 7 TO GROUND

FOR TTL USE VALUES SHOWN AT RIGHT

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
SHM-LM-2	0°C to 70°C
SHM-LM-2M	−55°C to +125°C

ACCESSORIES

Part Number	Description
TP1K	Trimming Potentiometer