

Am2901 • Am2901A • Am2901B

Four-Bit Bipolar Microprocessor Slice

DISTINCTIVE CHARACTERISTICS

- Two-address architecture – Independent simultaneous access to two working registers saves machine cycles.
- Eight-function ALU – Performs addition, two subtraction operations, and five logic functions on two source operands.
- Flexible data source selection – ALU data is selected from five source ports for a total of 203 source operand pairs for every ALU function.
- Left/right shift independent of ALU – Add and shift operations take only one cycle.
- Four status flags – Carry, overflow, zero, and negative.
- Expandable – Connect any number of Am2901's together for longer word lengths.
- Microprogrammable – Three groups of three bits each for source operand, ALU function, and destination control.
- Fast – Am2901B is up to 27% faster than Am2901A, up to 50% faster than Am2901. The Am2901B meets or exceeds all of the specifications for the Am2901 and Am2901A.

GENERAL DESCRIPTION

The four-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPU's, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the Am2901 will allow efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip.

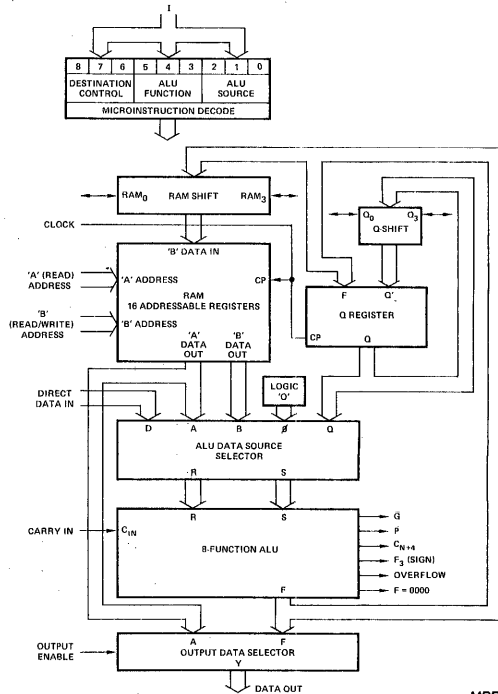
The Am2901B is a plug-in replacement for the Am2901 or Am2901A, but is 25% faster than the Am2901A and 50% faster than the Am2901.

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For applications information see the last part of this data sheet and chapters III and IV of "Build a Microcomputer", AMD's application note series on the Am2900 Family.

MICROPROCESSOR SLICE BLOCK DIAGRAM



MPR-004

ARCHITECTURE

A detailed block diagram of the bipolar microprogrammable microprocessor structure is shown in Figure 1. The circuit is a four-bit slice cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the Figure 1 block diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 16 words of the RAM as defined by the B address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 1, the ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent that AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant source operand pairs for the ALU. The Am2901 microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I₀, I₁, and I₂ inputs. The definition of I₀, I₁, and I₂ for the eight source operand combinations are as shown in Figure 2. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I₃, I₄, and I₅ microinstruction inputs are used to select the

ALU function. The definition of these inputs is shown in Figure 3. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, \bar{G} , and carry propagate, \bar{P} , are outputs of the device for use with a carry-look-ahead-generator such as the Am2902. A carry-out, C_{n+4}, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active HIGH.

The ALU has three other status-oriented outputs. These are F₃, F = 0, and overflow (OVR). The F₃ output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F₃ is non-inverted with respect to the sign bit output Y₃. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is HIGH when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I₆, I₇, and I₈ microinstruction inputs. These combinations are shown in Figure 4.

The four-bit data output field (Y) features three-state outputs and can be directly bus organized. An output control (\bar{OE}) is used to enable the three-state outputs. When \bar{OE} is HIGH, the Y outputs are in the high-impedance state.

A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I₆, I₇, and I₈ microinstruction inputs. Refer to Figure 4 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a three-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position (X2) or shifted down one position ($\div 2$). The shifter has two ports; one is labeled RAM₀ and the other is labeled RAM₃. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the FAM₃ buffer is enabled and the RAM₀ multiplexer input is enabled. Likewise, in the shift down mode, the RAM₀ buffer and RAM₃ input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I₆, I₇ and I₈ microinstruction inputs as defined in Figure 4.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports; one is labeled Q₀ and the other is Q₃. The operation of these two ports is similar to the RAM shifter and is also controlled from I₆, I₇, and I₈ as shown in Figure 4.

The clock input to the Am2901 controls the RAM, the Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B address field when the clock input is LOW.

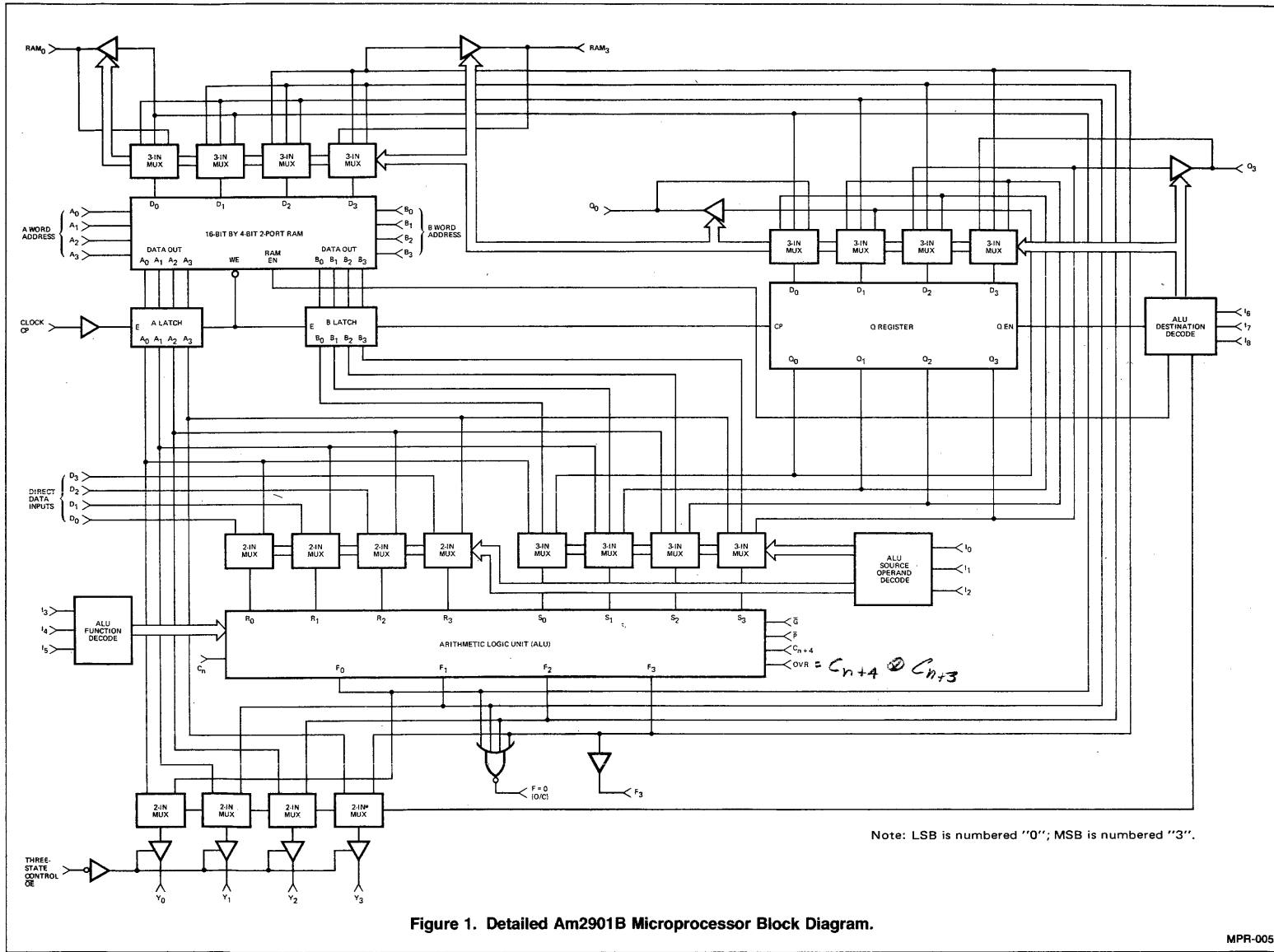


Figure 1. Detailed Am2901B Microprocessor Block Diagram.

MPR-005

Mnemonic	MICRO CODE				ALU SOURCE OPERANDS	
	I ₂	I ₁	I ₀	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

Figure 2. ALU Source Operand Control.

Mnemonic	MICRO CODE				ALU Function	SYMBOL
	I ₅	I ₄	I ₃	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S - R
SUBS	L	H	L	2	R Minus S	R - S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	\bar{R} AND S	$\bar{R} \wedge S$
EXOR	H	H	L	6	R EX OR S	R ⊕ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \oplus S}$

Figure 3. ALU Function Control.

Mnemonic	MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
	I ₈	I ₇	I ₆	Octal Code	Shift	Load	Shift	Load		RAM ₀	RAM ₃	Q ₀	Q ₃
OREG	L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F ₀	IN ₃	Q ₀	IN ₃
RAMD	H	L	H	5	DOWN	F/2 → B	X	NONE	F	F ₀	IN ₃	Q ₀	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN ₀	F ₃	IN ₀	Q ₃
RAMU	H	H	H	7	UP	2F → B	X	NONE	F	IN ₀	F ₃	X	Q ₃

□ DON'T USE
 ◻ DISABLE FEN
 △ ENABLE FEN
 X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state
 B = Register Addressed by B inputs.
 UP is toward MSB, DOWN is toward LSB.

Figure 4. ALU Destination Control.

OCTAL	ALU Source / ALU Function	0	1	2	3	4	5	6	7
		ALU Source	A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q
0	C _n = L R Plus S C _n = H	A+Q	A+B	Q	B	A	D+A	D+Q	D
1	C _n = L S Minus R C _n = H	Q-A-1	B-A-1	Q-1	B-1	A-1	A-D-1	Q-D-1	-D-1
2	C _n = L R Minus S C _n = H	A-Q-1	A-B-1	-Q-1	-B-1	-A-1	D-A-1	D-Q-1	D-1
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	\bar{R} AND S	$\bar{A} \wedge Q$	$\bar{A} \wedge B$	Q	B	A	$\bar{D} \wedge A$	$\bar{D} \wedge Q$	0
6	R EX-OR S	A ⊕ Q	A ⊕ B	Q	B	A	D ⊕ A	D ⊕ Q	D
7	R EX-NORS	$\overline{A \oplus Q}$	$\overline{A \oplus B}$	\bar{Q}	\bar{B}	\bar{A}	$\overline{D \oplus A}$	$\overline{D \oplus Q}$	\bar{D}

+ = Plus; - = Minus; ∨ = OR; ∧ = AND; ⊕ = EX-OR

Figure 5. Source Operand and ALU Function Matrix.

SOURCE OPERANDS AND ALU FUNCTIONS

There are eight source operand pairs available to the ALU as selected by the I₀, I₁, and I₂ instruction inputs. The ALU can perform eight functions; five logic and three arithmetic. The I₃, I₄, and I₅ instruction inputs control this function selection. The carry input, C_n, also affects the ALU results when in the arithmetic mode. The C_n input has no effect in the logic mode. When I₀ through I₅ and C_n are viewed together, the matrix of

Figure 5 results. This matrix fully defines the ALU/source operand function for each state.

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode, the carry will affect the function performed while in the logic mode, the carry will have no bearing on the ALU output. Figure 6 defines the various logic operations that the Am2901 can perform and Figure 7 shows the arithmetic functions of the device. Both carry-in LOW (C_n = 0) and carry-in HIGH (C_n = 1) are defined in these operations.

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Octal I543, I210	Group	Function
40 41 45 46	AND	A∧Q A∧B D∧A D∧Q
50 51 55 56	OR	A∨Q A∨B D∨A D∨Q
60 61 65 66	EX-OR	A⊕Q A⊕B D⊕A D⊕Q
70 71 75 76	EX-NOR	$\overline{A\oplus Q}$ $\overline{A\oplus B}$ $\overline{D\oplus A}$ $\overline{D\oplus Q}$
72 73 74 77	INVERT	\overline{Q} \overline{B} \overline{A} \overline{D}
62 63 64 67	PASS	Q B A D
32 33 34 37	PASS	Q B A D
42 43 44 47	"ZERO"	0 0 0 0
50 51 55 56	MASK	$\overline{A}\wedge Q$ $\overline{A}\wedge B$ $\overline{D}\wedge A$ $\overline{D}\wedge Q$

Figure 6. ALU Logic Mode Functions.

Octal I543, I210	C _n = 0 (Low)		C _n = 1 (High)	
	Group	Function	Group	Function
00 01 05 06	ADD	A+Q	ADD plus one	A+Q+1
		A+B		A+B+1
		D+A		D+A+1
		D+Q		D+Q+1
02 03 04 07	PASS	Q	Increment	Q+1
		B		B+1
		A		A+1
		D		D+1
12 13 14 27	Decrement	Q-1	PASS	Q
		B-1		B
		A-1		A
		D-1		D
22 23 24 17	1's Comp. INV.	$\overline{Q-1}$	2's Comp. (Negate)	\overline{Q}
		$\overline{B-1}$		\overline{B}
		$\overline{A-1}$		\overline{A}
		$\overline{D-1}$		\overline{D}
10 11 15 16 20 21 25 26	Subtract (1's Comp)	Q-A-1	Subtract (2's Comp)	Q-A
		B-A-1		B-A
		A-D-1		A-D
		Q-D-1		Q-D
		A-Q-1		A-Q
		A-B-1		A-B
		D-A-1		D-A
		D-Q-1		D-Q

Figure 7. ALU Arithmetic Mode Functions.

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LOGIC FUNCTIONS FOR G, P, C_{n+4}, AND OVR

The four signals G, P, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the Am2901 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Figure 2.

Definitions (+ = OR)

$$\begin{aligned}
 P_0 &= R_0 + S_0 & G_0 &= R_0 S_0 \\
 P_1 &= R_1 + S_1 & G_1 &= R_1 S_1 \\
 P_2 &= R_2 + S_2 & G_2 &= R_2 S_2 \\
 P_3 &= R_3 + S_3 & G_3 &= R_3 S_3 \\
 C_4 &= G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_n \\
 C_3 &= G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n
 \end{aligned}$$

I ₅₄₃	Function	\bar{P}	\bar{G}	C _{n+4}	OVR
0	R + S	$\overline{P_3 P_2 P_1 P_0}$	$\overline{G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0}$	C ₄	C ₃ ∨ C ₄
1	S - R	← Same as R + S equations, but substitute \bar{R}_i for R _i in definitions →			
2	R - S	← Same as R + S equations, but substitute \bar{S}_i for S _i in definitions →			
3	R ∨ S	LOW	$P_3 P_2 P_1 P_0$	$\overline{P_3 P_2 P_1 P_0} + C_n$	$\overline{P_3 P_2 P_1 P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\bar{R} \wedge S$	LOW	← Same as R ∧ S equations, but substitute \bar{R}_i for R _i in definitions →		
6	R ∨ \bar{S}	← Same as $\overline{R \wedge S}$, but substitute \bar{R}_i for R _i in definitions →			
7	$\overline{R \wedge S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 P_0$	$\frac{G_3 + P_3 G_2 + P_3 P_2 G_1}{+ P_3 P_2 P_1 P_0 (G_0 + C_n)}$	See note

Note: $[\bar{P}_2 + \bar{G}_2 \bar{P}_1 + \bar{G}_2 \bar{G}_1 \bar{P}_0 + \bar{G}_2 \bar{G}_1 \bar{G}_0 C_n] \vee [\bar{P}_3 + \bar{G}_3 \bar{P}_2 + \bar{G}_3 \bar{G}_2 \bar{P}_1 + \bar{G}_3 \bar{G}_2 \bar{G}_1 \bar{P}_0 + \bar{G}_3 \bar{G}_2 \bar{G}_1 \bar{G}_0 C_n]$ + = OR

Figure 8.

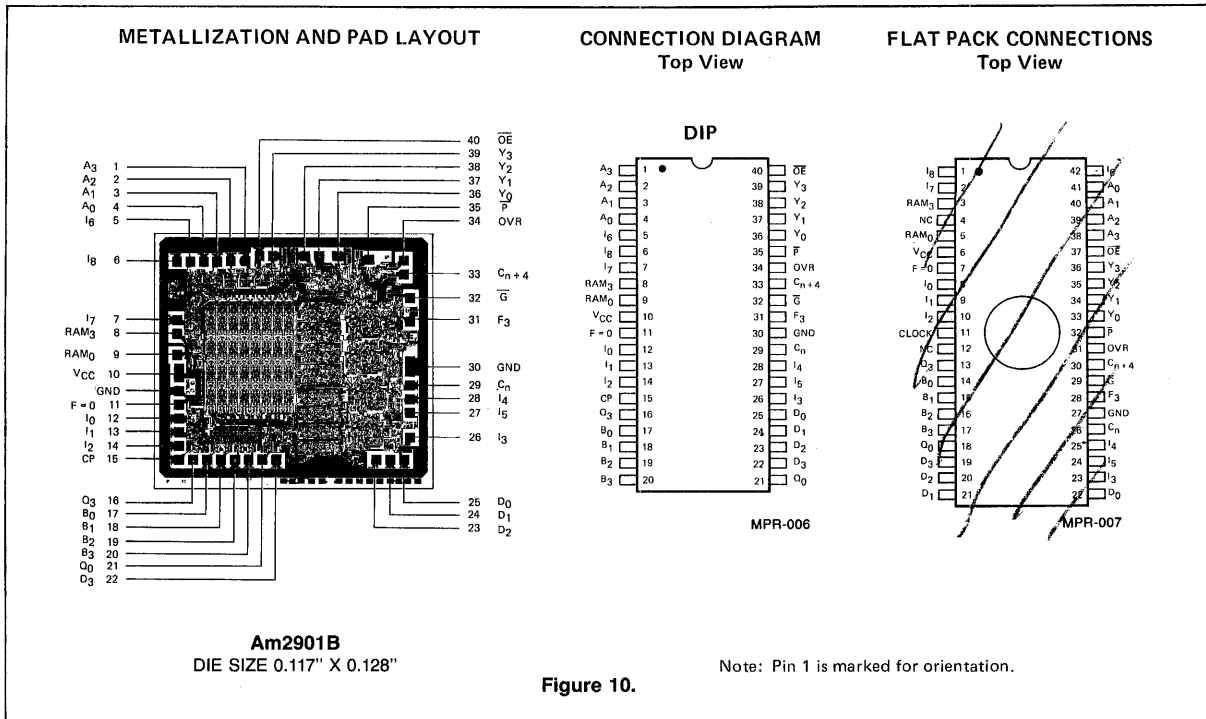
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2901 Order Number	Am2901A Order Number	Am2901B Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2901PC	AM2901APC	AM2901BPC	P-40	C	C-1
AM2901DC	AM2901ADC	AM2901BDC	D-40	C	C-1
AM2901DC-B	AM2901ADC-B	AM2901BDC-B	D-40	C	B-2 (Note 4)
	AM2901ADM	AM2901BDM	D-40	M	C-3
	AM2901ADM-B	AM2901BDM-B	D-40	M	B-3
	AM2901AFM	AM2901BFM	F-42	M	C-3
	AM2901AFM-B	AM2901BFM-B	F-42	M	B-3
	AM2901AXC	AM2901BXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
	AM2901AXM	AM2901BXM	Dice	M	

- Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
 2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = -55°C to +125°C, V_{CC} = 4.50V to 5.50V.
 3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
 4. 96 hour burn-in.

Figure 9.



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PIN DEFINITIONS

- A₀₋₃** The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.
- B₀₋₃** The four address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.
- I₀₋₈** The nine instruction control lines. Used to determine what data sources will be applied to the ALU (I₀₁₂), what function the ALU will perform (I₃₄₅), and what data is to be deposited in the Q-register or the register stack (I₆₇₈).
- Q₃** A shift line at the MSB of the Q register (Q₃) and the register stack (RAM₃). Electrically these lines are three-state outputs connected to TTL inputs internal to the device. When the destination code on I₆₇₈ indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q₃ pin and the MSB of the ALU output is available on the RAM₃ pin. Otherwise, the three-state outputs are OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).
- Q₀** Shift lines like Q₃ and RAM₃, but at the LSB of the Q-register and RAM. These pins are tied to the Q₃ and RAM₃ pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.
- RAM₀**
- D₀₋₃** Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the device. D₀ is the LSB.
- Y₀₋₃** The four data outputs. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I₆₇₈.
- \overline{OE}** Output Enable. When \overline{OE} is HIGH, the Y outputs are OFF; when \overline{OE} is LOW, the Y outputs are active (HIGH or LOW).
- \overline{G} , \overline{P}** The carry generate and propagate outputs of the internal ALU. These signals are used with the Am2902 for carry-lookahead.
- OVR** Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.
- F = 0** This is an open collector output which goes HIGH (OFF) if the data on the four ALU outputs F₀₋₃ are all LOW. In positive logic, it indicates the result of an ALU operation is zero.
- F₃** The most significant ALU output bit.
- C_n** The carry-in to the internal ALU.
- C_{n+4}** The carry-out of the internal ALU.
- CP** The clock input. The Q register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which comprises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5 V to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	-0.5 V to +V _{CC} max.
DC Input Voltage	-0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	-30 mA to +5.0 mA

OPERATING RANGE

Part Number Suffix	V _{CC}	Temperature
PC, PCB, DC, DCB XC	4.75V to 5.25V	T _A = 0°C to +70°C
DM, DMB FM, FMB XM	4.50V to 5.50V	T _C = -55°C to +125°C

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using V_{IL} ≤ 0.4V and V_{IH} ≥ 2.4V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)
(Group A, Subgroups 1, 2, and 3)

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = MIN. V _{IN} = V _{IH} or V _{IL}	Y ₀ , Y ₁ , Y ₂ , Y ₃	2.4			Volts
			I _{OH} = -1.0mA, C _{n+4}	2.4			
			I _{OH} = -800μA, OVR, P̄	2.4			
			I _{OH} = -600μA, F ₃	2.4			
			I _{OH} = -600μA RAM _{0, 3} , Q _{0, 3}	2.4			
I _{OH} = -1.6mA, Ḡ	2.4						
I _{CEX}	Output Leakage Current for F = 0 Output	V _{CC} = MIN., V _{OH} = 5.5V V _{IN} = V _{IH} or V _{IL}				250	μA
V _{OL}	Output LOW Voltage	V _{CC} = MIN., V _{IN} = V _{IH} or V _{IL}	Y ₀ , Y ₁ , Y ₂ , Y ₃	I _{OL} = 20mA (COM'L)		0.5	Volts
			Ḡ, F = 0	I _{OL} = 16mA (MIL)		0.5	
			C _{n+4}	I _{OL} = 16mA		0.5	
			OVR, P̄	I _{OL} = 10mA		0.5	
			F ₃ , RAM _{0, 3} , Q _{0, 3}	I _{OL} = 8.0mA		0.5	
I _{OL} = 6.0mA			0.5				
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 7)		2.0			Volts
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 7)				0.8	Volts
V _I	Input Clamp Voltage	V _{CC} = MIN., I _{IN} = -18mA				-1.5	Volts
I _{IL}	Input LOW Current	V _{CC} = MAX., V _{IN} = 0.5V	Clock, OE			-0.36	mA
			A ₀ , A ₁ , A ₂ , A ₃			-0.36	
			B ₀ , B ₁ , B ₂ , B ₃			-0.36	
			D ₀ , D ₁ , D ₂ , D ₃			-0.72	
			I ₀ , I ₁ , I ₂ , I ₆ , I ₈			-0.36	
			I ₃ , I ₄ , I ₅ , I ₇			-0.72	
			RAM _{0, 3} , Q _{0, 3} (Note 4)			-0.8	
			C _n			-3.6	
I _{IH}	Input HIGH Current	V _{CC} = MAX., V _{IN} = 2.7V	Clock, OE			20	μA
			A ₀ , A ₁ , A ₂ , A ₃			20	
			B ₀ , B ₁ , B ₂ , B ₃			20	
			D ₀ , D ₁ , D ₂ , D ₃			40	
			I ₀ , I ₁ , I ₂ , I ₆ , I ₈			20	
			I ₃ , I ₄ , I ₅ , I ₇			40	
			RAM _{0, 3} , Q _{0, 3} (Note 4)			100	
			C _n			200	
I _I	Input HIGH Current	V _{CC} = MAX., V _{IN} = 5.5V				1.0	mA
I _{OZH} I _{OZL}	Off State (High Impedance) Output Current	V _{CC} = MAX.	Y ₀ , Y ₁ , Y ₂ , Y ₃	V _O = 2.4V		50	μA
				V _O = 0.5V		-50	
			RAM _{0, 3} Q _{0, 3}	V _O = 2.4V (Note 4)		100	
				V _O = 0.5V (Note 4)		-800	
I _{OS}	Output Short Circuit Current (Note 3)	V _{CC} = MAX. + 0.5V, V _O = 0.5V	Y ₀ , Y ₁ , Y ₂ , Y ₃ , Ḡ		-30	-85	mA
			C _{n+4}		-30	-85	
			OVR, P̄		-30	-85	
			F ₃		-30	-85	
			RAM _{0, 3} , Q _{0, 3}		-30	-85	
I _{CC}	Power Supply Current (Note 6)	V _{CC} = MAX. (See Fig. 11)	COM'L and MIL	T _A = 25°C		160	mA
			COM'L Only	T _A = 0°C to +70°C		265	
				T _A = +70°C		220	
			MIL Only	T _C = -55°C to +125°C		280	
			T _C = +125°C			198	

- Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
 2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
 4. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I₆₇₈ in a state such that the three-state output is OFF.
 5. "MIL" = Am2901XM, DM, FM. "COM'L" = Am2901XC, PC, DC.
 6. Worst case I_{CC} is at minimum temperature.
 7. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

Am2901 • 2901A • Am2901B

I. Am2901B Guaranteed Commercial Range Performance


The tables below specify the guaranteed performance of the Am2901B over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2901BPC
Am2901BDC

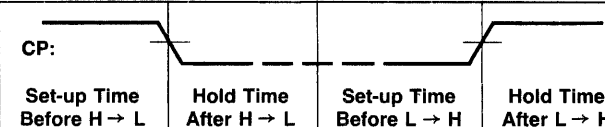
A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	69ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	16MHz
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Clock Period	69ns

B. Combinational Propagation Delays.
C_L = 50pF

To Output From Input	Y	F3	Cn+4	$\overline{G}, \overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address	60	61	59	50	70	67	71	—
D	38	36	40	33	48	44	45	—
Cn	30	29	20	—	37	29	38	—
I012	50	47	45	45	56	53	57	—
I345	51	52	52	45	60	49	53	—
I678	28	—	—	—	—	—	27	27
A Bypass ALU (I = 2XX)	37	—	—	—	—	—	—	—
Clock 	49	48	47	37	58	55	59	29

C. Set-up and Hold Times Relative to Clock (CP) Input.

Input	CP: 			
	Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	20	0 (Note 3)	69 (Note 4)	0
B Destination Address	15	Do Not Change		0
D	—	—	51	0
Cn	—	—	39	0
I012	—	—	56	0
I345	—	—	55	0
I678	11	Do Not Change		0
RAM0, 3, Q0, 3	—	—	16	0

D. Output Enable/Disable Times.

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
\overline{OE}	Y	35	25

- Notes: 1. A dash indicates a propagation delay path or set-up time constraint does not exist.
 2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
 3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
 4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes **all** the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

II. Am2901B Guaranteed Military Range Performance


The tables below specify the guaranteed performance of the Am2901B over the military operating range of -55°C to $+125^{\circ}\text{C}$, with V_{CC} from 4.5V to 5.5V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2901BDM
Am2901BFM

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.	88ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	15MHz
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Clock Period	88ns

B. Combinational Propagation Delays.
 $C_L = 50\text{pF}$

To Output From Input	Y	F3	Cn+4	$\overline{G}, \overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address	82	84	80	70	90	86	94	—
D	44	38	40	34	50	45	48	—
Cn	34	32	24	—	38	31	39	—
I012	53	50	47	46	65	55	58	—
I345	58	58	58	48	64	56	55	—
I678	29	—	—	—	—	—	27	27
A Bypass ALU (I = 2XX)	50	—	—	—	—	—	—	—
Clock 	53	50	49	41	63	58	61	31

2

C. Set-up and Hold Times Relative to Clock (CP) Input.

Input	CP:			
	Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	30	0 (Note 3)	88 (Note 4)	0
B Destination Address	15	Do Not Change		0
D	—	—	55	0
Cn	—	—	42	0
I012	—	—	58	0
I345	—	—	62	0
I678	14	Do Not Change		0
RAM0, 3, Q0, 3	—	—	18	3

D. Output Enable/Disable Times.

Output disable tests performed with $C_L = 5\text{pF}$ and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
\overline{OE}	Y	40	25

- Notes: 1. A dash indicates a propagation delay path or set-up time constraint does not exist.
 2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
 3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
 4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

III. Am2901A Guaranteed Commercial Range Performance

The Am2901B meets or exceeds all of the specifications for the earlier Am2901A.
Parts may still be ordered and marked as Am2901A.

IV. Am2901A Guaranteed Military Range Performance

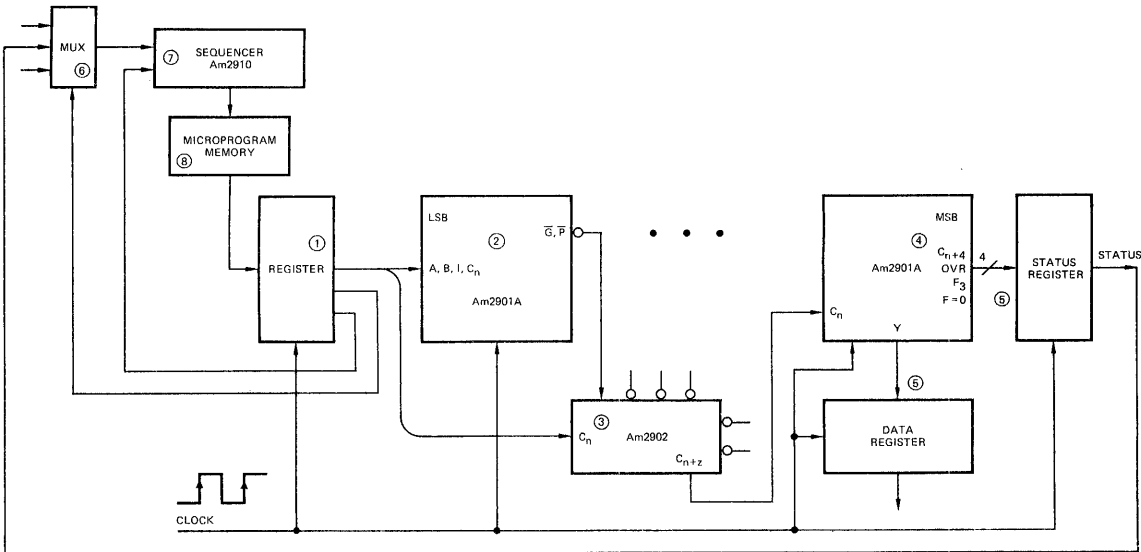
The Am2901B meets or exceeds all of the specifications for the earlier Am2901A.
Parts may still be ordered and marked as Am2901A.

V. Am2901 Guaranteed Commercial Range Performance

The Am2901B meets or exceeds all of the specifications of the Am2901.
Parts may still be ordered and marked as Am2901.

MINIMUM CYCLE TIME CALCULATIONS FOR 16-BIT SYSTEMS

Speeds used in calculations for parts other than Am2901B are representative for available MSI parts.



2

MPR-010

Pipelined System. Add without Simultaneous Shift.

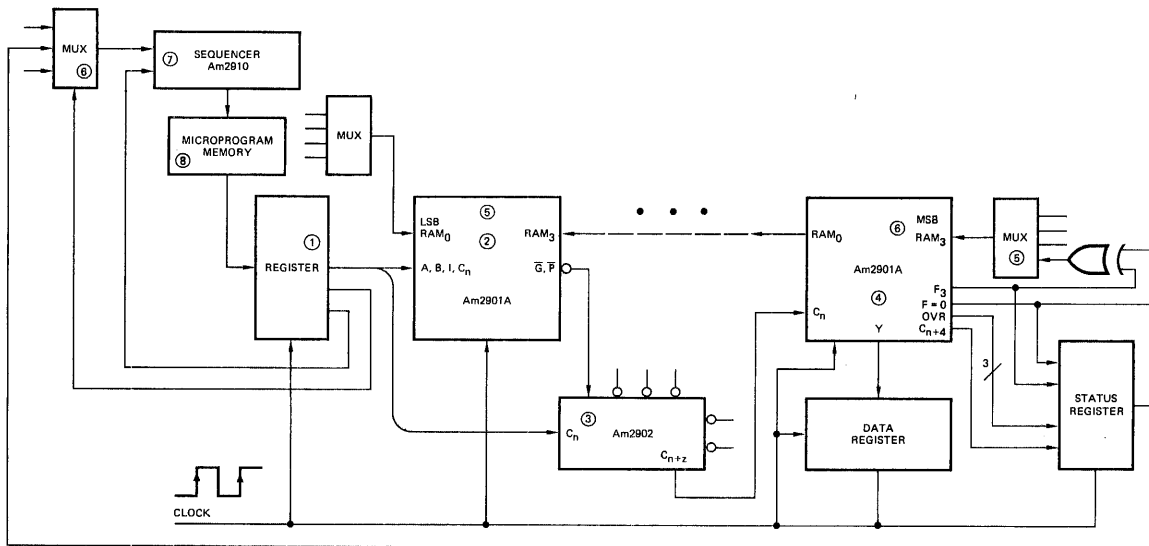
DATA LOOP			CONTROL LOOP		
① Register	Clock to Output	15	① Register	Clock to Output	15
+ ② 2901B	A, B to \bar{G} , \bar{P}	50	+ ⑥ MUX	Select to Output	20
+ ③ 2902	\bar{G}_0 , \bar{P}_0 to C_{n+z}	10	+ ⑦ 2910	CC to Output	45
+ ④ 2901B	C_n to C_{n+4} , OVR, F_3 , $F = 0$, Y	37	+ ⑧ PROM	Access Time	55
+ ⑤ Register	Set-up Time	5	+ ① Register	Set-up Time	5
		117ns			140ns

Minimum clock period = 140ns

Figure 12.

MINIMUM CYCLE TIME CALCULATIONS FOR 16-BIT SYSTEMS (Cont.)

Speeds used in calculations for parts other than Am2901B are representative for available MSI parts.



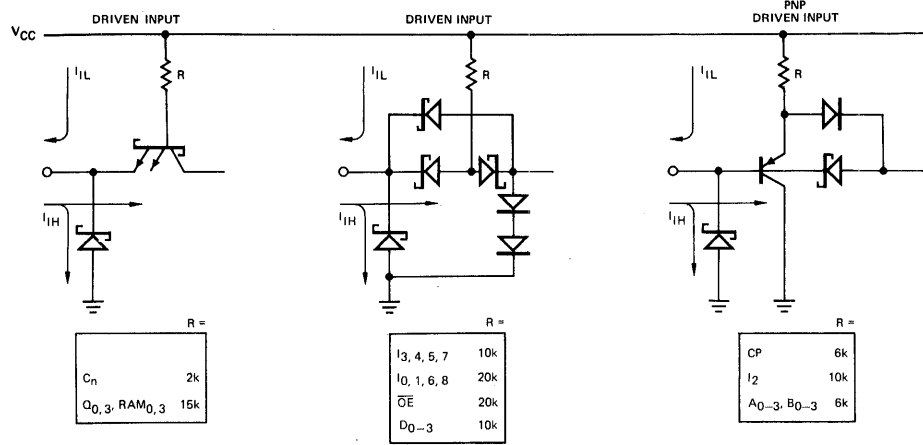
MPR-011

Pipelined System. Simultaneous Add and Shift Down.

DATA LOOP			CONTROL LOOP		
① Register	Clock to Output	15	① Register	Clock to Output	15
+ ② 2901B	A, B to \bar{G} , \bar{P}	50	+ ⑥ MUX	Select to Output	20
+ ③ 2902	$\bar{G}_0\bar{P}_0$ to C_{n+z}	10	+ ⑦ 2910	CC to Output	45
+ ④ 2901B	C_n to F_3 , OVR	29	+ ⑧ PROM	Access Time	55
+ ⑤ XOR and MUX		21	+ ① Register	Set-up Time	5
+ ⑥ 2901B	RAM_3 Set-up	16			140ns
		141ns			

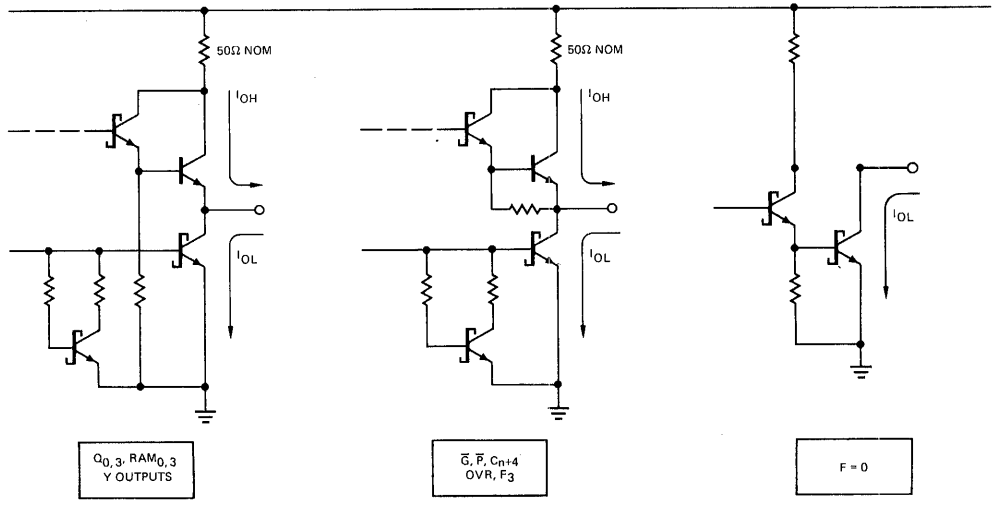
Minimum clock period = 141ns

Figure 12 (Cont.).



MPR-013

C_I ≈ 5.0pF, all inputs



MPR-014

C_O ≈ 5.0pF, all outputs

Figure 13. Input/Output Current Interface Conditions.

