TOSHIBA MOS MEMORY PRODUCTS

128K BIT (16K WORD × 8 BIT) MASK ROM
N-CHANNEL SILICON GATE

TMM23128P

220667

DESCRIPTION

The TMM23128P is a 131,072 bit read only memory organized as 16,384 words by 8 bits with low bit cost, thus being suitable for use in program memory for microprocessor and character generator.

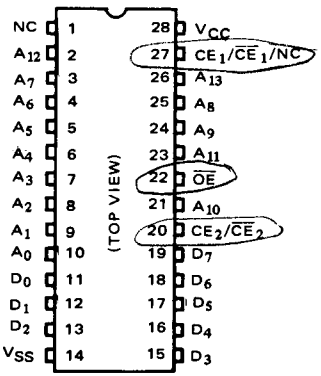
The TMM23128P is fully compatible with a 128K bits EPROM TMM27128D, so completely replace EPROM socket.

The TMM23128P also features an automatic standby power mode. When deselected by Chip Enable ($\overline{CE}_1$, 2/$\overline{CE}_1$, 2), the operating current is reduced form 80mA (Max.) to 20mA (Max.). Output Enable ($\overline{OE}$) is effective in preventing data confliction of a common bus line. The TMM23128P is fabricated with ion implanted N-channel silicon gate technology. The TMM23128P is moulded in a 28 pin standard plastic package, 0.6 inch in width.

FEATURES

- Fully Static Operation
- 16,384 word x 8 bit Structure
- Single 5V Power Supply
- t_{ACC} = 200ns Max.
- T_{opr} = 0 ~ 70°C
- I_{CC} ope = 80mA Max.
- I_{CC} sby = 20mA Max.
- Input and Output TTL Compatible
- Three State Outputs
- Programmable Chip Enable
- Pin Compatible with EPROM TMM27128D
- 28 pin 600 mil. width DIP Plastic Package

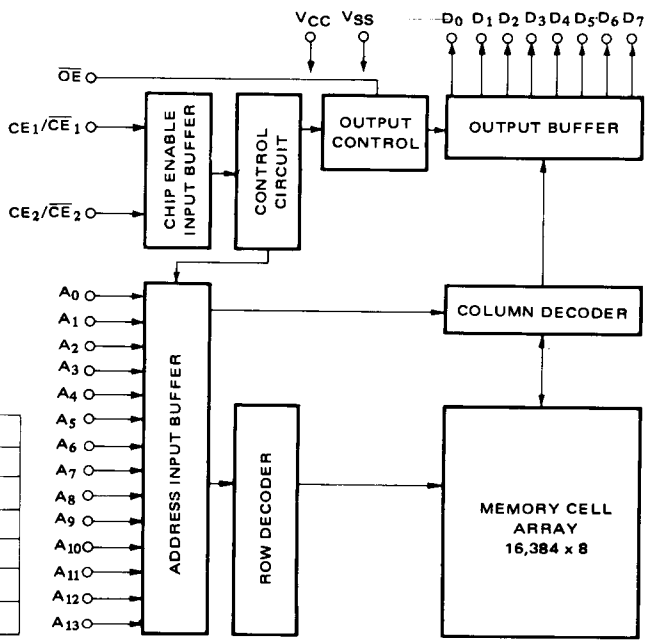
PIN CONNECTION



PIN NAMES

$A_0 \sim A_{13}$	Address Inputs
$D_0 \sim D_7$	Data Outputs
$CE_1 \sim {}_2/\overline{CE}_1 \sim {}_2$	Chip Enable Inputs
$\overline{OE}$	Output Enable Input
NC	No Connection
V_{CC}	5V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}, V_{OUT}	Input and Output Voltage	−0.5 ~ 7.0	V
P_D	Power Dissipation (Ta = 70°C)	1.0	W
T_{OPR}	Operating Temperature	0 ~ 70	°C
T_{STG}	Storage Temperature	−55 ~ 150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

D.C. OPERATING CONDITIONS (Ta = 0 ~ 70°C)

SYMBOL	ITEM	MIN.	MAX.	UNIT
V_{CC}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	V_{CC} + 1	V
V_{IL}	Input Low Voltage	−0.5	0.8	V

D.C. AND OPERATING CHARACTERISTICS (Ta = 0 ~ 70°C)

SYMBOL	ITEM	CONDITIONS	MIN.	MAX.	UNIT
I_{IN}	Input Current	$0V \leqq V_{IN} \leqq V_{CC}$	–	±10	μA
I_{LO}	Output Leakage Current	$0V \leqq V_{OUT} \leqq V_{CC}$	–	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−400	–	μA
I_{OL}	Output Low Current	V_{OL} = 0.4V	3.2	–	mA
I_{CC} ope	Operating Current	Min. Cycle	–	80	mA
I_{CC} sby	Standby Current	Note 1	–	20	mA

Note 1: Standby state occurs when either $CE_1/\overline{CE}_1$ or $CE_2/\overline{CE}_2$ is disenabled.

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	ITEM	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = AC GND	–	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = AC GND	–	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

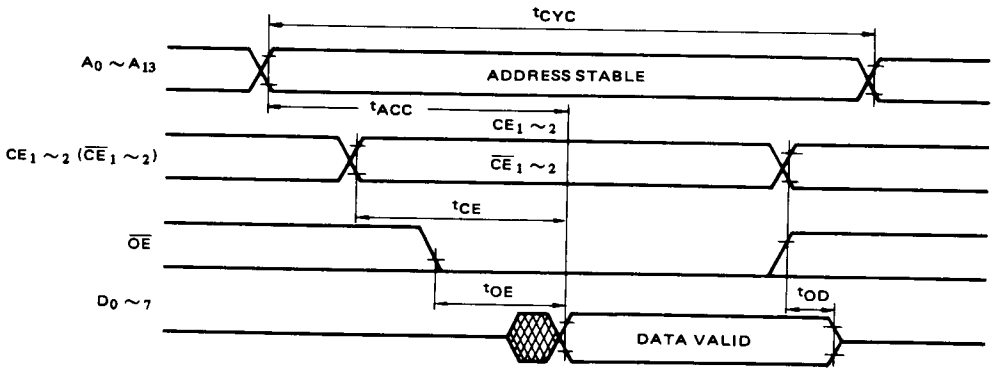
A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%)

SYMBOL	ITEM	MIN.	MAX.	UNIT
t_{ACC}	Access Time	–	200	ns
t_{CE}	Output Delay Time from $CE_{1\sim2}/\overline{CE}_{1\sim2}$	–	200	ns
t_{OE}	Output Delay Time from $\overline{OE}$	–	70	ns
t_{OD}	Output Turn Off Delay	–	60	ns
t_{CYC}	Cycle Time	200	–	ns

AC Test Conditions

- Output Load : 1 TTL + 100pF
- Input Rise and Fall Times (10% to 90%) : 5 ns
- Input Pulse Levels : 0.6V to 2.4V
- Timing Measurement Reference Levels : Input : 0.8V and 2.2V
  Output : 0.8V and 2.0V

TIMING WAVEFORMS



Note:
1) t_{CE} specifies the time interval of $CE_1 \sim_2$ ($\overline{CE}_1 \sim_2$) to become active until it is actually being output.
2) t_{OD} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

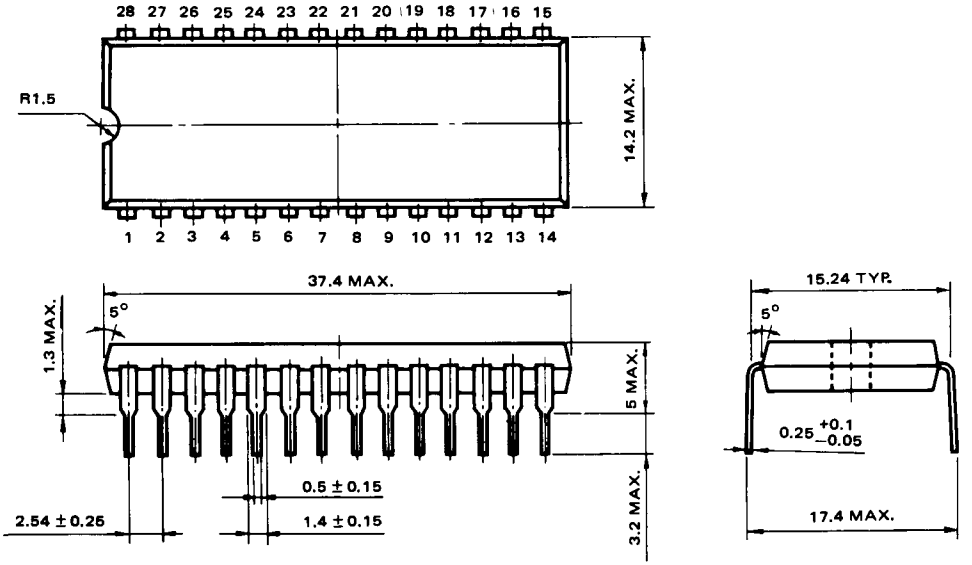
APPLICATION INFORMATION

TMM23128P has self substrate-bias generator internally. So a minimum 100μs time delay is required after the application of V_{CC} (4.5V to 5.5V) before proper device operation is achieved.

TMM23128P

OUTLINE DRAWINGS

Unit in mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.