

**TQFP, BGA**  
**Commercial Temp**  
**Industrial Temp**

**256K x 18 Sync**  
**Cache Tag**

**180 MHz–100 MHz**  
**3.3 V V<sub>DD</sub>**  
**3.3 V and 2.5 V I/O**

## Features

- 3.3 V +10%/–5% core power supply, 2.5 V or 3.3 V I/O supply
- Dual Cycle Deselect (DCD)
- Integrated data comparator for Tag RAM application
- $\overline{FT}$  mode pin for flow through or pipeline operation
- $\overline{LBO}$  pin for Linear or Interleave (Pentium™ and X86) Burst mode
- Synchronous address, data I/O, and control inputs
- Synchronous Data Enable ( $\overline{DE}$ )
- Asynchronous Output Enable ( $\overline{OE}$ )
- Asynchronous Match Output Enable ( $\overline{MOE}$ )
- Byte Write ( $\overline{BWE}$ ) and Global Write ( $\overline{GW}$ ) operation
- Three chip enable signals for easy depth expansion
- Internal self-timed write cycle
- JTAG Test mode conforms to IEEE standard 1149.1
- JEDEC-standard 100-lead TQFP package and 119-BGA packages available

## Functional Description

The GS841E18A is a 256K x 18 high performance synchronous DCD SRAM with integrated Tag RAM comparator. A 2-bit burst counter is included to provide burst interface with Pentium™ and other high performance CPUs. It is designed to be used as a Cache Tag SRAM, as well as data SRAM. Addresses, data I/Os, match output, chip enables ( $\overline{CE1}$ ,  $\overline{CE2}$ ,  $\overline{CE3}$ ), address control inputs ( $\overline{ADSP}$ ,  $\overline{ADSC}$ ,  $\overline{ADV}$ ), and write control inputs ( $\overline{BW1}$ ,  $\overline{BW2}$ ,  $\overline{BWE}$ ,  $\overline{GW}$ ,  $\overline{DE}$ ) are synchronous and are controlled by a positive-edge-triggered clock (CLK).

Output Enable ( $\overline{OE}$ ), Match Output Enable, and power down control ( $\overline{ZZ}$ ) are asynchronous. Burst can be initiated with either  $\overline{ADSP}$  or  $\overline{ADSC}$  inputs. Subsequent burst addresses are generated internally and are controlled by  $\overline{ADV}$ . The burst sequence is either interleave order (Pentium™ or x86) or linear order, and is controlled by  $\overline{LBO}$ .

Output registers and the Match output register are provided and controlled by the  $\overline{FT}$  mode pin (Pin 14). Through use of the  $\overline{FT}$  mode pin, I/O registers can be programmed to perform pipeline or flow through operation. Flow Through mode reduces latency.

Byte write operation is performed by using Byte Write Enable ( $\overline{BWE}$ ) input combined with two individual byte write signals  $\overline{BW1}$ -2. In addition, Global Write ( $\overline{GW}$ ) is available for writing all bytes at one time.

Compare cycles begin as a read cycle with output disabled so that compare data can be loaded into the data input register. The comparator compares the read data with the registered input data and a match signal is generated. The match output can be either in Pipeline or Flow Through modes controlled by the  $\overline{FT}$  signal.

Low power (Standby mode) is attained through the assertion of the  $\overline{ZZ}$  signal, or by stopping the clock (CLK). Memory data is retained during Standby mode.

JTAG boundary scan interface is provided using IEEE standard 1149.1 protocol. Four pins—Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK) and Test Mode Select (TMS)—are used to perform JTAG function.

The GS841E18A operates on a 3.3 V power supply and all inputs/ outputs are 3.3 V- or 2.5 V-LVTTL-compatible. Separate output ( $V_{DDQ}$ ) pins are used to allow both 3.3 V or 2.5 V IO interface.

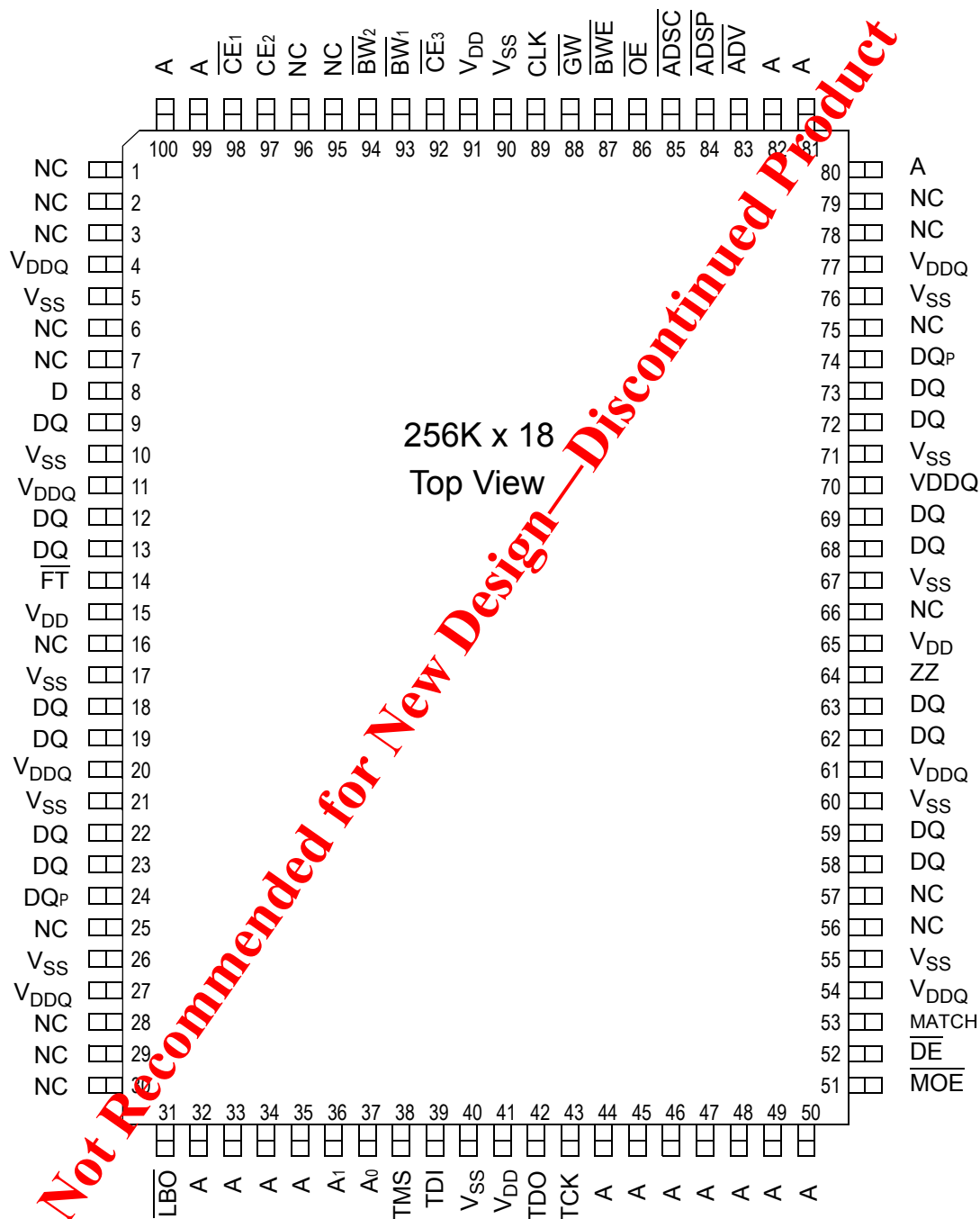
## Dual Cycle Deselect (DCD)

The GS841E18A is a DCD pipelines synchronous SRAM. DCD SRAMs pipeline disable commands to the same degree as read commands. DCD SRAMs hold the deselect command for one full cycle and then begin turning off their outputs just after the second rising edge of the clock.

## Parameter Synopsis

|                                                 |                    | -180   | -166   | -150   | -133   | -100   |
|-------------------------------------------------|--------------------|--------|--------|--------|--------|--------|
| <b>Pipeline</b><br><b>3-1-1-1</b>               | $t_{\text{cycle}}$ | 5.5 ns | 6.0 ns | 6.6 ns | 7.5 ns | 10 ns  |
|                                                 | $t_{\text{KQ}}$    | 3.2 ns | 3.5 ns | 3.8 ns | 4.0 ns | 4.5 ns |
|                                                 | $I_{\text{DD}}$    | 335 mA | 310 mA | 275 mA | 250 mA | 190 mA |
| <b>Flow</b><br><b>Through</b><br><b>2-1-1-1</b> | $t_{\text{KQ}}$    | 8 ns   | 8.5 ns | 10 ns  | 11 ns  | 12 ns  |
|                                                 | $t_{\text{cycle}}$ | 9.1 ns | 10 ns  | 10 ns  | 15 ns  | 15 ns  |
|                                                 | $I_{\text{DD}}$    | 210 mA | 190 mA | 190 mA | 140 mA | 140 mA |

# Pin Configuration (Package T)



## Note:

Pins marked with NC can be tied to either V<sub>DD</sub> or V<sub>SS</sub>. These pins can also be left floating.

## GS841E18A PadOut—119-Bump BGA—Top View (Package B)

|   | 1                | 2               | 3                       | 4                        | 5                      | 6                       | 7                      |
|---|------------------|-----------------|-------------------------|--------------------------|------------------------|-------------------------|------------------------|
| A | V <sub>DDQ</sub> | A               | A                       | $\overline{\text{ADSP}}$ | A                      | A                       | V <sub>DDQ</sub>       |
| B | NC               | E2              | A                       | $\overline{\text{ADSC}}$ | A                      | $\overline{\text{E3}}$  | NC                     |
| C | NC               | A               | A                       | V <sub>DD</sub>          | A                      | A                       | NC                     |
| D | DQB              | NC              | V <sub>SS</sub>         | NC                       | V <sub>SS</sub>        | DQP                     | NC                     |
| E | NC               | DQB             | V <sub>SS</sub>         | $\overline{\text{E1}}$   | V <sub>SS</sub>        | NC                      | DQA                    |
| F | V <sub>DDQ</sub> | NC              | V <sub>SS</sub>         | $\overline{\text{G}}$    | V <sub>SS</sub>        | DQA                     | V <sub>DDQ</sub>       |
| G | NC               | DQB             | $\overline{\text{Bb}}$  | $\overline{\text{ADV}}$  | NC                     | NC                      | DQA                    |
| H | DQB              | NC              | V <sub>SS</sub>         | $\overline{\text{CW}}$   | V <sub>SS</sub>        | DQA                     | NC                     |
| J | V <sub>DDQ</sub> | V <sub>DD</sub> | NC                      | V <sub>DD</sub>          | NC                     | V <sub>DD</sub>         | V <sub>DDQ</sub>       |
| K | NC               | DQB             | V <sub>SS</sub>         | CK                       | V <sub>SS</sub>        | NC                      | DQA                    |
| L | DQB              | NC              | NC                      | NC                       | $\overline{\text{BA}}$ | DQA                     | NC                     |
| M | V <sub>DDQ</sub> | DQB             | V <sub>SS</sub>         | $\overline{\text{BW}}$   | V <sub>SS</sub>        | MATCH                   | V <sub>DDQ</sub>       |
| N | DQB              | NC              | V <sub>SS</sub>         | A1                       | V <sub>SS</sub>        | DQA                     | $\overline{\text{DE}}$ |
| P | NC               | DQP             | V <sub>SS</sub>         | A0                       | V <sub>SS</sub>        | $\overline{\text{MOE}}$ | DQA                    |
| R | NC               | A               | $\overline{\text{LBO}}$ | V <sub>DD</sub>          | $\overline{\text{FT}}$ | A                       | NC                     |
| T | NC               | A               | A                       | NC                       | A                      | A                       | ZZ                     |
| U | V <sub>DDQ</sub> | TMS             | TDI                     | TCK                      | TDO                    | NC                      | V <sub>DDQ</sub>       |

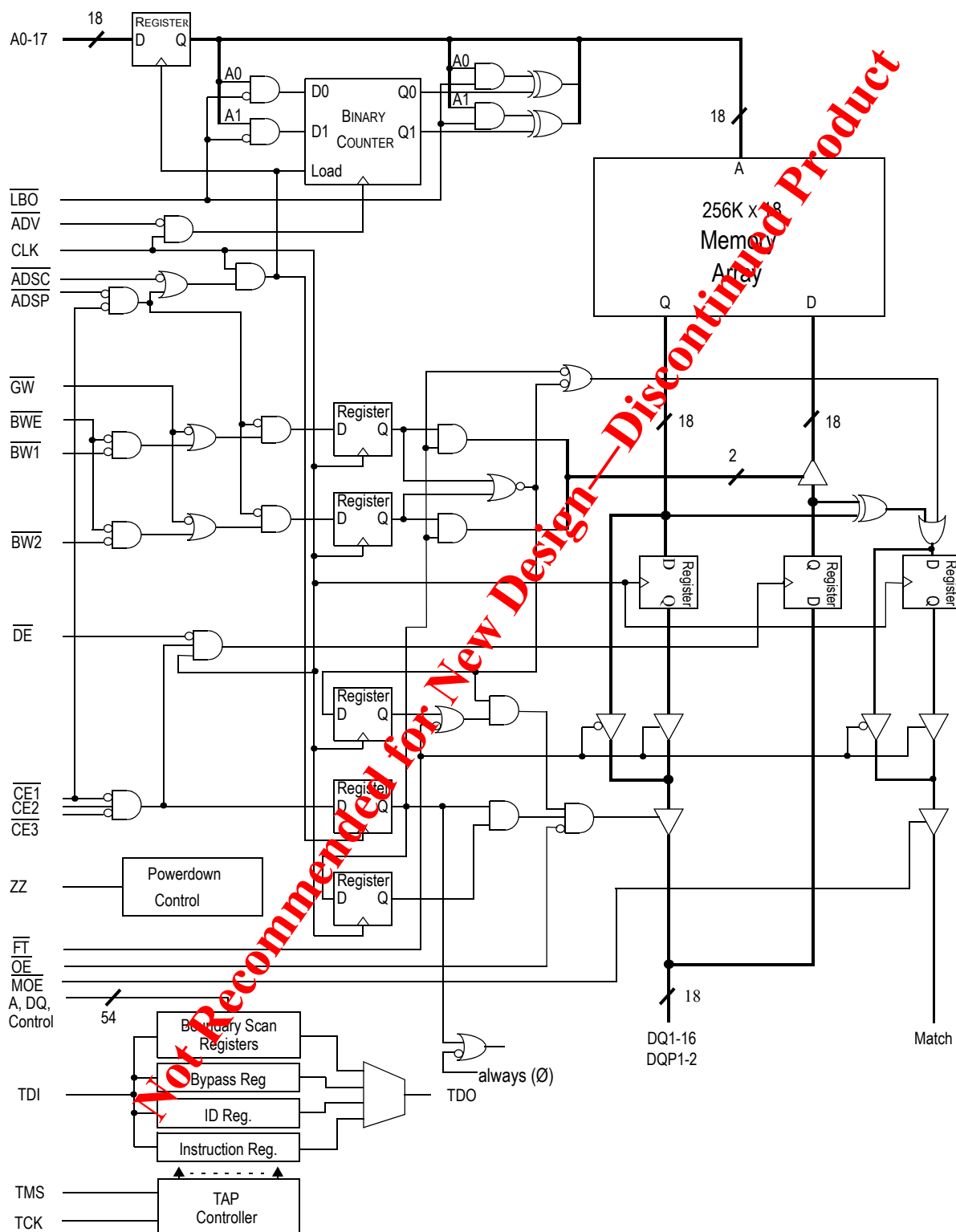
# TQFP Pin Description

| Symbol                                                                | Description                                                                                                                                        |
|-----------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| An                                                                    | Address Input Signals—Inputs are registered and must meet setup and hold times, as specified on page 11.                                           |
| CLK                                                                   | Clock Input Signal                                                                                                                                 |
| $\overline{\text{BWE}}$                                               | Byte Write Enable Signal—The byte write enable signal needs to be combined with one of the four byte write signals for a write operation to occur. |
| $\overline{\text{BW1}}$                                               | Byte Write signal for data outputs 1 thru 8                                                                                                        |
| $\overline{\text{BW2}}$                                               | Byte Write signal for data outputs 9 thru 16                                                                                                       |
| $\overline{\text{GW}}$                                                | Global Write Enable                                                                                                                                |
| $\overline{\text{CE1}}, \overline{\text{CE2}}, \overline{\text{CE3}}$ | Chip Enables                                                                                                                                       |
| $\overline{\text{OE}}$                                                | Output Enable                                                                                                                                      |
| $\overline{\text{ADV}}$                                               | Burst address advance                                                                                                                              |
| $\overline{\text{ADSP}}, \overline{\text{ADSC}}$                      | Address status signals                                                                                                                             |
| DQ                                                                    | Data Input and Output pins                                                                                                                         |
| DQP                                                                   | Parity Input and Output pins                                                                                                                       |
| MATCH                                                                 | Match Output                                                                                                                                       |
| $\overline{\text{MOE}}$                                               | Match Output Enable                                                                                                                                |
| $\overline{\text{DE}}$                                                | Data Enable—Data input registers are updated only when $\overline{\text{DE}}$ is active.                                                           |
| ZZ                                                                    | Power down control—Application of ZZ will result in a low standby power consumption.                                                               |
| $\overline{\text{FT}}$                                                | Flow Through or Pipeline mode                                                                                                                      |
| $\overline{\text{LBO}}$                                               | Linear Order Burst mode                                                                                                                            |
| TMS                                                                   | Test Mode Select                                                                                                                                   |
| TDI                                                                   | Test Data In                                                                                                                                       |
| TDO                                                                   | Test Data Out                                                                                                                                      |
| TCK                                                                   | Test Clock                                                                                                                                         |
| V <sub>DD</sub>                                                       | 3.3 V power supply                                                                                                                                 |
| V <sub>SS</sub>                                                       | Ground                                                                                                                                             |
| V <sub>DDQ</sub>                                                      | 2.5 V/3.3 V output power supply                                                                                                                    |
| NC                                                                    | No Connect                                                                                                                                         |

## PBGA Pin Description

| Symbol                                                                | Description                                                                                                                                        |
|-----------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| An                                                                    | Address Input Signals—Inputs are registered and must meet setup and hold times, as specified on page 11.                                           |
| CLK                                                                   | Clock Input Signal                                                                                                                                 |
| $\overline{\text{BWE}}$                                               | Byte Write Enable Signal—The byte write enable signal needs to be combined with one of the four byte write signals for a write operation to occur. |
| $\overline{\text{BW1}}$                                               | Byte Write signal for data outputs 1 thru 8                                                                                                        |
| $\overline{\text{BW2}}$                                               | Byte Write signal for data outputs 9 thru 16                                                                                                       |
| $\overline{\text{GW}}$                                                | Global Write Enable                                                                                                                                |
| $\overline{\text{CE1}}, \overline{\text{CE2}}, \overline{\text{CE3}}$ | Chip Enables                                                                                                                                       |
| $\overline{\text{OE}}$                                                | Output Enable                                                                                                                                      |
| $\overline{\text{ADV}}$                                               | Burst address advance                                                                                                                              |
| $\overline{\text{ADSP}}, \overline{\text{ADSC}}$                      | Address status signals                                                                                                                             |
| DQ                                                                    | Data Input and Output pins                                                                                                                         |
| DQP                                                                   | Parity Input and Output pins                                                                                                                       |
| MATCH                                                                 | Match Output                                                                                                                                       |
| $\overline{\text{MOE}}$                                               | Match Output Enable                                                                                                                                |
| $\overline{\text{DE}}$                                                | Data Enable—Data input registers are updated only when $\overline{\text{DE}}$ is active.                                                           |
| ZZ                                                                    | Power down control—Application of ZZ will result in a low standby power consumption.                                                               |
| $\overline{\text{FT}}$                                                | Flow Through or Pipeline mode                                                                                                                      |
| $\overline{\text{LBO}}$                                               | Linear Order Burst mode                                                                                                                            |
| TMS                                                                   | Test Mode Select                                                                                                                                   |
| TDI                                                                   | Test Data In                                                                                                                                       |
| TDO                                                                   | Test Data Out                                                                                                                                      |
| TCK                                                                   | Test Clock                                                                                                                                         |
| V <sub>DD</sub>                                                       | 3.3 V power supply                                                                                                                                 |
| V <sub>SS</sub>                                                       | Ground                                                                                                                                             |
| V <sub>DDQ</sub>                                                      | 2.5 V/3.3 V output power supply                                                                                                                    |
| NC                                                                    | No Connect                                                                                                                                         |

# Functional Block Diagram



## Mode Pin Function

| LBO     | Function          |
|---------|-------------------|
| L       | Linear Burst      |
| H or NC | Interleaved Burst |

| FT      | Function     |
|---------|--------------|
| L       | Flow Through |
| H or NC | Pipeline     |

## Power Down Control

| ZZ      | Function           |
|---------|--------------------|
| L or NC | Active             |
| H       | Standby, IDD = ISB |

### Note:

There are pull up devices on  $\overline{\text{LBO}}$  and  $\overline{\text{FT}}$  pins and pull down device on ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

### Linear Burst Sequence

|             | A[1:0] | A[1:0] | A[1:0] | A[1:0] |
|-------------|--------|--------|--------|--------|
| 1st address | 00     | 01     | 10     | 11     |
| 2nd address | 01     | 10     | 11     | 00     |
| 3rd address | 10     | 11     | 00     | 01     |
| 4th address | 11     | 00     | 01     | 10     |

### Interleaved Burst Sequence

|             | A[1:0] | A[1:0] | A[1:0] | A[1:0] |
|-------------|--------|--------|--------|--------|
| 1st address | 00     | 01     | 10     | 11     |
| 2nd address | 01     | 00     | 11     | 10     |
| 3rd address | 10     | 11     | 00     | 01     |
| 4th address | 11     | 10     | 01     | 00     |

### Byte Write Function

| Function        | GW | BWE | BW1 | BW2 |
|-----------------|----|-----|-----|-----|
| Read            | H  | H   | X   | X   |
| Read            | H  | L   | H   | H   |
| Write all bytes | L  | X   | X   | X   |
| Write all bytes | H  | L   | L   | L   |
| Write byte 1    | H  | L   | L   | H   |
| Write byte 2    | H  | L   | H   | L   |

Note: H = logic high, L = logic low, NC = no connect

## Synchronous Truth Table

| Operation                   | Address Used | CE1 | CE2 | CE3 | ADSP | ADSC | ADV | Write | OE | CLK | DQ     |
|-----------------------------|--------------|-----|-----|-----|------|------|-----|-------|----|-----|--------|
| Deselect Cycle, Power Down  | none         | H   | X   | X   | X    | L    | X   | X     | X  | L-H | High-Z |
| Deselect Cycle, Power Down  | none         | L   | L   | X   | L    | X    | X   | X     | X  | L-H | High-Z |
| Deselect Cycle, Power Down  | none         | L   | X   | H   | L    | X    | X   | X     | X  | L-H | High-Z |
| Deselect Cycle, Power Down  | none         | L   | L   | X   | H    | L    | X   | X     | X  | L-H | High-Z |
| Deselect Cycle, Power Down  | none         | L   | X   | H   | H    | L    | X   | X     | X  | L-H | High-Z |
| Read Cycle, Begin Burst     | external     | L   | H   | L   | L    | X    | X   | X     | L  | L-H | Q      |
| Read Cycle, Begin Burst     | external     | L   | H   | L   | L    | X    | X   | X     | H  | L-H | High-Z |
| Read Cycle, Begin Burst     | external     | L   | H   | L   | H    | X    | X   | H     | L  | L-H | Q      |
| Read Cycle, Begin Burst     | external     | L   | H   | L   | H    | L    | X   | H     | H  | L-H | High-Z |
| Write Cycle, Begin Burst    | external     | L   | H   | L   | H    | L    | X   | L     | X  | L-H | D      |
| Read Cycle, Continue Burst  | next         | X   | X   | X   | H    | H    | L   | H     | L  | L-H | Q      |
| Read Cycle, Continue Burst  | next         | X   | X   | X   | H    | H    | L   | H     | H  | L-H | High-Z |
| Read Cycle, Continue Burst  | next         | H   | X   | X   | X    | H    | L   | H     | L  | L-H | Q      |
| Read Cycle, Continue Burst  | next         | H   | X   | X   | X    | H    | L   | H     | H  | L-H | High-Z |
| Write Cycle, Continue Burst | next         | X   | X   | X   | H    | H    | L   | L     | X  | L-H | D      |
| Write Cycle, Continue Burst | next         | H   | X   | X   | X    | H    | L   | L     | X  | L-H | D      |
| Read Cycle, Suspend Burst   | current      | X   | X   | X   | H    | H    | H   | H     | L  | L-H | Q      |
| Read Cycle, Suspend Burst   | current      | X   | X   | X   | H    | H    | H   | H     | H  | L-H | High-Z |
| Read Cycle, Suspend Burst   | current      | H   | X   | X   | X    | H    | H   | H     | L  | L-H | Q      |
| Read Cycle, Suspend Burst   | current      | H   | X   | X   | X    | H    | H   | H     | H  | L-H | High-Z |
| Write Cycle, Suspend Burst  | current      | X   | X   | X   | H    | H    | H   | L     | X  | L-H | D      |
| Write Cycle, Suspend Burst  | current      | H   | X   | X   | X    | H    | H   | L     | X  | L-H | D      |

### Notes:

1. X means "don't care," H means "logic high," L means "logic low."
2. Write is the logic function of  $\overline{GW}$ ,  $\overline{LWE}$ ,  $\overline{BW1}$ ,  $\overline{BW2}$ . See Byte Write Function table for detail.
3. All inputs, except OE, must meet setup and hold on rising edge of CLK.
4. Suspending burst generates a wait cycle.
5. ADSP LOW along with CS#M being selected always initiates a Read cycle at the L-H edge of the clock (CLK).
6. A Write cycle can only be performed by setting Write low for the clock L-H edge of the subsequent wait cycle. Refer to **page 12** for the Write timing diagram.

**Truth Table For Read/Write/Compare/Fill Write Operation**

|                | CE | Write | DE | MOE | OE | Match    | DQ     |
|----------------|----|-------|----|-----|----|----------|--------|
| Read           | L  | H     | X  | X   | L  | —        | Q      |
| Write          | L  | L     | L  | X   | H  | —        | D      |
| Compare        | L  | H     | L  | L   | H  | Data Out | D      |
| Fill Write     | L  | L     | H  | X   | X  | —        | X      |
| Match Deselect | H  | X     | X  | L   | X  | High     | High Z |
| Deselect       | H  | X     | X  | H   | X  | High Z   | High Z |

**Notes:**

1. X means "don't care," H means "logic high," L means "logic low."
2. Write is the logic function of  $\overline{GW}$ ,  $\overline{BWE}$ ,  $\overline{BW1}$ ,  $\overline{BW2}$ . See Byte Write Function table for details.
3.  $\overline{CE}$  is defined as  $\overline{CE1}=L$ ,  $\overline{CE2}=H$  and  $\overline{CE3}=L$
4. All signals are synchronous and are sampled by CLK except  $\overline{OE}$  and  $\overline{MOE}$ .  $\overline{OE}$  and  $\overline{MOE}$  are asynchronous and drive the bus immediately.

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**Absolute Maximum Ratings** (Voltage reference to  $V_{SS} = 0$  V)

| Symbol    | Description            | Commercial                                      | Unit |
|-----------|------------------------|-------------------------------------------------|------|
| $V_{DD}$  | Supply Voltage         | -0.5 to 4.6                                     | V    |
| $V_{DDQ}$ | Output Supply Voltage  | -0.5 to $V_{DD}$                                | V    |
| $V_{CLK}$ | CLK Input Voltage      | -0.5 to 6                                       | V    |
| $V_{in}$  | Input Voltage          | -0.5 to $V_{DD} + 0.5$<br>( $\leq 4.6$ V max. ) | V    |
| $V_{out}$ | Output Voltage         | -0.5 to $V_{DD} + 0.5$<br>( $\leq 4.6$ V max. ) | V    |
| $I_{out}$ | Output Current per I/O | +/-20                                           | mA   |
| $P_D$     | Power Dissipation      | 1.5                                             | W    |
| $T_{OPR}$ | Operating Temperature  | 0 to 70                                         | °C   |
| $T_{STG}$ | Storage Temperature    | -55 to 125                                      | °C   |

**Note:**

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the recommended operation conditions. Exposure to higher than recommended voltages, for an extended period of time, could effect the performance and reliability of this component.

## Package Thermal Characteristics

| Rating                           | Layer Board | Symbol          | TQFP max | PBGA max | Unit                 | Notes |
|----------------------------------|-------------|-----------------|----------|----------|----------------------|-------|
| Junction to Ambient (at 200 lfm) | single      | $R_{\Theta JA}$ | 32       | 28       | $^{\circ}\text{C/W}$ | 1,2   |
| Junction to Ambient (at 200 lfm) | four        | $R_{\Theta JA}$ | 20       | 18       | $^{\circ}\text{C/W}$ | 1,2   |
| Junction to Case (TOP)           | —           | $R_{\Theta JC}$ | 7        | 5        | $^{\circ}\text{C/W}$ | 3     |

### Notes:

- Junction temperature is a function of SRAM power dissipation, package thermal resistance, mounting board temperature, ambient. Temperature air flow, board density, and PCB thermal resistance.
- SCMI G-38-87.
- Average thermal resistance between die and top surface, MIL SPEC-883, Method 1012.1.

### AC Test Conditions

(VDD = 3.135 V–3.6 V, Ta = 0–70°C)

| Parameter              | Conditions               |
|------------------------|--------------------------|
| Input high level       | $V_{IH} = 2.3 \text{ V}$ |
| Input low level        | $V_{IL} = 0.2 \text{ V}$ |
| Input slew rate        | $1R = 1 \text{ V/ns}$    |
| Input reference level  | 1.25 V                   |
| Output reference level | 1.25 V                   |
| Output load            | Fig. 1 & 2               |

### Notes:

- Include scope and jig capacitance.
- Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
- Output load 2 for  $t_{LZ}$ ,  $t_{HZ}$ ,  $t_{OLZ}$  and  $t_{OHZ}$ .
- Device is deselected as defined by the Truth Table.

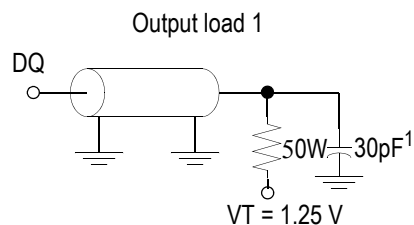


FIG. 1

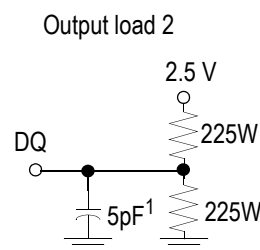


FIG. 2

**DC Characteristics and Supply Currents** (Voltage reference to  $V_{SS} = 0$  V)

(VDD = 3.135 V–3.6 V, Ta = 0–70°C for Commercial Temperature Offering)

| Parameter                                          | Symbol     | Test Conditions                                                           | Min                         | Max                      |
|----------------------------------------------------|------------|---------------------------------------------------------------------------|-----------------------------|--------------------------|
| Input Leakage Current<br>(except ZZ, FT, LBO pins) | $I_{IL}$   | $V_{IN} = 0$ to $V_{DD}$                                                  | –1 $\mu$ A                  | 1 $\mu$ A                |
| ZZ Input Current                                   | $I_{inZZ}$ | $V_{DD} \geq V_{IN} \geq V_{IH}$<br>$0 \text{ V} \leq V_{IN} \leq V_{IH}$ | –1 $\mu$ A<br>–1 $\mu$ A    | 1 $\mu$ A<br>300 $\mu$ A |
| Mode Input Current<br>(FT & LBO pins)              | $I_{inM}$  | $V_{DD} \geq V_{IN} \geq V_{IL}$<br>$0 \text{ V} \leq V_{IN} \leq V_{IL}$ | –30 0 $\mu$ A<br>–1 $\mu$ A | 1 $\mu$ A<br>1 $\mu$ A   |
| Output Leakage Current                             | $I_{ol}$   | Output Disable,<br>$V_{OUT} = 0$ to $V_{DD}$                              | –1 $\mu$ A                  | 1 $\mu$ A                |
| Output High Voltage                                | $V_{OH}$   | $I_{OH} = -4 \text{ mA}$ , $V_{DDQ} = 2.375 \text{ V}$                    | 1.7 V                       |                          |
| Output High Voltage                                | $V_{OH}$   | $I_{OH} = -4 \text{ mA}$ , $V_{DDQ} = 3.135 \text{ V}$                    | 2.4 V                       |                          |
| Output Low Voltage                                 | $V_{OL}$   | $I_{OL} = +4 \text{ mA}$                                                  |                             | 0.4 V                    |

**Not Recommended for New Design—Discontinued Product**

## Operating Currents

| Parameter                  | Test Conditions                                                                       | Symbol                      | -180            |                   | -166            |                    | -150            |                    | -133            |                    | -100            |                    | Unit |
|----------------------------|---------------------------------------------------------------------------------------|-----------------------------|-----------------|-------------------|-----------------|--------------------|-----------------|--------------------|-----------------|--------------------|-----------------|--------------------|------|
|                            |                                                                                       |                             | 0<br>to<br>70°C | -40<br>to<br>85°C | 0<br>to<br>70°C | -40<br>to<br>+85°C | 0<br>to<br>70°C | -40<br>to<br>+85°C | 0<br>to<br>70°C | -40<br>to<br>+85°C | 0<br>to<br>70°C | -40<br>to<br>+85°C |      |
| Operating<br>Current       | Device Selected;<br>All other inputs<br>$\geq V_{IH}$ or $\leq V_{IL}$<br>Output open | $I_{DD}$<br>Pipeline        | 335             | 345               | 310             | 320                | 275             | 285                | 250             | 260                | 190             | 200                | mA   |
|                            |                                                                                       | $I_{DD}$<br>Flow<br>Through | 210             | 220               | 190             | 200                | 190             | 200                | 140             | 150                | 140             | 150                | mA   |
| Standby<br>Current         | $ZZ \geq V_{DD} - 0.2 V$                                                              | $I_{SB}$<br>Pipeline        | 20              | 30                | 30              | 40                 | 30              | 40                 | 30              | 40                 | 30              | 40                 | mA   |
|                            |                                                                                       | $I_{SB}$<br>Flow<br>Through | 20              | 30                | 30              | 40                 | 30              | 40                 | 30              | 40                 | 30              | 40                 | mA   |
| Deselect<br>Supply Current | Device Deselected;<br>All other inputs<br>$\geq V_{IH}$ OR $\leq V_{IL}$              | $I_{DD}$<br>Pipeline        | 55              | 65                | 110             | 120                | 105             | 115                | 100             | 110                | 80              | 90                 | mA   |
|                            |                                                                                       | $I_{DD}$<br>Flow<br>Through | 40              | 50                | 80              | 90                 | 80              | 90                 | 65              | 75                 | 65              | 75                 | mA   |

**Not Recommended for New Design - Discontinued Product**

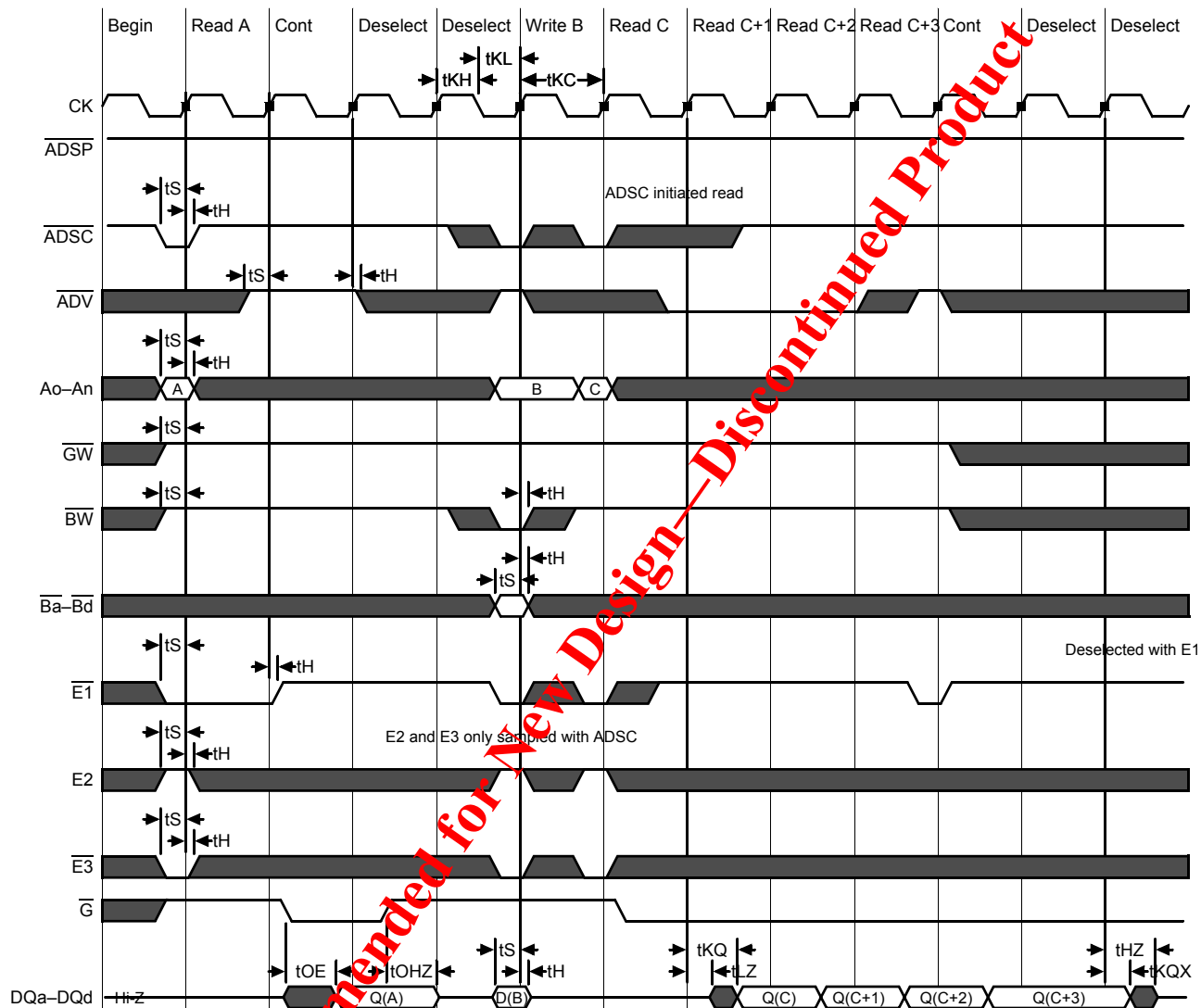
## AC Electrical Characteristics

|              | Parameter                                  | Symbol                         | -180 |     | -166 |     | -150 |      | -133 |      | -100 |      | Unit |
|--------------|--------------------------------------------|--------------------------------|------|-----|------|-----|------|------|------|------|------|------|------|
|              |                                            |                                | Min  | Max | Min  | Max | Min  | Max  | Min  | Max  | Min  | Max  |      |
| Pipeline     | Clock Cycle Time                           | t <sub>KC</sub>                | 5.5  | —   | 6.0  | —   | 6.7  | —    | 7.5  | —    | 10   | —    | ns   |
|              | Clock to Output Valid                      | t <sub>KQ</sub>                | —    | 3.2 | —    | 3.5 | —    | 3.8  | —    | —    | 4.5  | —    | ns   |
|              | Clock to Output Invalid                    | t <sub>KQX</sub>               | 1.5  | —   | 1.5  | —   | 1.5  | —    | 1.5  | —    | 1.5  | —    | ns   |
|              | Clock to Output in Low-Z                   | t <sub>LZ</sub> <sup>1</sup>   | 1.5  | —   | 1.5  | —   | 1.5  | —    | 1.5  | —    | 1.5  | —    | ns   |
|              | Clock to Match Valid                       | t <sub>KM</sub>                | —    | 3.2 | —    | 3.5 | —    | 3.8  | —    | 4    | —    | 4.5  | ns   |
|              | Clock to Match Invalid                     | t <sub>KMX</sub>               | 1.5  | —   | 1.5  | —   | 1.5  | —    | 1.5  | —    | 1.5  | —    | ns   |
|              | Clock to Match in Low-Z                    | t <sub>MLZ</sub> <sup>1</sup>  | 1.5  | —   | 1.5  | —   | 1.5  | —    | 1.5  | —    | 1.5  | —    | ns   |
| Flow Through | Clock Cycle Time                           | t <sub>KC</sub>                | 9.1  | —   | 10.0 | —   | 10.0 | —    | 15.0 | —    | 15.0 | —    | ns   |
|              | Clock to Output Valid                      | t <sub>KQ</sub>                | —    | 8.0 | —    | 8.5 | —    | 10.0 | —    | 11.0 | —    | 12.0 | ns   |
|              | Clock to Output Invalid                    | t <sub>KQX</sub>               | 3.0  | —   | 3.0  | —   | 3.0  | —    | 3.0  | —    | 3.0  | —    | ns   |
|              | Clock to Output in Low-Z                   | t <sub>LZ</sub> <sup>1</sup>   | 3.0  | —   | 3.0  | —   | 3.0  | —    | 3.0  | —    | 3.0  | —    | ns   |
|              | Clock to Match Valid                       | t <sub>KM</sub>                | —    | 8.5 | —    | 8.5 | —    | 10.0 | —    | 11.0 | —    | 12.0 | ns   |
|              | Clock to Match Invalid                     | t <sub>KMX</sub>               | 3.0  | —   | 3.0  | —   | 3.0  | —    | 3.0  | —    | 3.0  | —    | ns   |
|              | Clock to Match in Low-Z                    | t <sub>MLZ</sub> <sup>1</sup>  | 3.0  | —   | 3.0  | —   | 3.0  | —    | 3.0  | —    | 3.0  | —    | ns   |
|              | Clock HIGH Time                            | t <sub>KH</sub>                | 1.3  | —   | 1.3  | —   | 1.5  | —    | 1.7  | —    | 2    | —    | ns   |
|              | Clock LOW Time                             | t <sub>KL</sub>                | 1.5  | —   | 1.5  | —   | 1.7  | —    | 1.9  | —    | 2.2  | —    | ns   |
|              | Clock to Output in High-Z                  | t <sub>HZ</sub> <sup>1</sup>   | 1.5  | 3.2 | 1.5  | 3.5 | 1.5  | 3.8  | 1.5  | 4    | 1.5  | 5    | ns   |
|              | $\overline{\text{OE}}$ to Output Valid     | t <sub>OE</sub>                | —    | 3.2 | —    | 3.5 | —    | 3.8  | —    | 4    | —    | 5    | ns   |
|              | $\overline{\text{OE}}$ to output in Low-Z  | t <sub>OLZ</sub> <sup>1</sup>  | 0    | —   | 0    | —   | 0    | —    | 0    | —    | 0    | —    | ns   |
|              | $\overline{\text{OE}}$ to output in High-Z | t <sub>OHZ</sub> <sup>1</sup>  | —    | 3.2 | —    | 3.5 | —    | 3.8  | —    | 4    | —    | 5    | ns   |
|              | $\overline{\text{MOE}}$ to Match Valid     | t <sub>MOE</sub>               | —    | 3.2 | —    | 3.5 | —    | 3.8  | —    | 4    | —    | 5    | ns   |
|              | $\overline{\text{MOE}}$ to Match in Low-Z  | t <sub>MOLZ</sub> <sup>1</sup> | 0    | —   | 0    | —   | 0    | —    | 0    | —    | 0    | —    | ns   |
|              | $\overline{\text{MOE}}$ to Match in High-Z | t <sub>MOHZ</sub> <sup>1</sup> | —    | 3.2 | —    | 3.5 | —    | 3.8  | —    | 4    | —    | 5    | ns   |
|              | Setup time                                 | t <sub>S</sub>                 | 1.5  | —   | 1.5  | —   | 1.5  | —    | 2.0  | —    | 2.0  | —    | ns   |
|              | Hold time                                  | t <sub>H</sub>                 | 0.5  | —   | 0.5  | —   | 0.5  | —    | 0.5  | —    | 0.5  | —    | ns   |
|              | ZZ setup time                              | t <sub>ZZS</sub> <sup>2</sup>  | 5    | —   | 5    | —   | 5    | —    | 5    | —    | 5    | —    | ns   |
|              | ZZ hold time                               | t <sub>ZZH</sub> <sup>2</sup>  | 1    | —   | 1    | —   | 1    | —    | 1    | —    | 1    | —    | ns   |
|              | ZZ recovery                                | t <sub>ZZR</sub>               | 20   | —   | 20   | —   | 20   | —    | 20   | —    | 20   | —    | ns   |

### Notes:

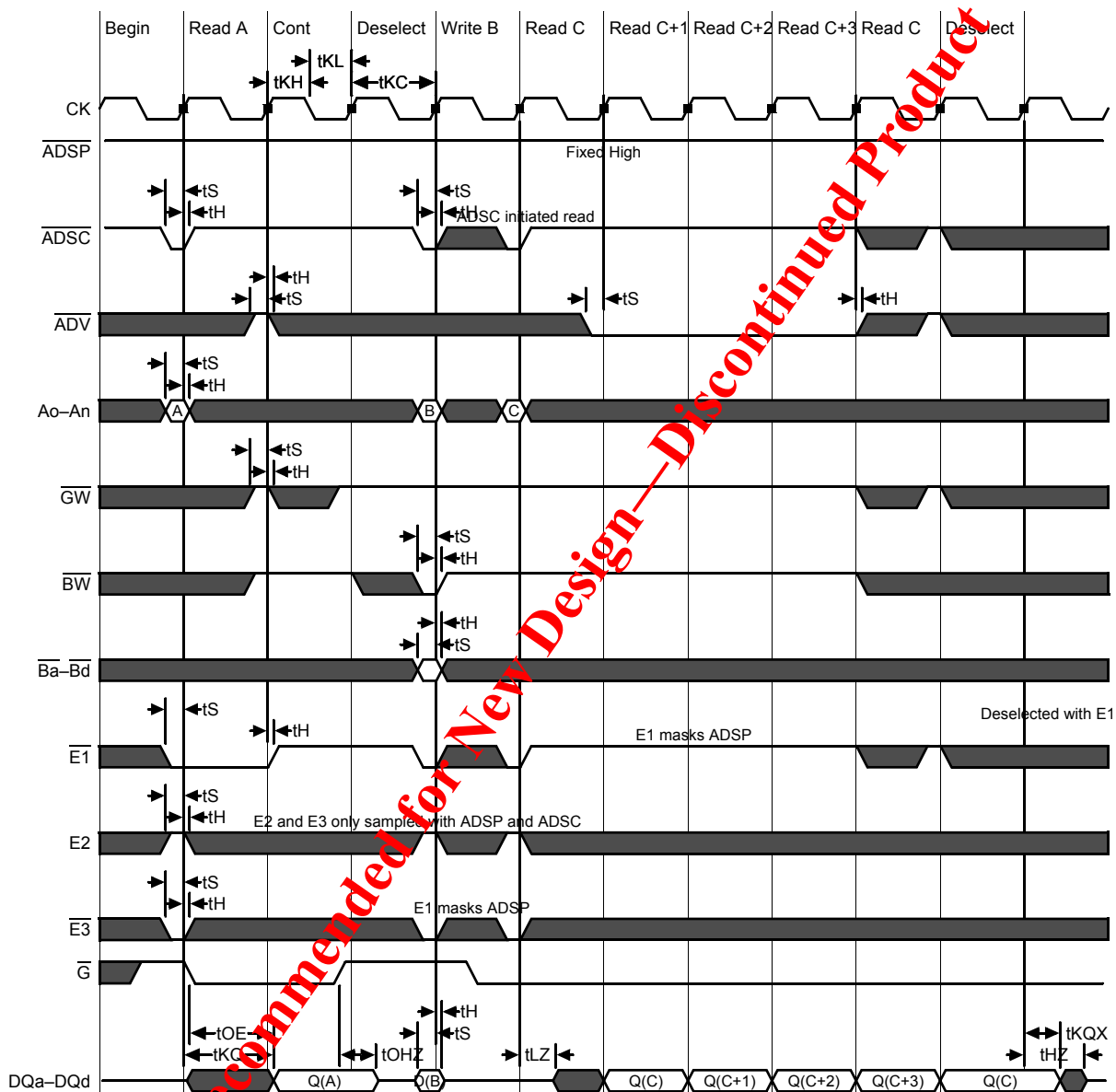
- These parameters are sampled and are not 100% tested
- ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

# Pipeline Mode Timing

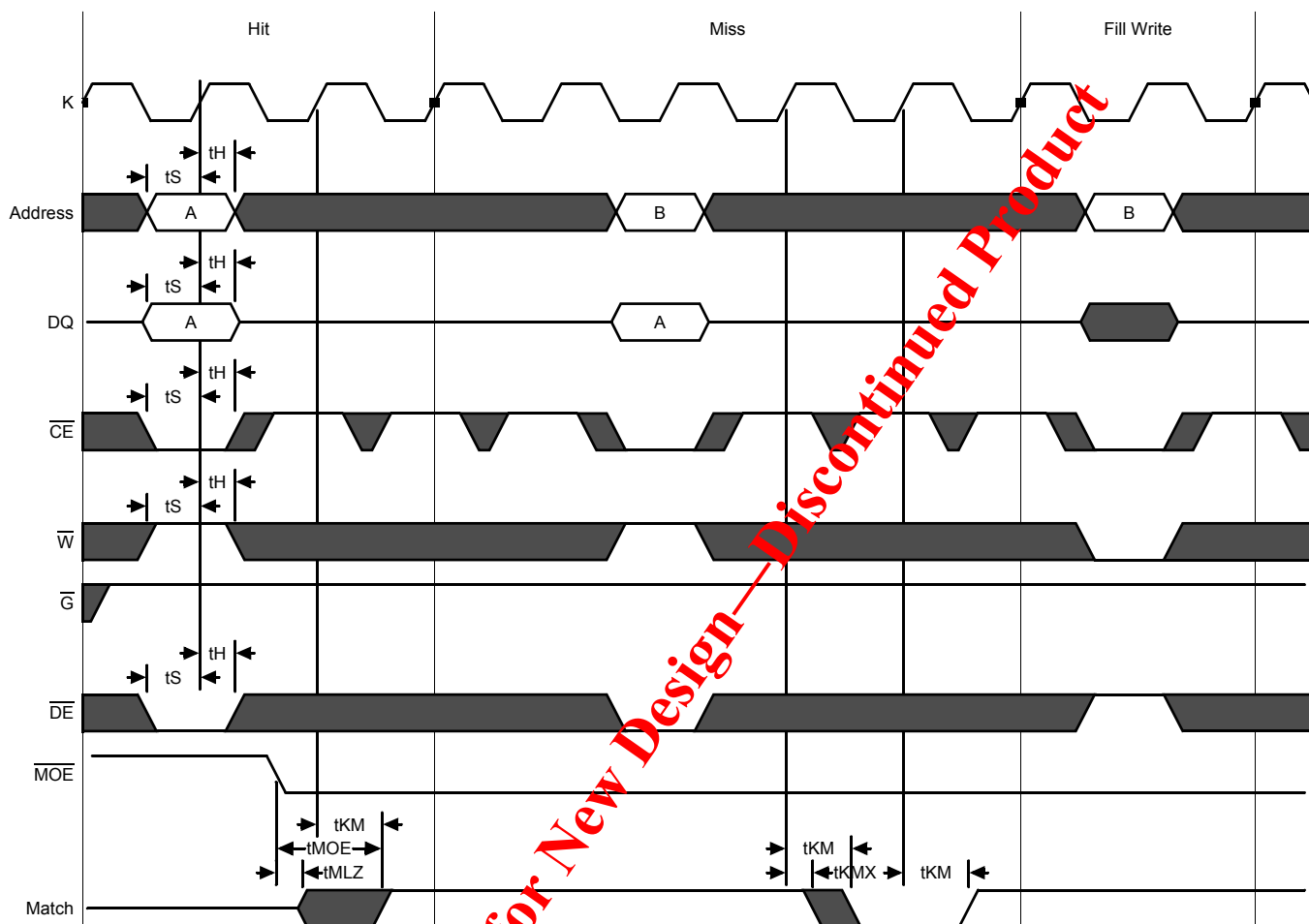


**Not Recommended for New Design - Discontinued Product**

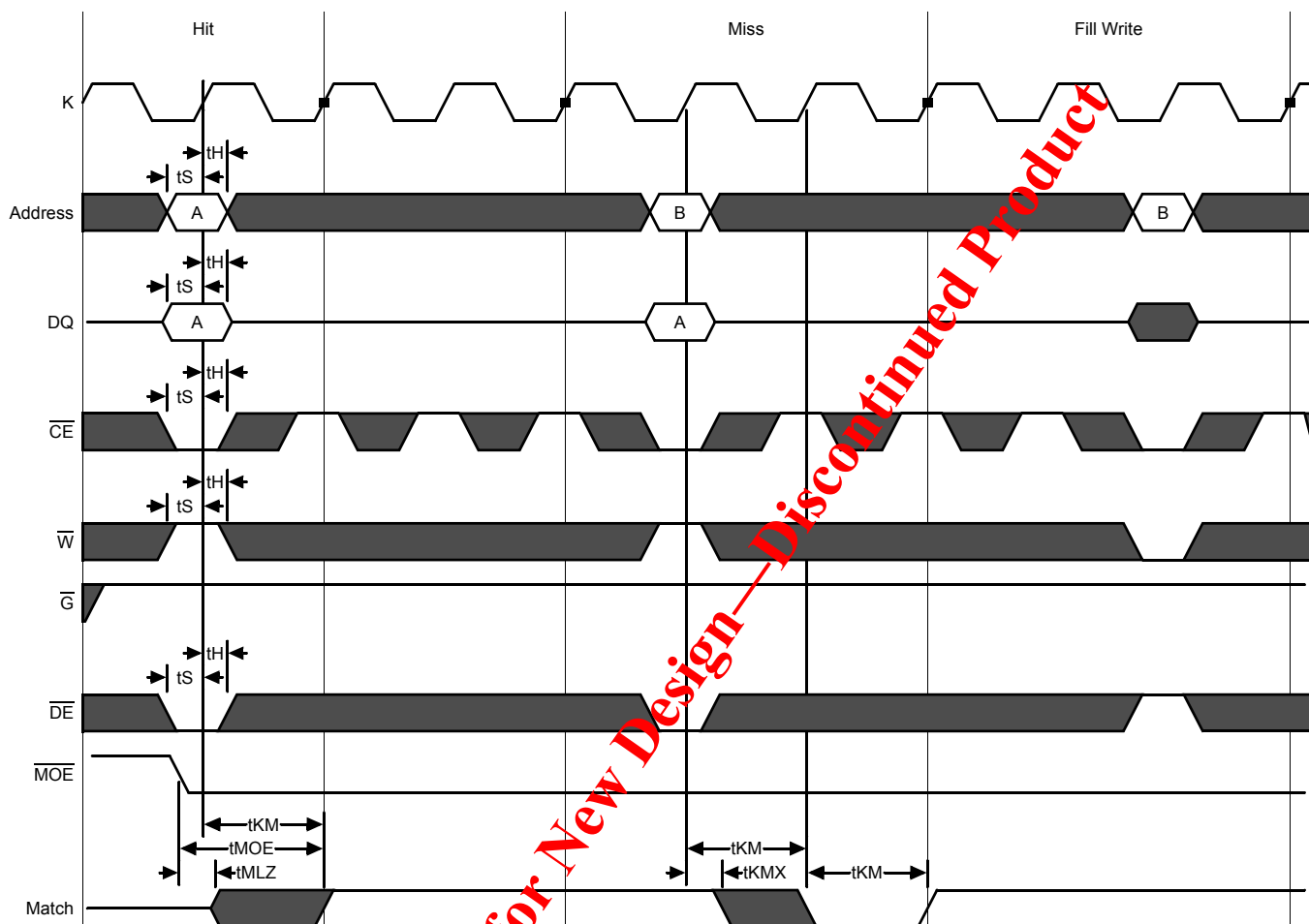
# Flow Through Mode Timing



# Pipeline Compare Fill Write Cycle



# Flow Through Compare Fill Write Cycle



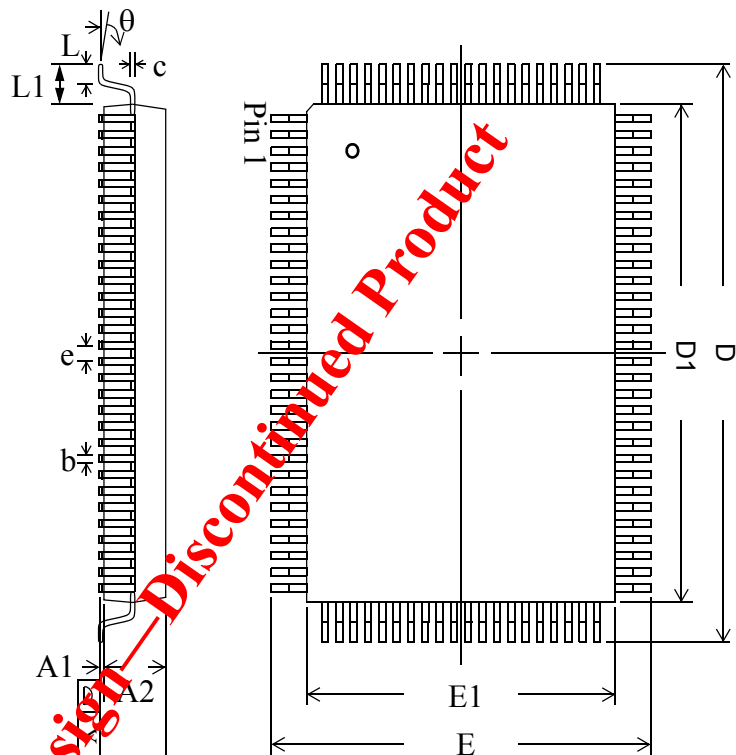
**Not Recommended for New Design—Discontinued Product**

## TQFP Package Drawing (Package T)

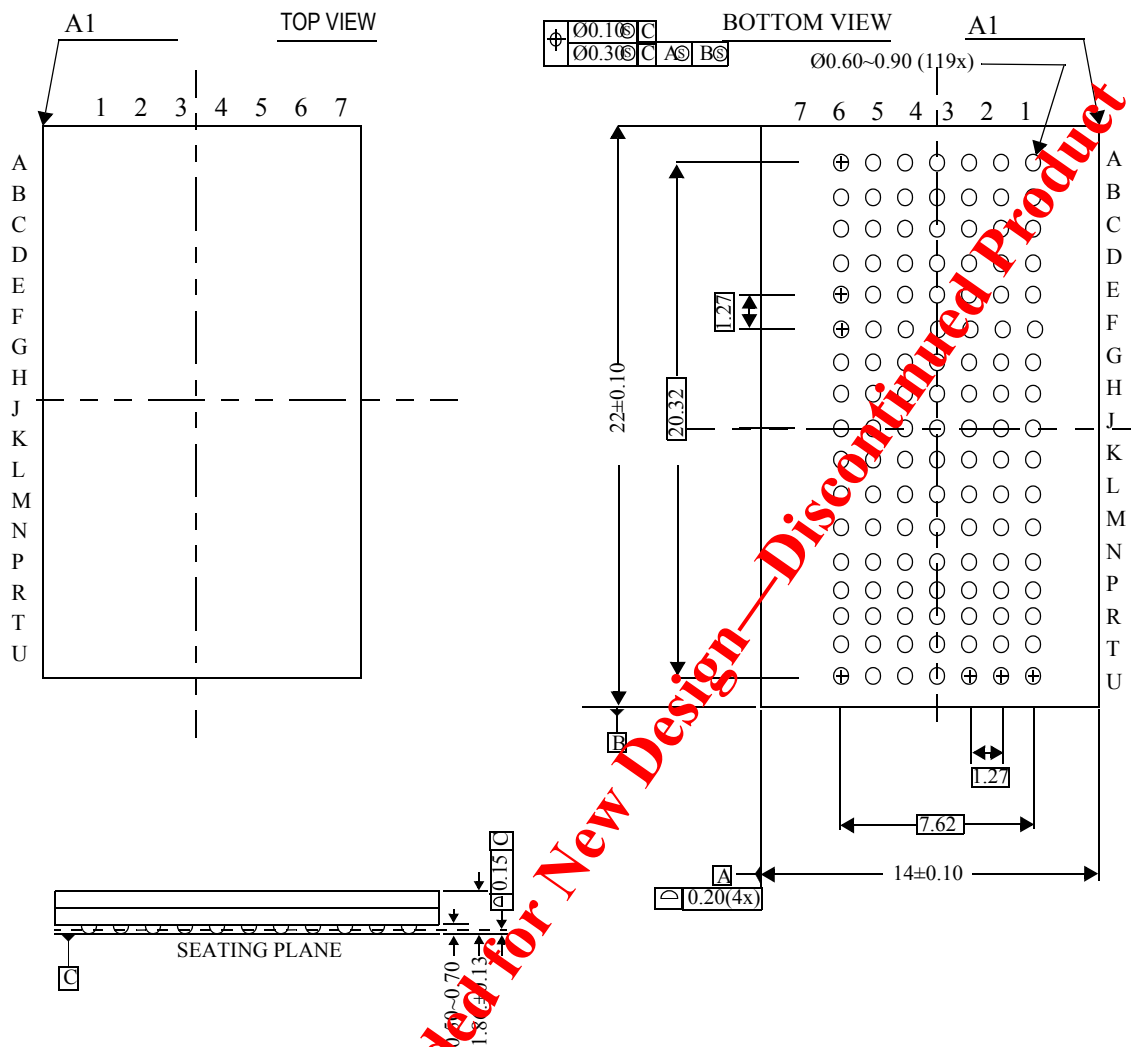
| Symbol   | Description        | Min. | Nom. | Max  |
|----------|--------------------|------|------|------|
| A1       | Standoff           | 0.05 | 0.10 | 0.15 |
| A2       | Body Thickness     | 1.35 | 1.40 | 1.45 |
| b        | Lead Width         | 0.20 | 0.30 | 0.40 |
| c        | Lead Thickness     | 0.09 | —    | 0.20 |
| D        | Terminal Dimension | 21.9 | 22.0 | 22.1 |
| D1       | Package Body       | 19.9 | 20.0 | 20.1 |
| E        | Terminal Dimension | 15.9 | 16.0 | 16.1 |
| E1       | Package Body       | 13.9 | 14.0 | 14.1 |
| e        | Lead Pitch         | —    | 0.65 | —    |
| L        | Foot Length        | 0.45 | 0.60 | 0.75 |
| L1       | Lead Length        | —    | 1.00 | —    |
| Y        | Coplanarity        |      |      | 0.10 |
| $\theta$ | Lead Angle         | 0°   | —    | 7°   |

## Notes:

1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.



Package Dimensions—119-Bump FPBGA (Package GB (MCM), Variation 2)



**Ordering Information**

| Org       | Part Number <sup>1</sup> | Type                      | Package             | Speed <sup>2</sup><br>(MHz/ns) | T <sub>A</sub> <sup>3</sup> |
|-----------|--------------------------|---------------------------|---------------------|--------------------------------|-----------------------------|
| 256K x 18 | GS841E18AT-180           | DCD Pipeline/Flow Through | TQFP                | 180/8                          | C                           |
| 256K x 18 | GS841E18AT-166           | DCD Pipeline/Flow Through | TQFP                | 166/8.5                        | C                           |
| 256K x 18 | GS841E18AT-150           | DCD Pipeline/Flow Through | TQFP                | 150/10                         | C                           |
| 256K x 18 | GS841E18AT-133           | DCD Pipeline/Flow Through | TQFP                | 133/11                         | C                           |
| 256K x 18 | GS841E18AT-100           | DCD Pipeline/Flow Through | TQFP                | 100/12                         | C                           |
| 256K x 18 | GS841E18AT-180I          | DCD Pipeline/Flow Through | TQFP                | 180/8                          | I                           |
| 256K x 18 | GS841E18AT-166I          | DCD Pipeline/Flow Through | TQFP                | 166/8.5                        | I                           |
| 256K x 18 | GS841E18AT-150I          | DCD Pipeline/Flow Through | TQFP                | 150/10                         | I                           |
| 256K x 18 | GS841E18AT-133I          | DCD Pipeline/Flow Through | TQFP                | 133/11                         | I                           |
| 256K x 18 | GS841E18AT-100I          | DCD Pipeline/Flow Through | TQFP                | 100/12                         | I                           |
| 256K x 18 | GS841E18AGT-180          | DCD Pipeline/Flow Through | RoHS-compliant TQFP | 180/8                          | C                           |
| 256K x 18 | GS841E18AGT-166          | DCD Pipeline/Flow Through | RoHS-compliant TQFP | 166/8.5                        | C                           |
| 256K x 18 | GS841E18AGT-150          | DCD Pipeline/Flow Through | RoHS-compliant TQFP | 150/10                         | C                           |
| 256K x 18 | GS841E18AGT-133          | DCD Pipeline/Flow Through | RoHS-compliant TQFP | 133/11                         | C                           |
| 256K x 18 | GS841E18AGT-100          | DCD Pipeline/Flow Through | RoHS-compliant TQFP | 100/12                         | C                           |
| 256K x 18 | GS841E18AGT-180I         | DCD Pipeline/Flow Through | RoHS-compliant TQFP | 180/8                          | I                           |
| 256K x 18 | GS841E18AGT-166I         | DCD Pipeline/Flow Through | RoHS-compliant TQFP | 166/8.5                        | I                           |
| 256K x 18 | GS841E18AGT-150I         | DCD Pipeline/Flow Through | RoHS-compliant TQFP | 150/10                         | I                           |
| 256K x 18 | GS841E18AGT-133I         | DCD Pipeline/Flow Through | RoHS-compliant TQFP | 133/11                         | I                           |
| 256K x 18 | GS841E18AGT-100I         | DCD Pipeline/Flow Through | RoHS-compliant TQFP | 100/12                         | I                           |
| 256K x 18 | GS841E18AB-180           | DCD Pipeline/Flow Through | 119 BGA (var. 2)    | 180/8                          | C                           |
| 256K x 18 | GS841E18AB-166           | DCD Pipeline/Flow Through | 119 BGA (var. 2)    | 166/8.5                        | C                           |
| 256K x 18 | GS841E18AB-150           | DCD Pipeline/Flow Through | 119 BGA (var. 2)    | 150/10                         | C                           |
| 256K x 18 | GS841E18AB-133           | DCD Pipeline/Flow Through | 119 BGA (var. 2)    | 133/11                         | C                           |
| 256K x 18 | GS841E18AB-100           | DCD Pipeline/Flow Through | 119 BGA (var. 2)    | 100/12                         | C                           |
| 256K x 18 | GS841E18AB-180I          | DCD Pipeline/Flow Through | 119 BGA (var. 2)    | 180/8                          | I                           |
| 256K x 18 | GS841E18AB-166I          | DCD Pipeline/Flow Through | 119 BGA (var. 2)    | 166/8.5                        | I                           |
| 256K x 18 | GS841E18AB-150I          | DCD Pipeline/Flow Through | 119 BGA (var. 2)    | 150/10                         | I                           |
| 256K x 18 | GS841E18AB-133I          | DCD Pipeline/Flow Through | 119 BGA (var. 2)    | 133/11                         | I                           |
| 256K x 18 | GS841E18AB-100I          | DCD Pipeline/Flow Through | 119 BGA (var. 2)    | 100/12                         | I                           |

**Notes:**

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS841E18AT-166T.
- The speed column indicates the cycle frequency (Mhz) of the device in Pipelined mode and the latency (ns) in Flow Through mode. Each device is Pipeline / Flow through mode selectable by the user.
- T<sub>A</sub> = C = Commercial Temperature Range. T<sub>A</sub> = I = Industrial Temperature Range.
- GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site for a complete listing of current offerings.

**Ordering Information**

| Org       | Part Number <sup>1</sup> | Type                      | Package                         | Speed <sup>2</sup><br>(MHz/ns) | T <sub>A</sub> <sup>3</sup> |
|-----------|--------------------------|---------------------------|---------------------------------|--------------------------------|-----------------------------|
| 256K x 18 | GS841E18AGB-180          | DCD Pipeline/Flow Through | RoHS-compliant 119 BGA (var. 2) | 180/8                          | C                           |
| 256K x 18 | GS841E18AGB-166          | DCD Pipeline/Flow Through | RoHS-compliant 119 BGA (var. 2) | 166/8.5                        | C                           |
| 256K x 18 | GS841E18AGB-150          | DCD Pipeline/Flow Through | RoHS-compliant 119 BGA (var. 2) | 150/10                         | C                           |
| 256K x 18 | GS841E18AGB-133          | DCD Pipeline/Flow Through | RoHS-compliant 119 BGA (var. 2) | 133/11                         | C                           |
| 256K x 18 | GS841E18AGB-100          | DCD Pipeline/Flow Through | RoHS-compliant 119 BGA (var. 2) | 100/12                         | C                           |
| 256K x 18 | GS841E18AGB-180I         | DCD Pipeline/Flow Through | RoHS-compliant 119 BGA (var. 2) | 180/8                          | I                           |
| 256K x 18 | GS841E18AGB-166I         | DCD Pipeline/Flow Through | RoHS-compliant 119 BGA (var. 2) | 166/8.5                        | I                           |
| 256K x 18 | GS841E18AGB-150I         | DCD Pipeline/Flow Through | RoHS-compliant 119 BGA (var. 2) | 150/10                         | I                           |
| 256K x 18 | GS841E18AGB-133I         | DCD Pipeline/Flow Through | RoHS-compliant 119 BGA (var. 2) | 133/11                         | I                           |
| 256K x 18 | GS841E18AGB-100I         | DCD Pipeline/Flow Through | RoHS-compliant 119 BGA (var. 2) | 100/12                         | I                           |

**Notes:**

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS841E18AT-166T.
- The speed column indicates the cycle frequency (Mhz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline / Flow through mode selectable by the user.
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- GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site for a complete listing of current offerings.

**4Mb Synchronous Tag RAM Datasheet Revision History**

| Rev. Code: Old;New                  | Types of Changes<br>Format or Content | Page /Revisions;Reason                                                                                                                                                                                                                                                          |
|-------------------------------------|---------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GS841E18A_r1                        |                                       | • Creation of new datasheet                                                                                                                                                                                                                                                     |
| GS841E18A_r1;<br>GS841E18A_r1_01    | Content                               | • Moved TCK from U6 (incorrect placement) to U4 (correct placement) on BGA<br>• Changed U6 to NC                                                                                                                                                                                |
| GS841E18A_r1_01;<br>GS841E18A_r1_02 | Format/Content                        | • Updated format<br>• Added 180 MHz speed bin<br>• Updated timing diagrams<br>• Updated mechanical drawings<br>• Added Pb-Free info for TQFP                                                                                                                                    |
| GS841E18A_r1_02;<br>GS841E18A_r1_03 | Content                               | • Added Pipeline Compare Fill Write Cycle and Flow Through Compare Fill Write Cycle timing diagrams<br>• (Rev1.03a: Added RoHS-compliant information for BGA)<br>• Rev1.03b: updated coplanarity for 119 BGA mechanical, removed status column from Ordering Information table. |