

### DESCRIPTION:

The DPE8M624 is a high-performance Electrically Erasable and Programmable Read Only Memory (EEPROM) module and may be organized as 64K X 16 or 128K X 8.

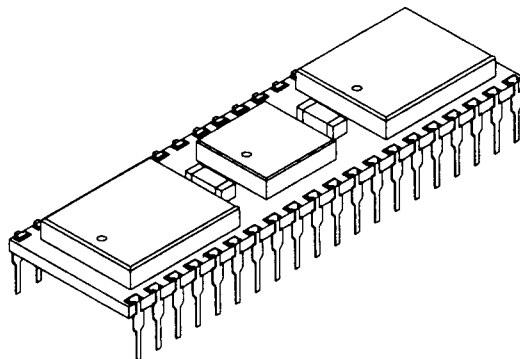
The module is built with four low-power CMOS 32K X 8 EEPROMs and one high speed 139 decoder. The decoder uses A15 to select between the upper and lower bank of memory. The  $\overline{UB}$  (Upper Byte Enable) and  $\overline{LB}$  (Lower Byte Enable) inputs allow control of the individual devices connected to I/O0 - I/O7 and I/O8 - I/O15. The DPE8M624 is ideally suited for those computer systems having 16-bit architectures.

The DPE8M624 contains a 64-BW\* page register to allow writing of up to 64 BWs simultaneously. During a write cycle, the address and 1 to 64 BWs of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the module will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by  $\overline{DATA}$  Polling of the most significant data bit in each byte. Once the end of a write cycle has been detected, a new access for a read or write can begin.

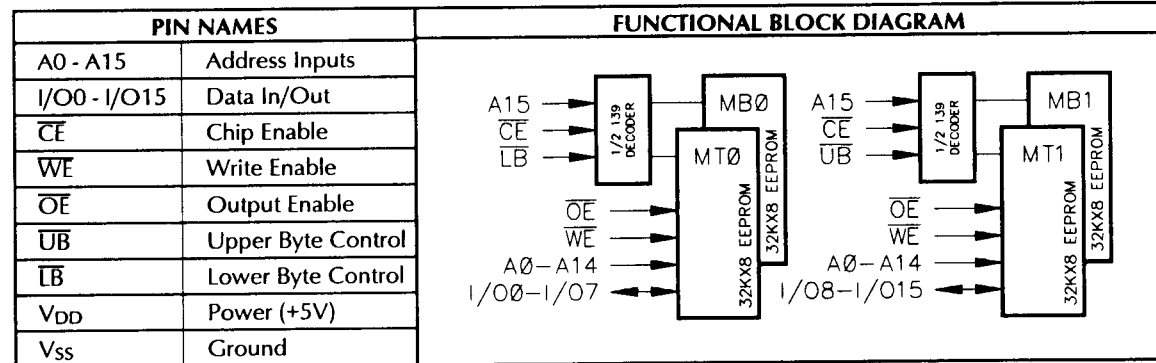
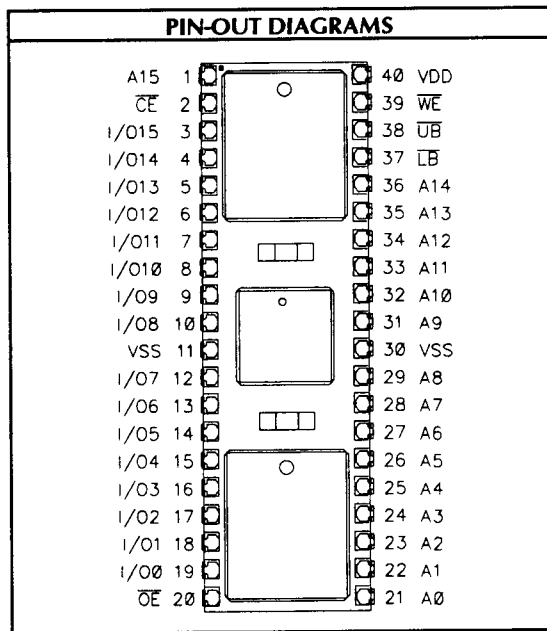
### FEATURES:

- Fast Access Times: 90, 120, 150, 170, 200, 250ns
- Automatic Page Write Operation
  - Internal Address and Data Latches
  - Internal Control Timer
- Fast Write Cycle Times
  - Page Write Cycle Time: 10ms maximum
  - 1 to 64 BW\* Page Write Operation
- $\overline{DATA}$  Polling for END of Write Detection
- High Reliability CMOS Technology
  - Endurance:  $10^4$  Cycles
  - Data Retention: 10 years
- Single +5V Power Supply,  $\pm 10\%$  Tolerance
- CMOS and TTL Compatible Inputs and Outputs
- Available with All Semiconductor Components
  - Compliant to MIL-STD-883; Class B
  - 40-Pin, 600 Mil Wide Ceramic DIP

\* Byte or Word (BW)



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TRUTH TABLE								
Mode	CE	LB	UB	WE	OE	I/O0 - I/O7	I/O8 - I/O15	Supply Current
Not Selected	H	X	X	X	X	HIGH-Z	HIGH-Z	Standby
Not Selected	X	H	H	X	X	HIGH-Z	HIGH-Z	Standby
DOUT Disable	L	L	L	H	H	HIGH-Z	HIGH-Z	Active
Read Lower Block	L	L	H	H	L	DOUT	HIGH-Z	Active
Read Upper Block	L	H	L	H	L	HIGH-Z	DOUT	Active
Read All	L	L	L	H	L	DOUT	DOUT	Active
Write Lower Block	L	L	H	L	X	DIN	HIGH-Z	Active
Write Upper Block	L	H	L	L	X	HIGH-Z	DIN	Active
Write All	L	L	L	L	X	DIN	DIN	Active

H = HIGH, L = LOW, X = Don't Care.

RECOMMENDED OPERATING RANGE <sup>1</sup>					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input HIGH Voltage	2.2		V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input LOW Voltage	-0.1 <sup>2</sup>		0.8	V

CAPACITANCE <sup>4</sup> : T <sub>A</sub> = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
CADR	Address Input	60	pF	V <sub>IN</sub> =0V
CCE	Chip Enable	25		
CWE	Write Enable	60		
COE	Output Enable	60		
C <sub>I/O</sub>	Data Input/Output	45		

ABSOLUTE MAXIMUM RATINGS <sup>3</sup>			
Symbol	Parameter	Value	Unit
T <sub>STC</sub>	Storage Temperature	-65 to +150	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
V <sub>DD</sub>	Supply Voltage <sup>1</sup>	-0.3 to +6.25	V
V <sub>I/O</sub>	Input/Output Voltage <sup>1</sup>	-0.3 <sup>2</sup> to +6.25	V

DC OPERATING CHARACTERISTICS: Over the operating ranges.							
Symbol	Characteristics	Test Conditions	64K X 16		128K X 8		Unit
			Min.	Max.	Min.	Max.	
I <sub>CC</sub>	Operating Supply Current	CE = OE = V <sub>IL</sub> , all I/O = 0mA f = t <sub>rc</sub> Min.		170		90	mA
I <sub>S81</sub>	V <sub>DD</sub> Current Standby (TTL)	CE = V <sub>IH</sub>		12		12	mA
I <sub>S82</sub>	V <sub>DD</sub> Current Standby (CMOS)	CE = V <sub>DD</sub> -0.3Vdc		1.4		1.4	mA
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = V <sub>DD</sub> Max.	-20	20	-20	20	μA
I <sub>OL</sub>	Output Leakage Current	V <sub>OUT</sub> = V <sub>DD</sub> Max.	-10	10	-20	20	μA
V <sub>IL</sub>	Input Voltage Low		-0.1	0.8	-0.1	0.8	V
V <sub>IH</sub>	Input Voltage High		2.0	V <sub>DD</sub> +0.3	2.0	V <sub>DD</sub> +0.3	V
V <sub>OL</sub>	Output Voltage Low	I <sub>OUT</sub> = 2.1mA		0.45		0.45	V
V <sub>OH</sub>	Output Voltage High	I <sub>OUT</sub> = -400μA	2.4		2.4		V

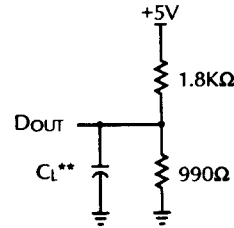
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

\* Transition between 0.8V and 2.2V.

OUTPUT LOAD		
Float	C <sub>L</sub>	Parameters Measured
1	100 pF	except t <sub>DF</sub>
2	5 pF	t <sub>DF</sub>

Figure 1. Output Load

\*\* Including Probe and Jig Capacitance.



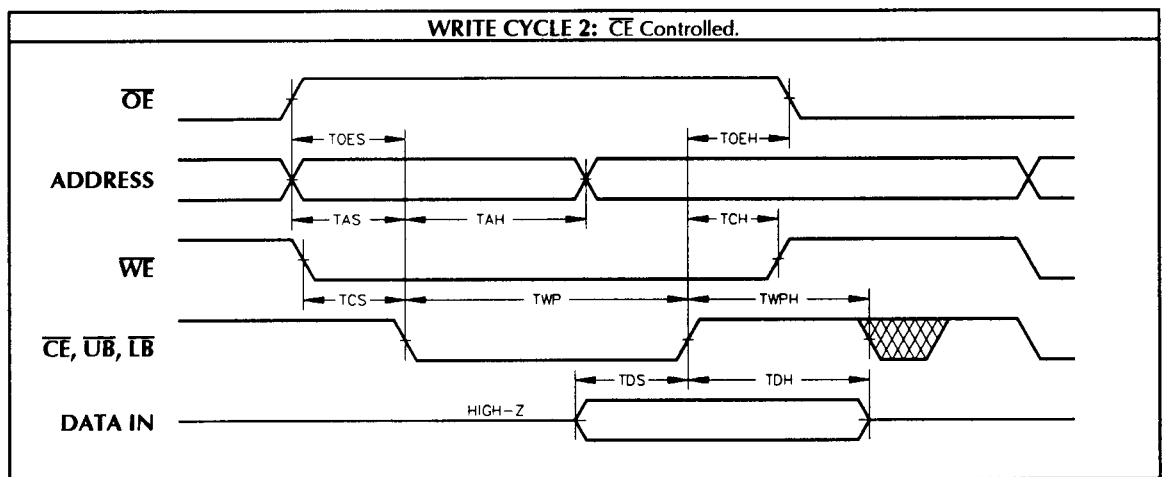
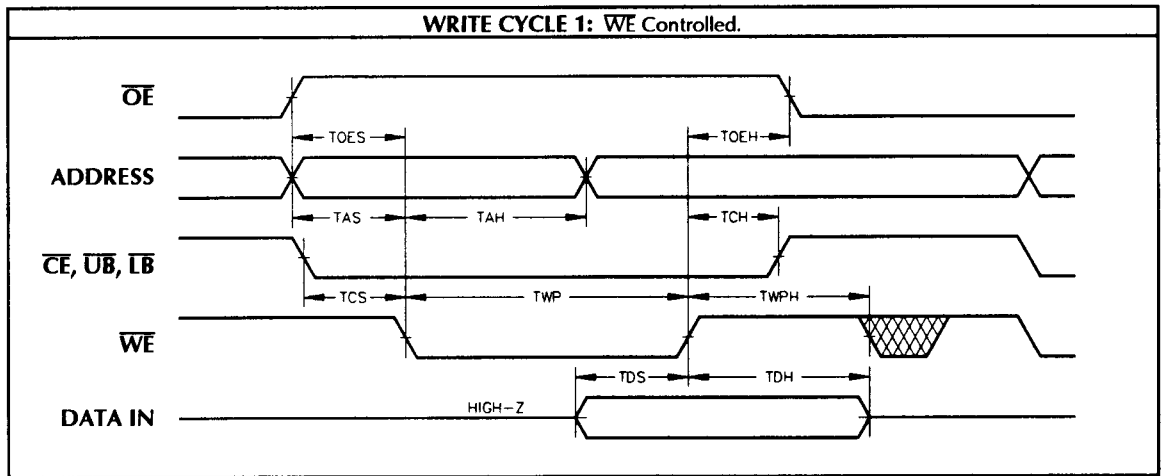
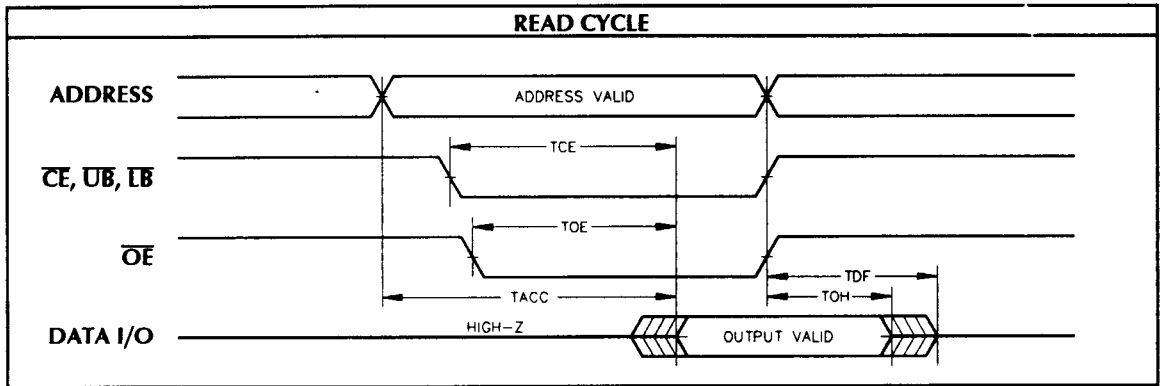
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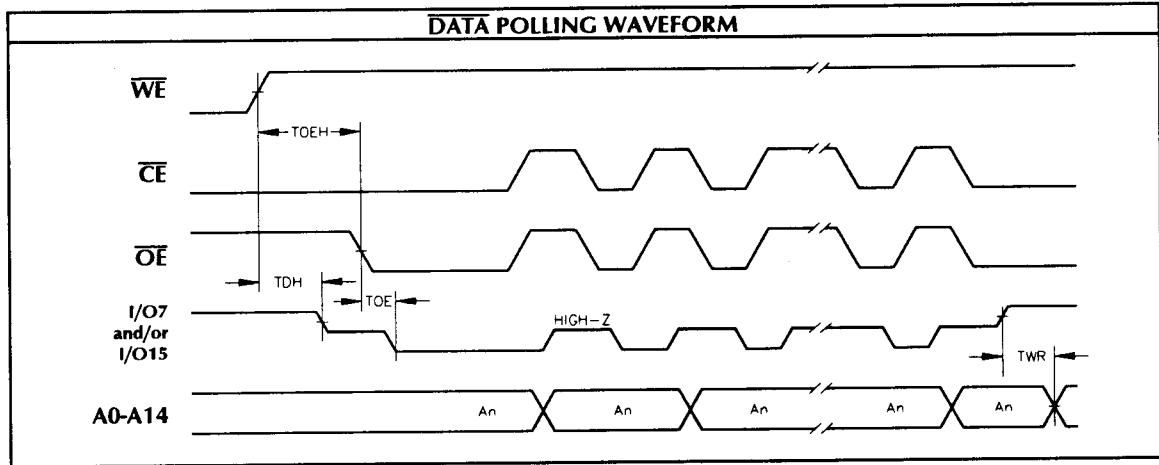
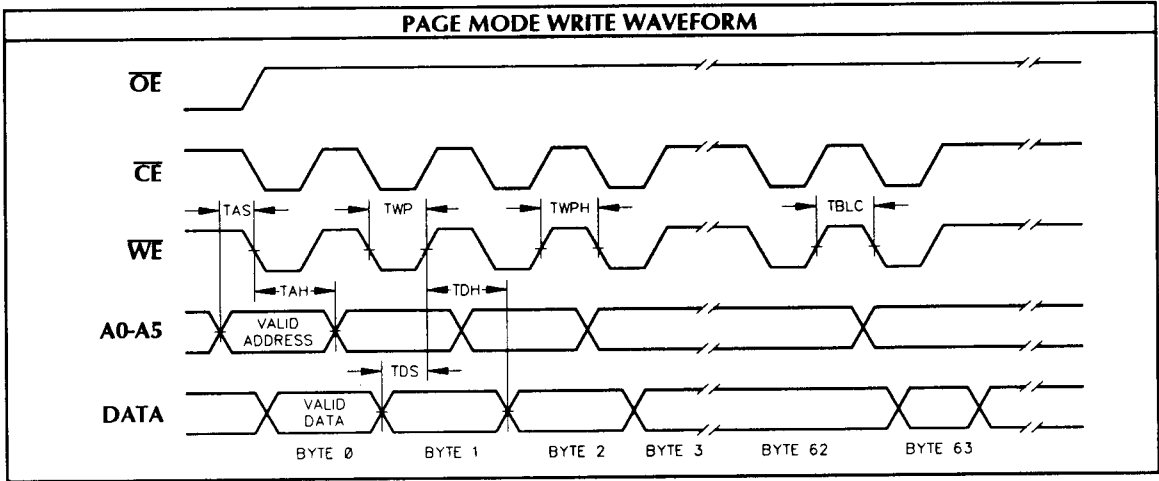
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges <sup>6,7</sup>									
No.	Symbol	Parameter	-90		-120		-150		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	t <sub>ACC</sub>	Address to Output Valid		90		120		150	ns
2	t <sub>CE</sub>	Chip Enable to Output Valid		90		120		150	ns
3	t <sub>OE</sub>	Output Enable to Output Valid		35		45		50	ns
4	t <sub>DF</sub>	Chip Enable or Output Enable to Output Float <sup>4</sup>		50		60		65	ns
5	t <sub>OH</sub>	Output Hold from Chip Enable, Output Enable, or Address, Whichever Occurs First	0		0		0		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges <sup>6,7</sup>									
No.	Symbol	Parameter	-170		-200		-250		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	t <sub>ACC</sub>	Address to Output Valid		170		200		250	ns
2	t <sub>CE</sub>	Chip Enable to Output Valid		170		200		250	ns
3	t <sub>OE</sub>	Output Enable to Output Valid		70		75		80	ns
4	t <sub>DF</sub>	Chip Enable or Output Enable to Output Float <sup>4</sup>		70		70		75	ns
5	t <sub>OH</sub>	Output Hold from Chip Enable, Output Enable, or Address, Whichever Occurs First	0		0		0		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges <sup>6,7</sup>						
No.	Symbol	Parameter	MIN.		MAX.	Unit
6	t <sub>WC</sub>	Write Cycle Time			10	ms
7	t <sub>AS</sub>	Address Set-up Time***	20			ns
8	t <sub>AH</sub>	Address Hold Time	100			ns
9	t <sub>CS</sub>	Chip Select Set-up Time	0			ns
10	t <sub>CH</sub>	Chip Select Hold Time	0			ns
11	t <sub>WP</sub>	Write Pulse Width (CE or OE)	150			ns
12	t <sub>DS</sub>	Data Set-up Time	100			ns
13	t <sub>DH</sub>	Data Hold Time	10			ns
14	t <sub>OES</sub>	OE Set-up Time	20			ns
15	t <sub>OEH</sub>	OE Hold Time	20			ns
16	t <sub>WPH</sub>	Write Pulse Width High	100			ns
17	t <sub>BLC</sub>	Byte Load Cycle Time			150	μs

\*\*\* Valid for both Read and Write Cycles.





**DEVICE OPERATION**

**READ:** The DPE8M624 is accessed like a Static RAM. When  $\overline{CE}$  and  $\overline{OE}$  are low and  $\overline{WE}$  is high, the data stored at the memory location determined by address pins is asserted on the outputs. The outputs are put in the high impedance state whenever  $\overline{CE}$  or  $\overline{OE}$  is high. This dual line control gives designers flexibility in preventing bus contention.

**WRITE:** A low pulse on the  $\overline{WE}$  or  $\overline{CE}$  input with  $\overline{CE}$  or  $\overline{WE}$  low (respectively) and  $\overline{OE}$  high initiates a write cycle. The address is latched on the falling edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. The data is latched by the first rising edge of  $\overline{CE}$  or  $\overline{WE}$ . Once a BW\* write has been started it will automatically time itself to completion.

**PAGE WRITE MODE:** The page write operation of the DPE8M624 allows 1 to 64 BWs of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data BW has been loaded into the device, successive BWs may be loaded in the same manner. Each new BW to be written must have its high to low transition on  $\overline{WE}$  (or  $\overline{CE}$ ) within 150µs of the low to high

transition of  $\overline{WE}$  (or  $\overline{CE}$ ) of the preceding BW. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end and the internal programming period will start. A6 to A15 specify the page address. The page address must be valid during each high to low transition of  $\overline{WE}$  (or  $\overline{CE}$ ). A0 to A5 are used to specify which BWs within the page are to be written. The BWs may be loaded in any order and may be changed within the same load period. Only BWs which are specified for writing will be written; unnecessary cycling of other BWs within the page does not occur.

**DATA POLLING:** The DPE8M624 features  $\overline{DATA}$  Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the compliment of the written data on  $I/O7$  and/or  $I/O15$ . Once the the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin.  $\overline{DATA}$  Polling may begin at any time during the write cycle.

\* Byte or Word (BW)

## ORDERING INFORMATION

DP E8M624 - XXX X  
 PREFIX DEVICE TYPE SPEED GRADE

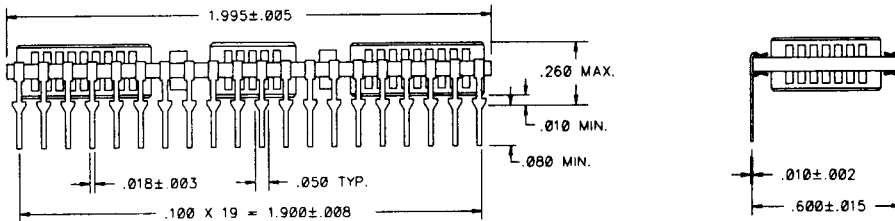
C	COMMERCIAL	0°C to +70°C
I	INDUSTRIAL	-40°C to +85°C
M	MILITARY	-55°C to +125°C
B *	MIL-PROCESSED	-55°C to +125°C

90	90ns
120	120ns
150	150ns
200	200ns
250	250ns

64K X 16 OR 128K X 8 CMOS EEPROM MODULE

\* B grade modules are constructed with 883 devices.

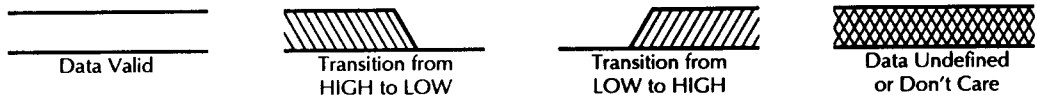
## MECHANICAL DIAGRAM



### NOTES:

1. All voltages are with respect to V<sub>SS</sub>.
2. -1.0V min. for pulse width less than 20ns (V<sub>IL</sub> min. = -0.3V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When  $\overline{OE}$  and  $\overline{CE}$  are LOW and  $\overline{WE}$  is HIGH, I/O pins are in the output state; and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when  $\overline{WE}$  is LOW.

## WAVEFORM KEY



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