



NEC Electronics Inc.

$\mu$ PD424260A/L, 42S4260A/L

262,144 x 16-Bit

Dynamic CMOS RAM

T-46-23-17

**Description**

The  $\mu$ PD424260A/L and  $\mu$ PD42S4260A/L are fast-page dynamic RAMs organized as 262,144 words by 16 bits and designed to operate from a single power supply:

Optional features are power supply voltage (+5 V or +3.3 V) and a new refresh mode called "self-refresh."

$\mu$ PD	Options
424260A	+5 V
424260L	+3.3 V
42S4260A	+5 V; self-refresh mode
42S4260L	+3.3 V; self-refresh mode

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by  $\overline{UCAS}$  and  $\overline{LCAS}$  independent of  $\overline{RAS}$ . After a valid read or read-modify-write cycle, upper or lower byte data is held on the outputs by maintaining  $\overline{UCAS}$  or  $\overline{LCAS}$  low. Data outputs return to high impedance when either  $\overline{UCAS}$  or  $\overline{LCAS}$  goes high. Fast-page read and write cycles can be executed by cycling  $\overline{UCAS}$  or  $\overline{LCAS}$ .

Refreshing may be accomplished by a  $\overline{CAS}$  before  $\overline{RAS}$  refresh cycle (CBR) that internally generates the refresh address.  $\overline{RAS}$ -only refresh cycles will also refresh all memory locations.

The self-refresh mode is entered by holding  $\overline{RAS}$  low for longer than 100  $\mu$ s during a CBR cycle. Detection of this long  $\overline{RAS}$  time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 microamperes. Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

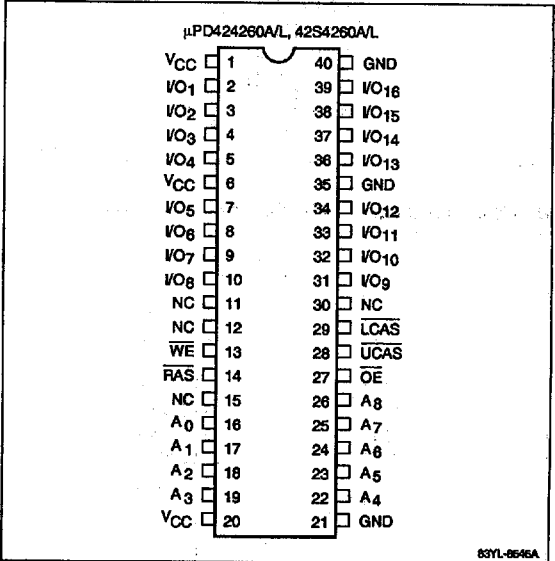
**Features**

- 262,144 by 16-bit organization
- Single power supply (+5-volt or +3.3-volt)
- Self-refresh option (slow internal automatic refresh)
- Fast-page option
- Byte read/write control with  $\overline{UCAS}$  and  $\overline{LCAS}$

- Low power dissipation
- $\overline{CAS}$  before  $\overline{RAS}$  refreshing
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- Multiplexed row and column addresses
- 512 refresh cycles every 8 ms
- 40-pin SOJ, 40-pin ZIP, and 44/40-pin TSOP plastic packaging

**Pin Configurations**

**40-Pin Plastic SOJ**



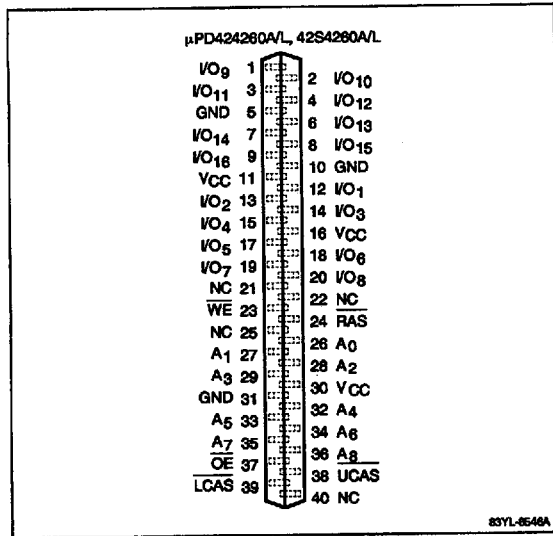
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**μPD424260A/L, 42S4260A/L**

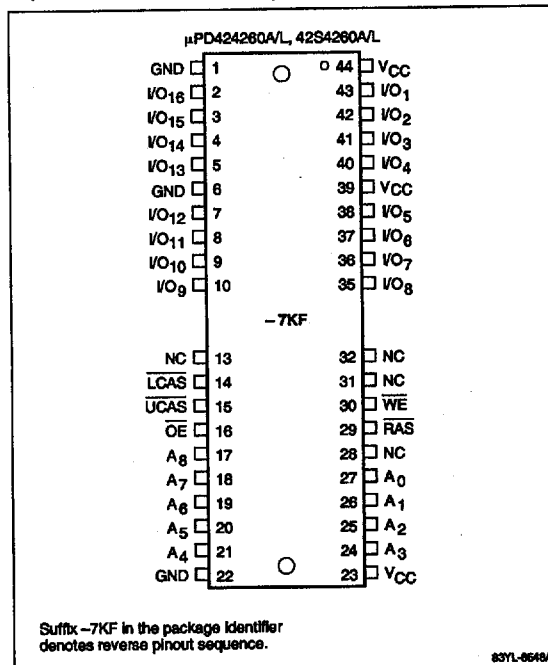


**Pin Configurations (cont)**

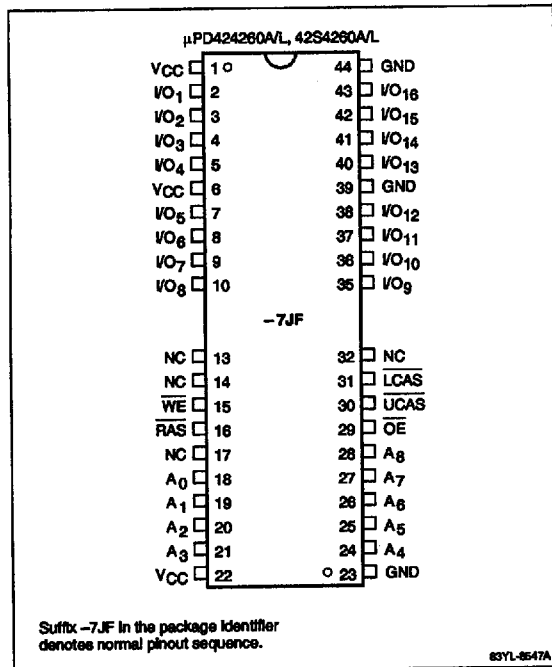
**40-Pin Plastic ZIP**



**44/40-Pin Plastic TSOP (Reverse Pinouts)**



**44/40-Pin Plastic TSOP (Normal Pinouts)**



**Pin Identification**

Name	Function
A <sub>0</sub> - A <sub>8</sub>	Address inputs
VO <sub>1</sub> - VO <sub>16</sub>	Data inputs and outputs
LCAS, UCAS	Column address strobes
OE	Output enable
RAS	Row address strobe
WE	Write enable
GND	Ground
VCC	+5-volt or +3.3-volt power supply
NC	No connection



**μPD424260A/L, 42S4260A/L**

**Ordering Information, μPD424260A (+ 5-volt power)**

Part Number	RAS Access Time (max)	Fast-Page Cycle Time (max)	CAS Access Time (max)	Package
μPD424260ALE-60	60 ns	40 ns	20 ns	40-pin plastic SOJ
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD424260AV-60	60 ns	40 ns	20 ns	40-pin plastic ZIP
V-70	70 ns	45 ns		
V-80	80 ns	50 ns		
μPD424260AG5-60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD424260AG5M-60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

**Ordering Information, μPD424260L (+ 3.3-volt power)**

Part Number	RAS Access Time (max)	Fast-Page Cycle Time (max)	CAS Access Time (max)	Package
μPD424260LLE-A60	60 ns	40 ns	20 ns	40-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD424260LV-A60	60 ns	40 ns	20 ns	40-pin plastic ZIP
V-A70	70 ns	45 ns		
V-A80	80 ns	50 ns		
μPD424260LG5-A60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD424260LG5M-A60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

**μPD424260A/L, 42S4260A/L****NEC****Ordering Information, μPD42S4260A (+ 5-volt power; self-refresh mode)**

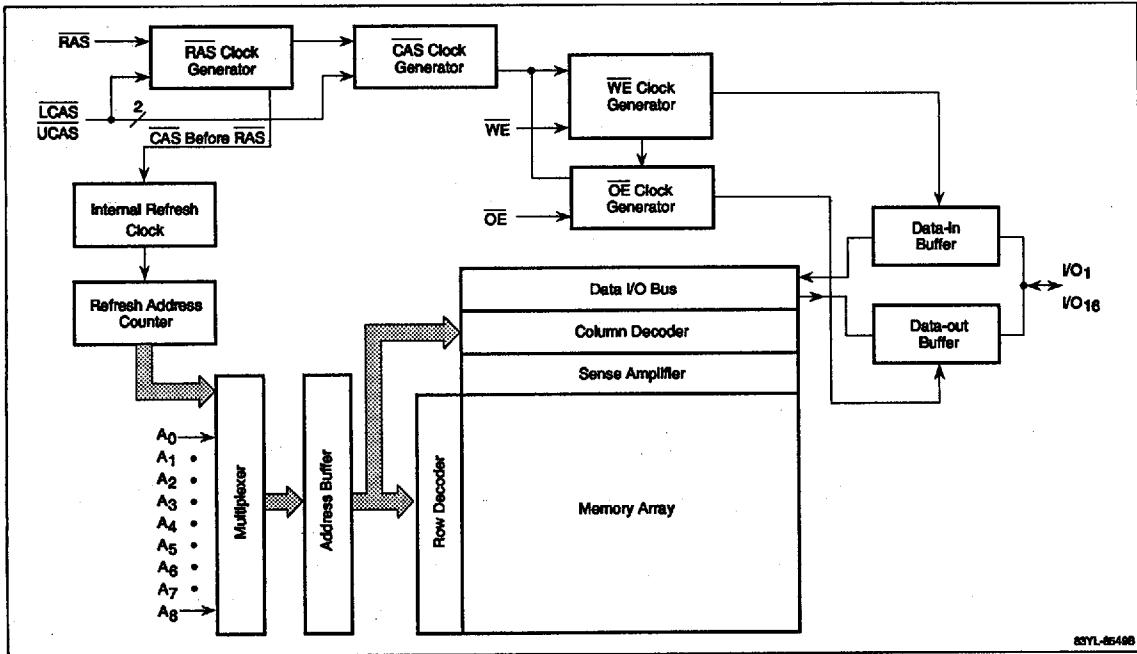
Part Number	RAS Access Time (max)	Fast-Page Cycle Time (max)	CAS Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4260ALE-60	60 ns	40 ns	20 ns	300 μA	40-pin plastic SOJ
LE-70	70 ns	45 ns			
LE-80	80 ns	50 ns			
μPD42S4260AV-60	60 ns	40 ns	20 ns	300 μA	40-pin plastic ZIP
V-70	70 ns	45 ns			
V-80	80 ns	50 ns			
μPD42S4260AG5-60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns			
G5-80	80 ns	50 ns			
μPD42S4260AG5M-60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns			
G5M-80	80 ns	50 ns			

**Ordering Information, μPD42S4260L (+ 3.3-volt power; self-refresh mode)**

Part Number	RAS Access Time (max)	Fast-Page Cycle Time (max)	CAS Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4260LLE-A60	60 ns	40 ns	20 ns	100 μA	40-pin plastic SOJ
LE-A70	70 ns	45 ns			
LE-A80	80 ns	50 ns			
μPD42S4260LV-A60	60 ns	40 ns	20 ns	100 μA	40-pin plastic ZIP
V-A70	70 ns	45 ns			
V-A80	80 ns	50 ns			
μPD42S4260LG5-A60	60 ns	40 ns	20 ns	100 μA	44/40-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns			
G5-A80	80 ns	50 ns			
μPD42S4260LG5M-A60	60 ns	40 ns	20 ns	100 μA	44/40-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns			
G5M-A80	80 ns	50 ns			



Block Diagram



Truth Table

Function	RAS	LCAS	UCAS	WE	OE	I/O <sub>1</sub> - I/O <sub>8</sub>	I/O <sub>9</sub> - I/O <sub>16</sub>
Standby	H	X	X	X	X	High-Z	High-Z
Refresh cycle	L	H	H	X	X	High-Z	High-Z
Byte read cycle	L	L	H	H	L	Data output	High-Z
	L	H	L	H	L	High-Z	Data output
Word read cycle	L	L	L	H	L	Data output	Data output
Byte write cycle	L	L	H	L	H	Data input	—
	L	H	L	L	H	—	Data input
Word write cycle	L	L	L	L	H	Data input	Data input
—	L	L	L	H	H	High-Z	High-Z

X = don't care.

**μPD424260A/L, 42S4260A/L****Absolute Maximum Ratings**

Voltage on any pin relative to GND	
424260A, 42S4260A	-1.0 to +7.0 V
424260L, 42S4260L	-0.5 to +4.6 V
Operating temperature, $T_{OPR}$	0 to +70°C
Storage temperature, $T_{STG}$	-55 to +125°C
Short-circuit output current, $I_{OS}$	
424260A, 42S4260A	50 mA
424260L, 42S4260L	20 mA
Power dissipation, $P_D$	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

**Capacitance** $T_A = 25^\circ\text{C}; f = 1\text{ MHz}$ 

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	$C_{I1}$	5	pF	Addresses
	$C_{I2}$	7	pF	LCAS, UCAS, WE, OE, RAS
Input/output capacitance	$C_O$	7	pF	$I/O_1 - I/O_{16}$

**Recommended Operating Conditions**

Parameter	Symbol	424260A, 42S4260A			424260L, 42S4260L			Unit
		Min	Typ	Max	Min	Typ	Max	
Input voltage, high	$V_{IH}$	2.4		$V_{CC} + 1.0$	2.0		$V_{CC} + 0.3$	V
Input voltage, low	$V_{IL}$	-1.0		0.8	-0.5		0.8	V
Supply voltage	$V_{CC}$	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	$T_A$	0		+70	0		+70	°C

**Self-Refresh Current** $T_A = 0$  to +70°C;  $V_{CC} = +5\text{ V} \pm 10\%$  (42S4260A) or  $+3.3\text{ V} \pm 0.3\text{ V}$  (42S4260L)

Symbol	42S4260A	42S4260L	Conditions
$I_{CC7}$	300 $\mu\text{A}$ max	100 $\mu\text{A}$ max	I/O pins: $V_{IH} \geq V_{CC} - 0.2\text{ V}$ ; $V_{IL} \leq 0.2\text{ V}$ or open. Other input pins: $V_{IH} \geq V_{CC} - 0.2\text{ V}$ ; $V_{IL} \leq 0.2\text{ V}$ or open. $t_{RAS} \geq 100\ \mu\text{s}$

**DC Characteristics; μPD424260A, 42S4260A** $T_A = 0$  to +70°C;  $V_{CC} = +5.0\text{ V} \pm 10\%$ 

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	$I_{CC2}$			2.0	mA	RAS = CAS $\geq V_{IH}$ (min); $I_O = 0\text{ mA}$
				300	$\mu\text{A}$	RAS = CAS $\geq V_{CC} - 0.2\text{ V}$ ; $I_O = 0\text{ mA}$
Input leakage current	$I_{I(L)}$	-10		10	$\mu\text{A}$	$V_{IN} = 0\text{ V}$ to $V_{CC}$ ; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	-10		10	$\mu\text{A}$	DO <sub>OUT</sub> disabled; $V_{OUT} = 0\text{ V}$ to $V_{CC}$
Output voltage, low	$V_{OL}$			0.4	V	$I_{OL} = 4.2\text{ mA}$
Output voltage, high	$V_{OH}$	2.4			V	$I_{OH} = -5\text{ mA}$

DC Characteristics;  $\mu$ PD424260L, 42S4260L $T_A = 0$  to  $+70^\circ\text{C}$ ;  $V_{CC} = +3.3\text{ V} \pm 0.3\text{ V}$ 

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	$I_{CC2}$			500	$\mu\text{A}$	$\overline{\text{RAS}} = \overline{\text{CAS}} \geq V_{IH}(\text{min}); I_O = 0\text{ mA}$
				100	$\mu\text{A}$	$\overline{\text{RAS}} = \overline{\text{CAS}} \geq V_{CC} - 0.2\text{ V}; I_O = 0\text{ mA}$
Input leakage current	$I_{I(L)}$	-5		5	$\mu\text{A}$	$V_{IN} = 0\text{ V}$ to $V_{CC}$ ; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	-5		5	$\mu\text{A}$	$D_{OUT}$ disabled; $V_{OUT} = 0\text{ V}$ to $V_{CC}$
Output voltage, low	$V_{OL}$			0.4	V	$I_{OL} = 2.0\text{ mA}$
Output voltage, high	$V_{OH}$	2.4			V	$I_{OH} = -2.0\text{ mA}$

## AC Characteristics

 $T_A = 0$  to  $+70^\circ\text{C}$  $\mu$ PD424260A, 42S4260A:  $V_{CC} = +5.0\text{ V} \pm 10\%$  $\mu$ PD424260L, 42S4260L:  $V_{CC} = +3.3\text{ V} \pm 0.3\text{ V}$ 

Parameter	Symbol	-60		-70		-80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Operating current, average	$I_{CC1} (+5)$		140		130		120	mA	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling; $t_{RC} = t_{RC} \text{ min}$ (Note 5)
	$I_{CC1} (+3.3)$		130		120		110		
Operating current, $\overline{\text{RAS}}$ -only refresh cycle, average	$I_{CC3} (+5)$		140		130		120	mA	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}} \geq V_{IH} \text{ min}$ ; $t_{RC} = t_{RC} \text{ min}$ (Note 5)
	$I_{CC3} (+3.3)$		130		120		110		
Operating current, fast-page cycle, average	$I_{CC4} (+5)$		90		80		70	mA	$\overline{\text{RAS}} \leq V_{IL}$ ; $\overline{\text{CAS}}$ cycling; $t_{PC} = t_{PC} \text{ min}$ (Note 5)
	$I_{CC4} (+3.3)$		90		80		70		
Operating current, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle, average	$I_{CC5} (+5)$		140		130		120	mA	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}} \leq V_{IL} \text{ max}$ ; $t_{RC} = t_{RC} \text{ min}$ (Note 5)
	$I_{CC5} (+3.3)$		130		120		110		
Access time from column address	$t_{AA}$		30		35		40	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{\text{CAS}}$ precharge (rising edge)	$t_{ACP}$		35		40		45	ns	(Notes 3, 4, 7, 8)
Column address setup time	$t_{ASC}$	0		0		0		ns	
Row address setup time	$t_{ASR}$	0		0		0		ns	
Column address to $\overline{\text{WE}}$ delay time	$t_{AWD}$	50		55		70		ns	(Note 14)
Access time from $\overline{\text{CAS}}$ (falling edge)	$t_{CAC}$		20		20		20	ns	(Notes 3, 4, 7, 8)
Column address hold time	$t_{CAH}$	15		15		15		ns	
$\overline{\text{CAS}}$ pulse width	$t_{CAS}$	20	10,000	20	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ hold time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refreshing	$t_{CHR}$	15		15		15		ns	(Note 15)
$\overline{\text{CAS}}$ hold time (CBR self-refresh mode)	$t_{CHS}$	-35		-40		-50		ns	For 42S4260A/L only

$\mu$ PD424260A/L, 42S4260A/L

## AC Characteristics (cont)

Parameter	Symbol	-60		-70		-80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
CAS to output in low-Z	t <sub>CLZ</sub>	0		0		0		ns	(Notes 4, 7)
Fast-page CAS precharge time	t <sub>CP</sub>	10		10		10		ns	
CAS precharge time	t <sub>CPN</sub>	10		10		10		ns	
Fast-page CAS precharge to $\overline{WE}$ delay time	t <sub>CPWD</sub>	55		60		75		ns	(Note 14)
CAS to $\overline{RAS}$ precharge time	t <sub>CRP</sub>	10		10		10		ns	(Note 10)
CAS hold time	t <sub>CSH</sub>	60		70		80		ns	
CAS setup time for CAS before RAS refresh cycle	t <sub>CSR</sub>	5		5		5		ns	(Note 15)
CAS to $\overline{WE}$ delay	t <sub>CWD</sub>	40		40		50		ns	(Note 14)
Write command referenced to CAS lead time	t <sub>CWL</sub>	15		15		15		ns	
Data-in hold time	t <sub>DH</sub>	15		15		15		ns	(Notes 13, 16)
Data-in setup time	t <sub>DS</sub>	0		0		0		ns	(Notes 13, 16)
Masked write hold time referenced to RAS	t <sub>MRH</sub>	0		0		0		ns	
Access time from OE	t <sub>OEA</sub>		20		20		20	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t <sub>OED</sub>	15		15		15		ns	
$\overline{OE}$ command hold time	t <sub>OEH</sub>	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t <sub>OES</sub>	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t <sub>OEZ</sub>	0	15	0	15	0	15	ns	(Note 9)
Output disable from CAS high	t <sub>OFF</sub>	0	15	0	15	0	20	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t <sub>OLZ</sub>	0		0		0		ns	(Notes 5, 7)
Fast-page read or write cycle time	t <sub>PC</sub>	40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time with extended data output	t <sub>PRWC</sub>	85		90		100		ns	(Note 6)



## AC Characteristics (cont)

Parameter	Symbol	-60		-70		-80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Access time from RAS	t <sub>RAC</sub>		60		70		80	ns	(Notes 3, 4, 7, 8)
RAS to column address delay time	t <sub>RAD</sub>	15	30	15	35	15	40	ns	(Note 8)
Row address hold time	t <sub>RAH</sub>	10		10		10		ns	
Column address lead time referenced to $\overline{\text{RAS}}$ (rising edge)	t <sub>RAL</sub>	30		35		40		ns	
RAS pulse width	t <sub>RAS</sub>	60	10,000	70	10,000	80	10,000	ns	
Fast-page RAS pulse width	t <sub>RASP</sub>	60	125,000	70	125,000	80	125,000	ns	
RAS pulse width (CBR self-refresh mode)	t <sub>RASS</sub>	100		100		100		μs	For 42S4260A/L
Random read or write cycle time	t <sub>RC</sub>	120		130		150		ns	(Note 6)
RAS to CAS delay time	t <sub>RCD</sub>	20	40	20	50	20	60	ns	(Note 8)
Read command hold time referenced to $\overline{\text{CAS}}$	t <sub>RCH</sub>	0		0		0		ns	(Note 11)
Read command setup time	t <sub>RCS</sub>	0		0		0		ns	
Refresh period	t <sub>REF</sub>		8		8		8	ms	Addresses A <sub>0</sub> - A <sub>8</sub>
RAS hold time referenced to $\overline{\text{CAS}}$ precharge	t <sub>RHCP</sub>	35		40		45		ns	
RAS precharge time	t <sub>RP</sub>	50		50		60		ns	
RAS precharge CAS hold time	t <sub>RPC</sub>	0		0		0		ns	
RAS precharge time (CBR self-refresh mode)	t <sub>RPS</sub>	120		130		150		ns	For 42S4260A/L
Read command hold time referenced to $\overline{\text{RAS}}$	t <sub>RRH</sub>	0		0		0		ns	(Note 11)
RAS hold time	t <sub>RSH</sub>	20		20		25		ns	
Read-modify-write cycle time	t <sub>RWC</sub>	165		175		200		ns	(Note 6)
RAS to $\overline{\text{WE}}$ delay	t <sub>RWD</sub>	80		90		105		ns	(Note 14)
Write command referenced to $\overline{\text{RAS}}$ lead time	t <sub>RWL</sub>	20		20		20		ns	
Rise and fall times	t <sub>T</sub>	3	50	3	50	3	50	ns	(Note 4)

$\mu$ PD424260A/L, 42S4260A/L**NEC****AC Characteristics (cont)**

Parameter	Symbol	-60		-70		-80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Write command hold time	$t_{WCH}$	15		15		15		ns	(Note 12)
Write command setup time	$t_{WCS}$	0		0		0		ns	(Note 14)
Write command pulse width	$t_{WP}$	15		15		15		ns	(Note 12)

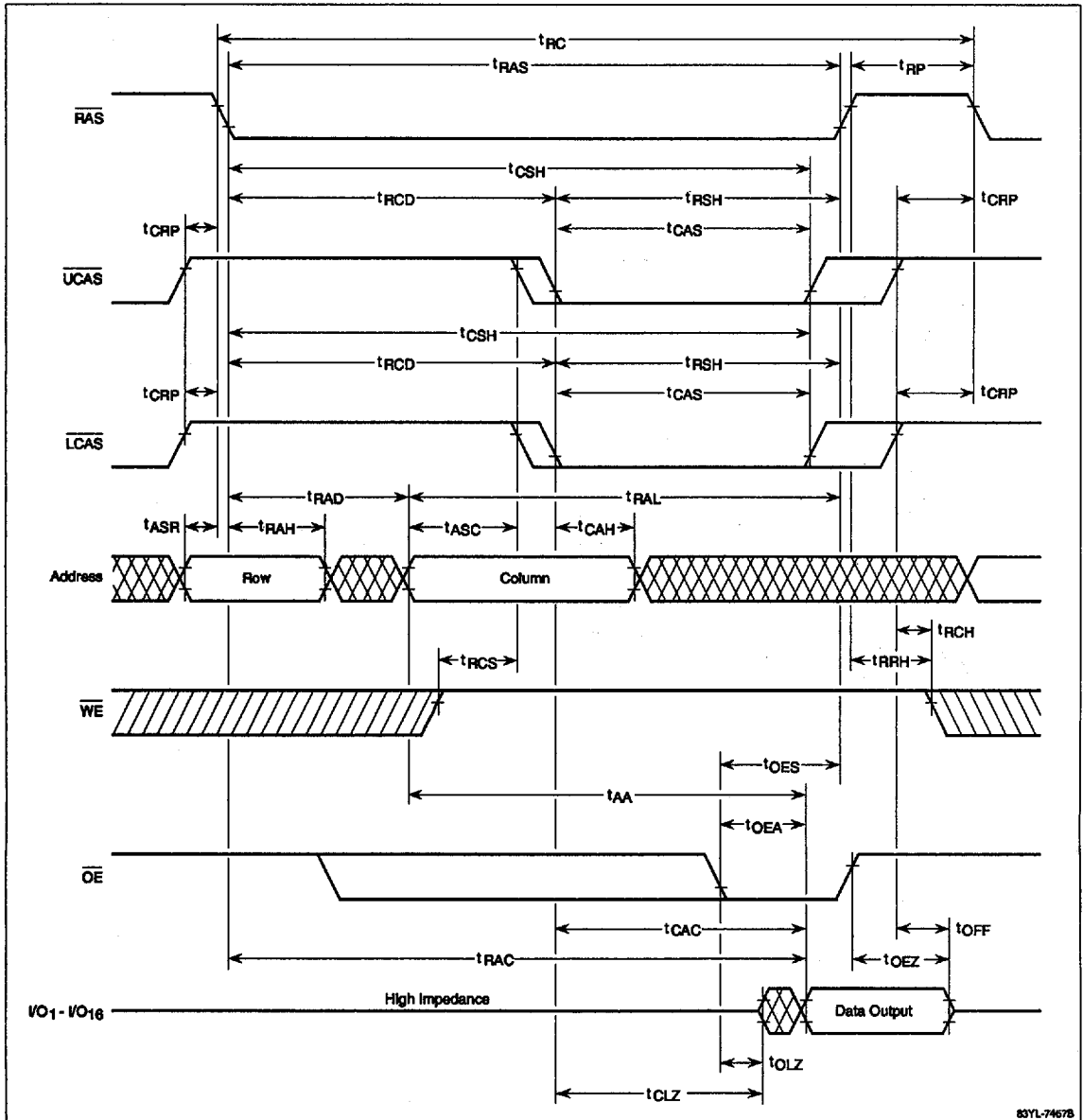
**Notes:**

- (1) All voltages are referenced to GND.
- (2) An initial pause of 100  $\mu$ s is required after power-up, followed by any eight RAS cycles, before proper device operation is achieved.
- (3) Ac measurements assume  $t_T = 5$  ns.
- (4)  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring the timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- (5)  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ , and  $I_{CC5}$  depend on output loading and cycle rates. Specified values are obtained with the output open.  $I_{CC3}$  is measured assuming that all column address inputs are held at either a high level or a low level during RAS-only refresh cycles.  $I_{CC4}$  is measured assuming that all column address inputs are switched only once during each fast-page cycle.
- (6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ( $T_A = 0$  to  $+70^\circ\text{C}$ ) is assured.
- (7) Load = 2 TTL ( $-1$  mA,  $+4$  mA) loads and 100 pF. For 3.3-volt devices,  $V_{OH} = 2.0$  V,  $V_{OL} = 0.8$  V.
- (8) If  $t_{RCD} \leq t_{RCD}(\text{max})$  and  $t_{RAD} \leq t_{RAD}(\text{max})$ , access time is defined by  $t_{RAC}(\text{max})$ . If  $t_{RCD} \geq t_{RCD}(\text{max})$ , access time is defined by  $t_{CAC}(\text{max})$ ; if  $t_{RAD} \geq t_{RAD}(\text{max})$  access time is defined by  $t_{AA}(\text{max})$ .
- (9)  $t_{OFF}(\text{max})$  and  $t_{OEZ}(\text{max})$  define the time at which the outputs become open-circuit and are not referenced to  $V_{OH}$  or  $V_{OL}$ .
- (10) The  $t_{CRP}$  requirement should be applicable for RAS/CAS cycles preceded by any cycle.
- (11) Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.
- (12) Parameter  $t_{WP}$  is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both  $t_{WCS}$  and  $t_{WCH}$  must be met.
- (13) These parameters are referenced to the falling edge of one of the CAS signals for early write cycles and to the falling edge of WE for delayed write or read-modify-write cycles.
- (14)  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{CPWD}$  and  $t_{AWD}$  are restrictive operating parameters in read-write/read-modify-write cycles only. If  $t_{WCS} \geq t_{WCS}(\text{min})$ , the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If  $t_{CWD} \geq t_{CWD}(\text{min})$ ,  $t_{RWD} \geq t_{RWD}(\text{min})$ , and  $t_{AWD} \geq t_{AWD}(\text{min})$ , then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until CAS returns to  $V_{IH}$ ) is indeterminate.
- (15) Holding  $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$  low prior to RAS going negative will initiate a CAS before RAS refresh cycle ( $t_{CSR}$  and  $t_{CHR}$  must be satisfied).
- (16) The first  $\overline{\text{WE}}$  falling edge is used as a reference for the setup and hold requirements of  $t_{ASC}$ ,  $t_{CAH}$ ,  $t_{DS}$ , and  $t_{DH}$  (early write cycle).
- (17) The first  $\overline{\text{CAS}}$  falling edge is used as a reference for the start of  $t_{ACP}$  (CAS precharge access time).



Timing Waveforms

Word Read Cycle



7c

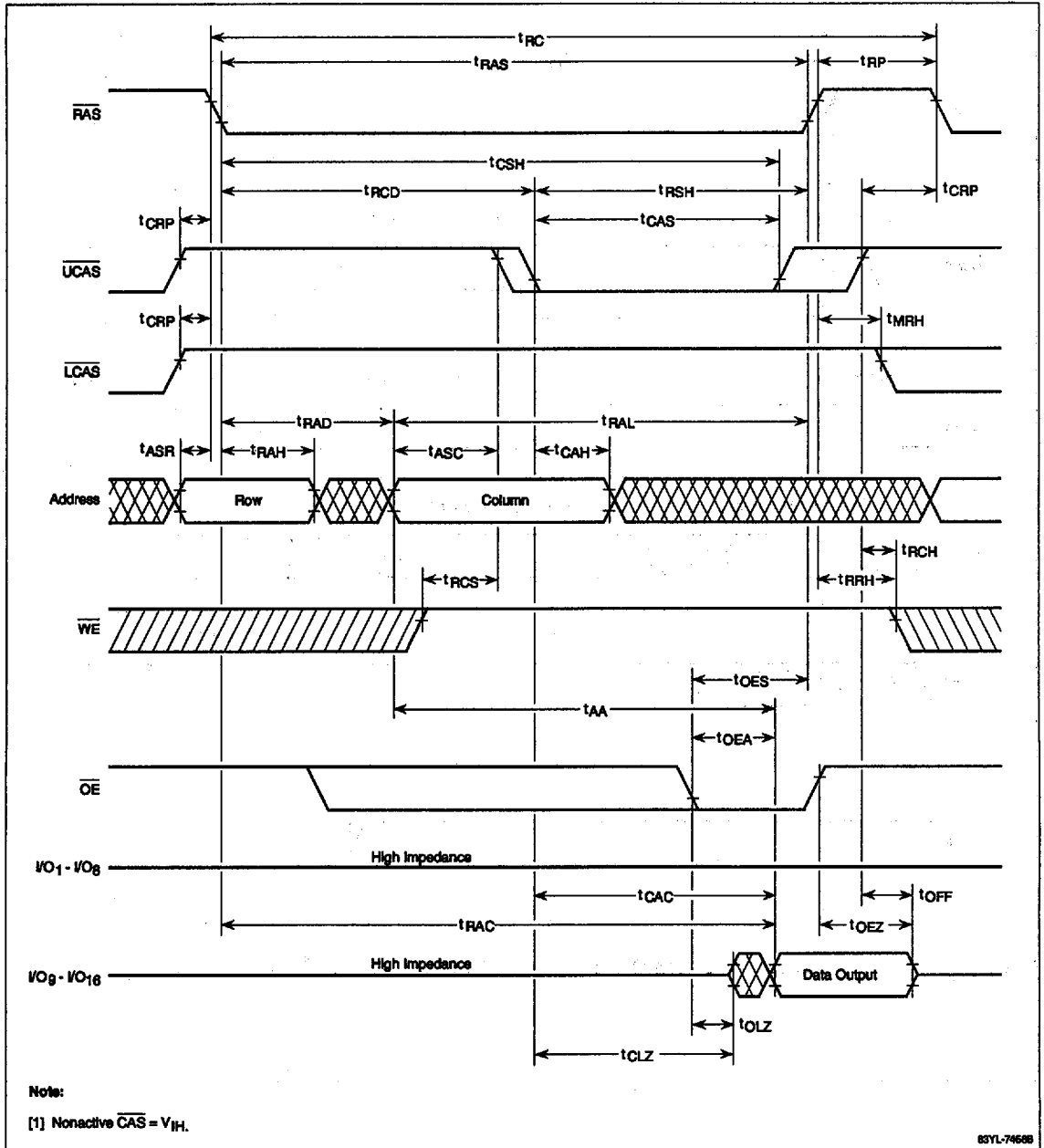
83YL-74678

**μPD424260A/L, 42S4260A/L**



**Timing Waveforms (cont)**

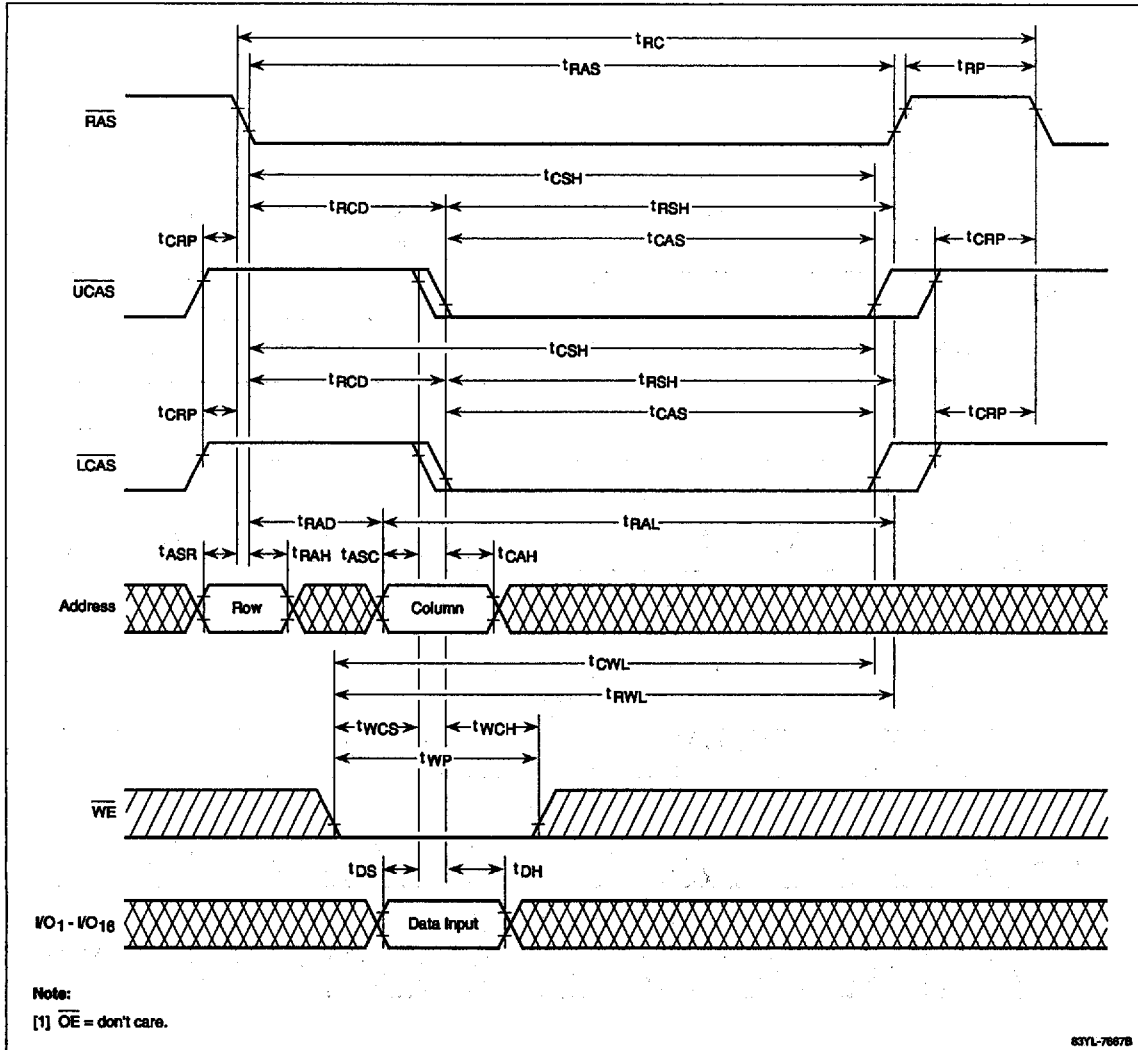
**Byte Read Cycle**



83YL-74688

Timing Waveforms (cont)

**Word Early-Write Cycle**



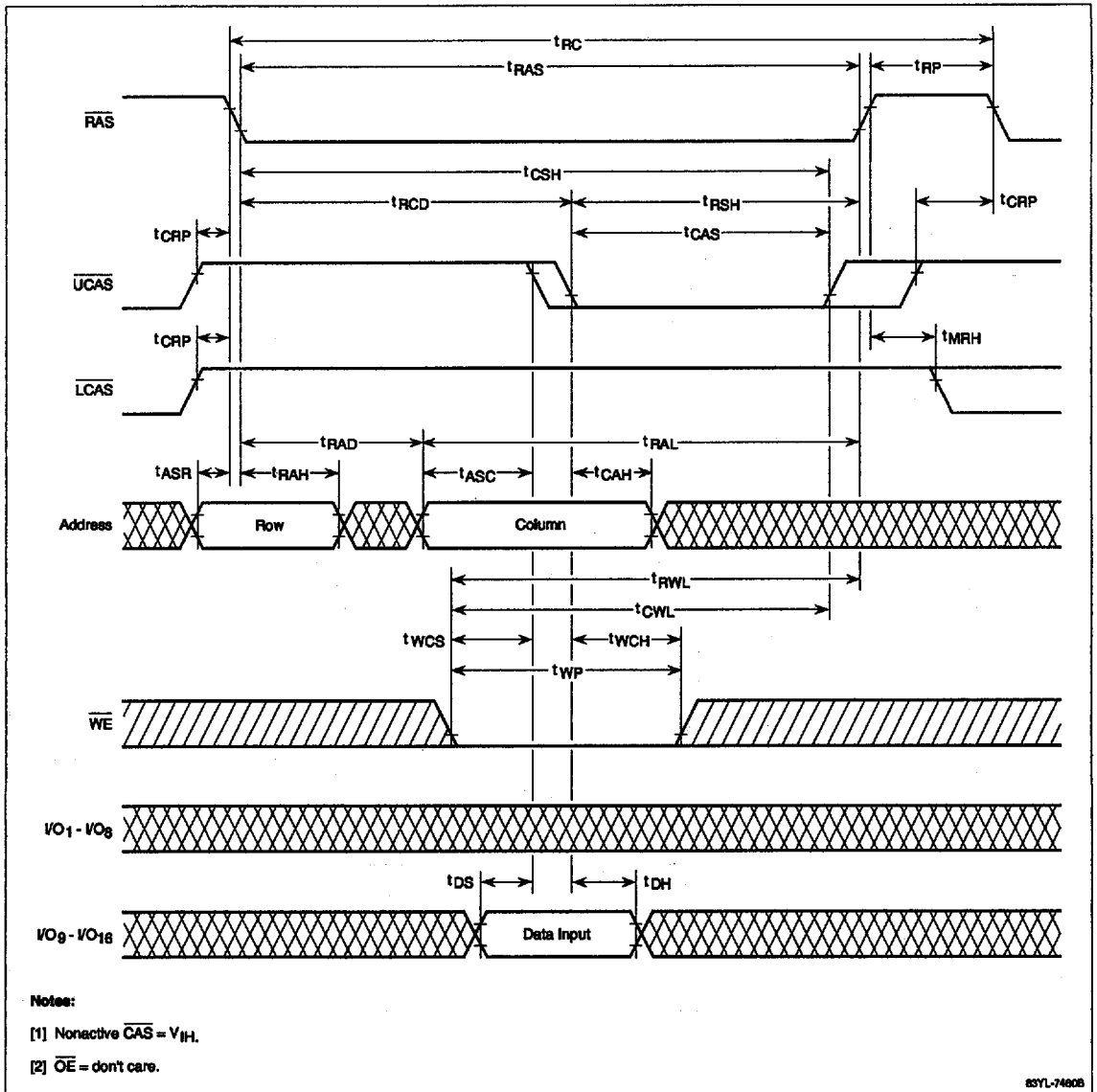
7c

**μPD424260A/L, 42S4260A/L**



**Timing Waveforms (cont)**

**Byte Early-Write Cycle**

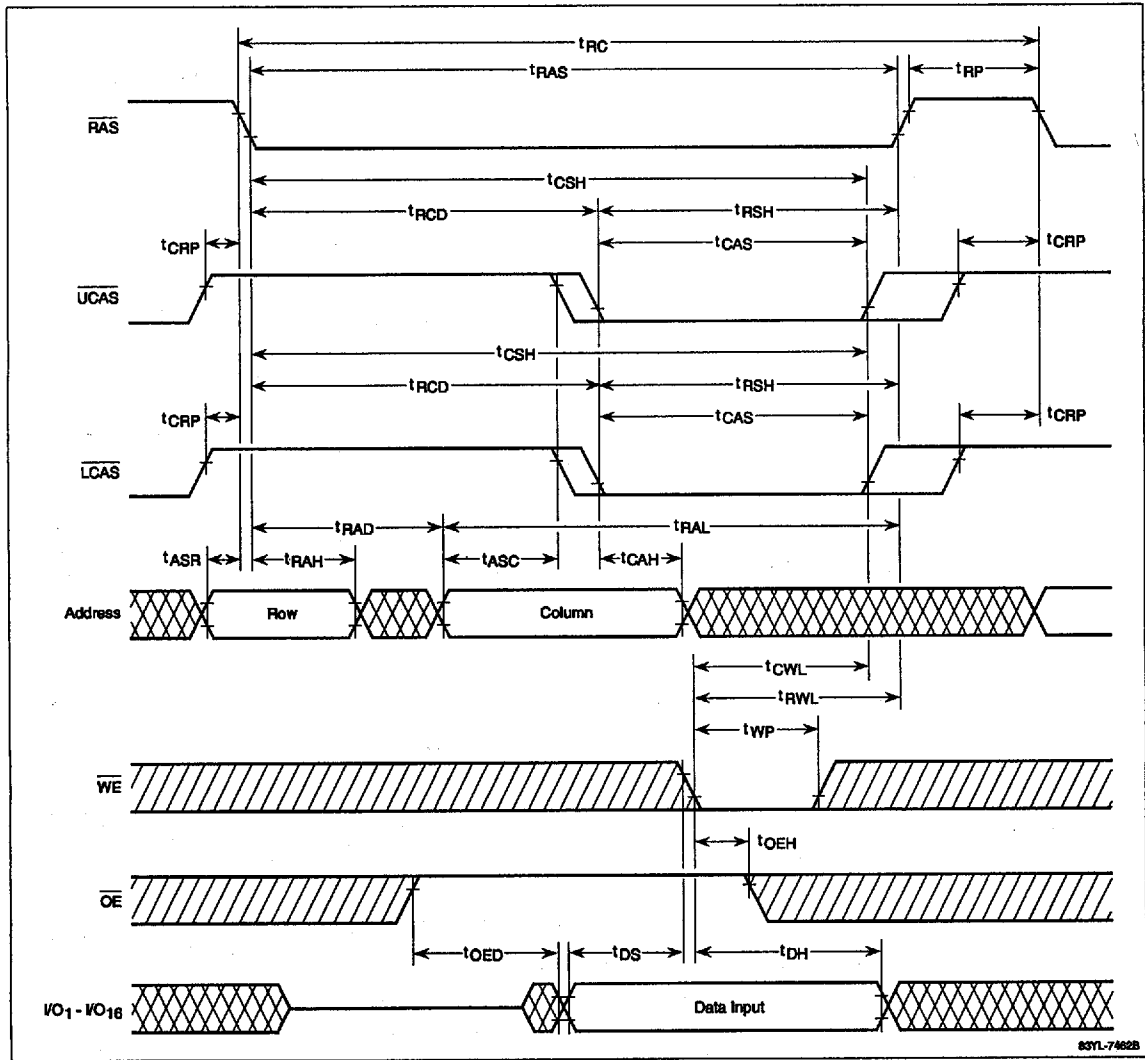


63YL-74008



Timing Waveforms (cont)

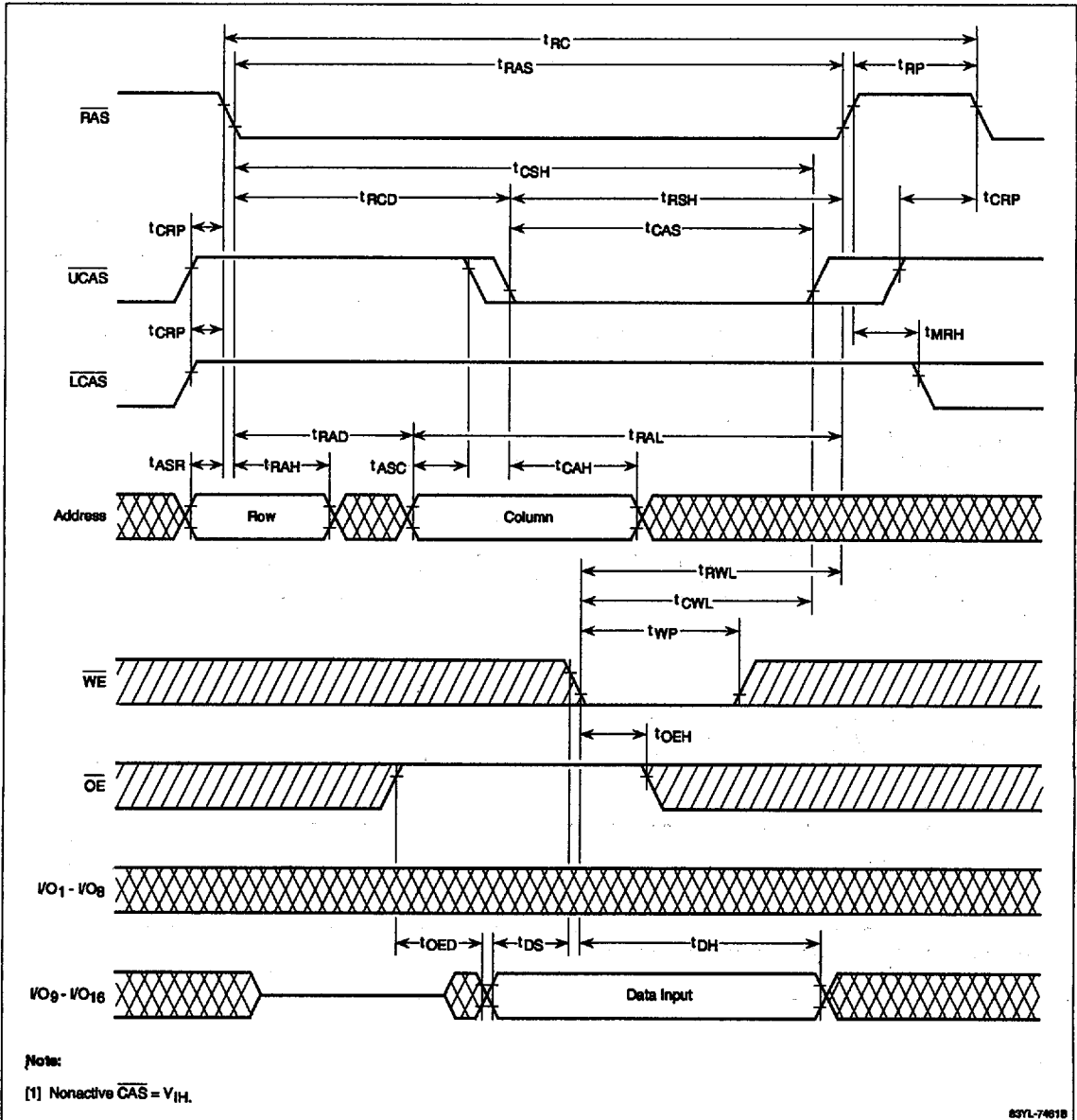
Word Late-Write Cycle



7c

Timing Waveforms (cont)

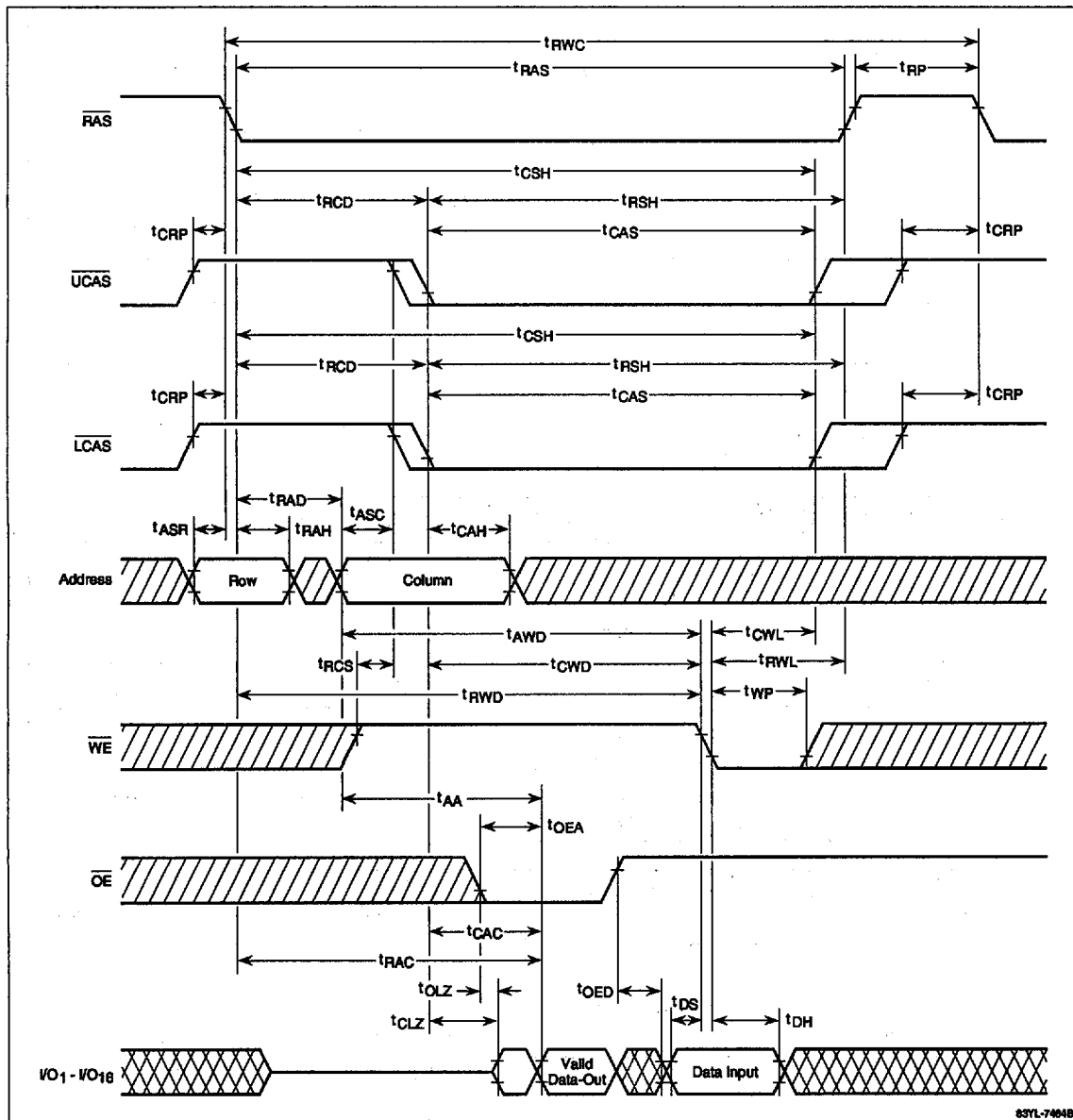
Byte Late-Write Cycle



63YL-7461B

Timing Waveforms (cont)

Word Read-Modify-Write Cycle

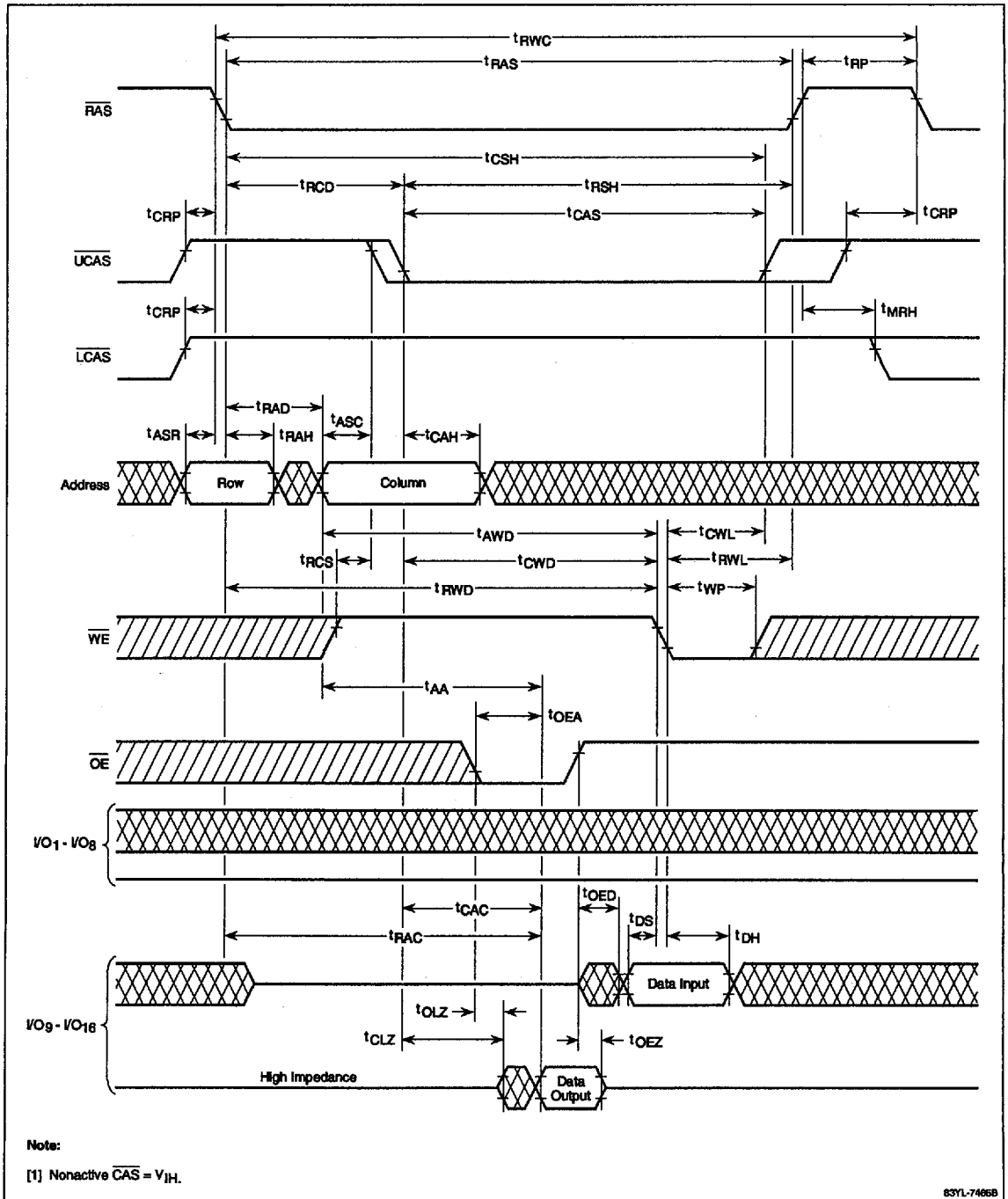


7c

**$\mu$ PD424260A/L, 42S4260A/L**

**Timing Waveforms (cont)**

**Byte Read-Modify-Write Cycle**





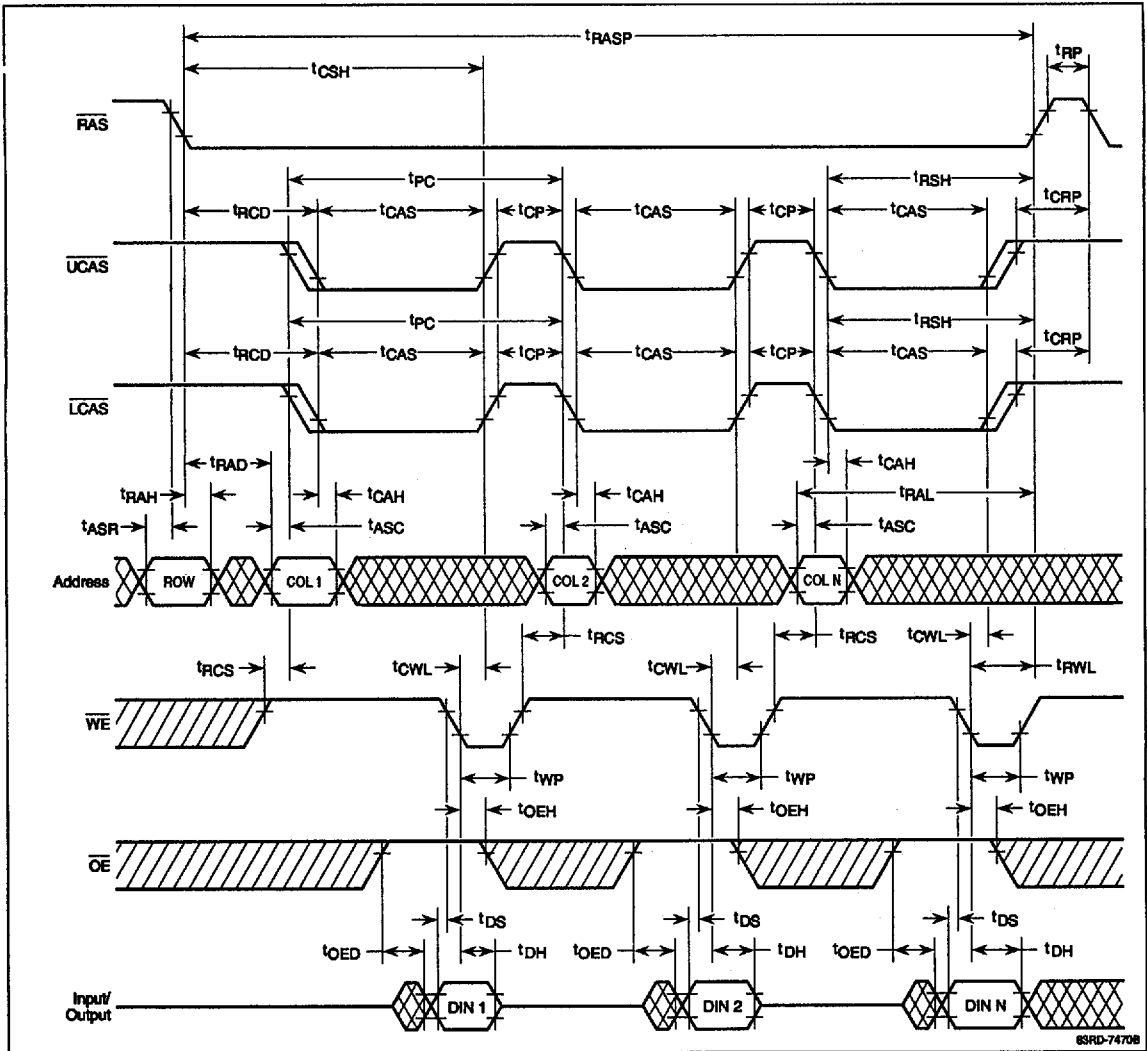






Timing Waveforms (cont)

Word Fast-Page Late-Write Cycle



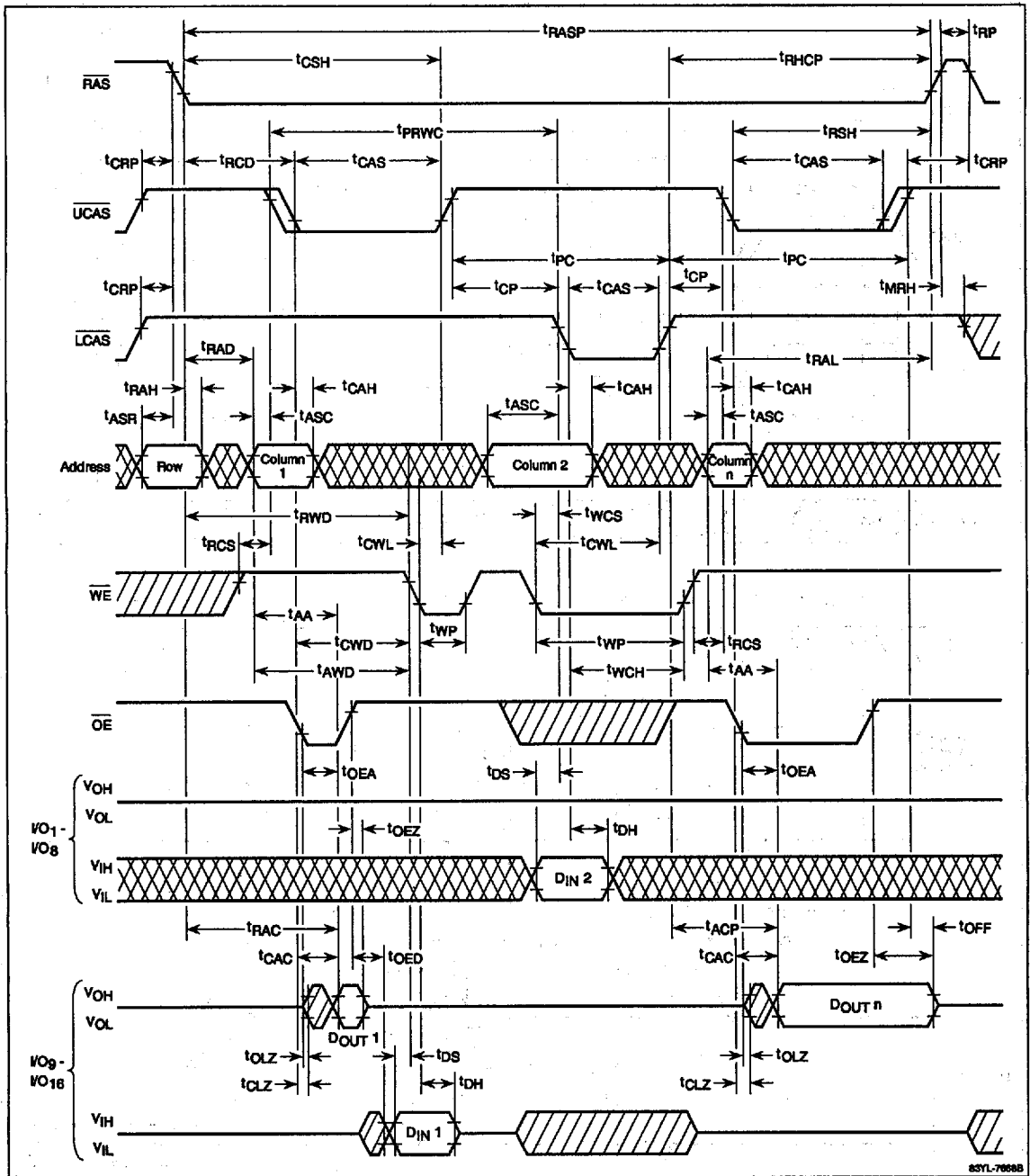
7c





Timing Waveforms (cont)

Byte Fast-Page Read/Write Cycle



7c

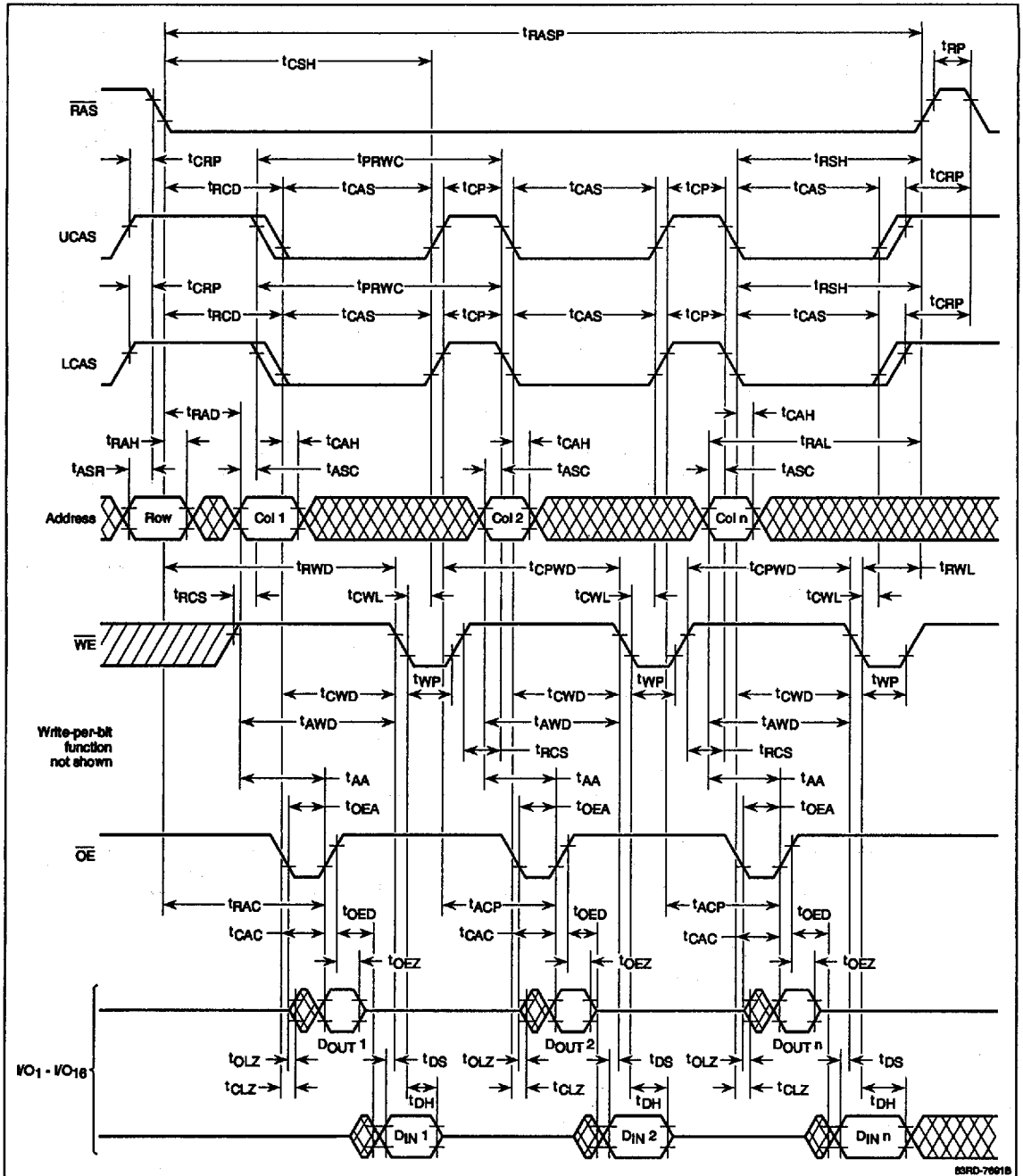
85YL-7668

**μPD424260A/L, 42S4260A/L**



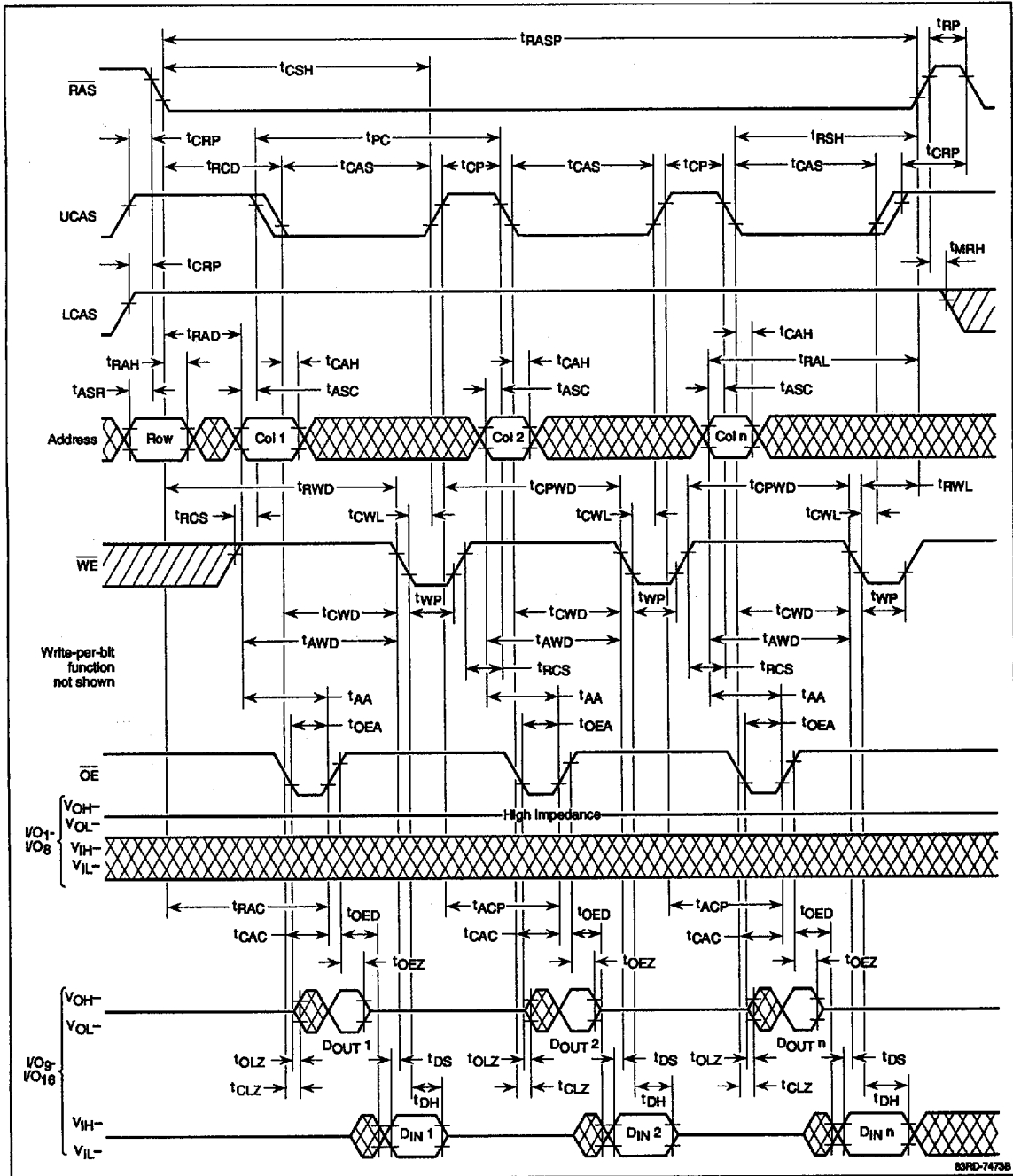
**Timing Waveforms (cont)**

**Word Fast-Page Read-Modify-Write Cycle**



Timing Waveforms (cont)

Byte Fast-Page Read-Modify-Write Cycle

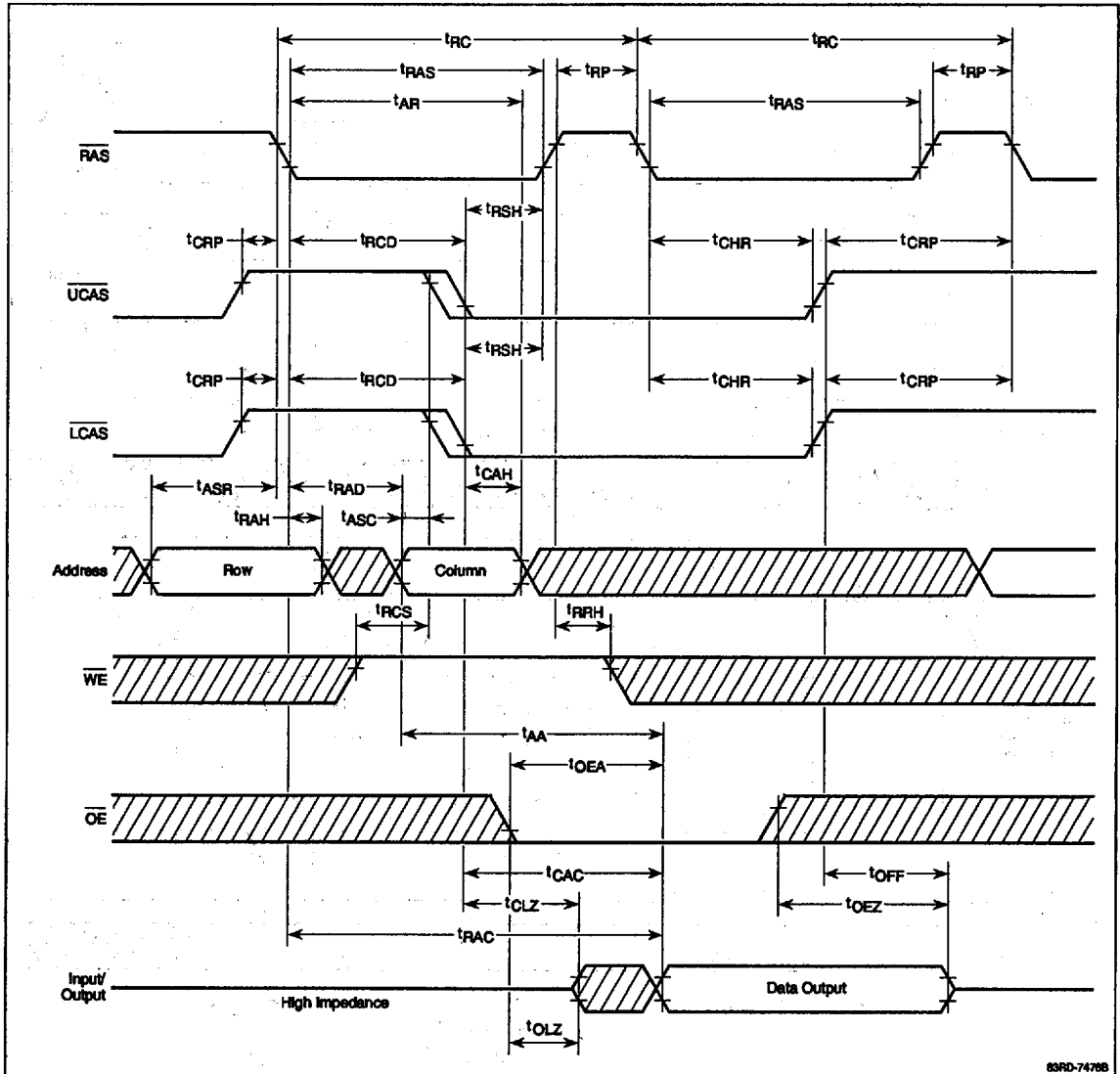


7c

83RD-7478B

Timing Waveforms (cont)

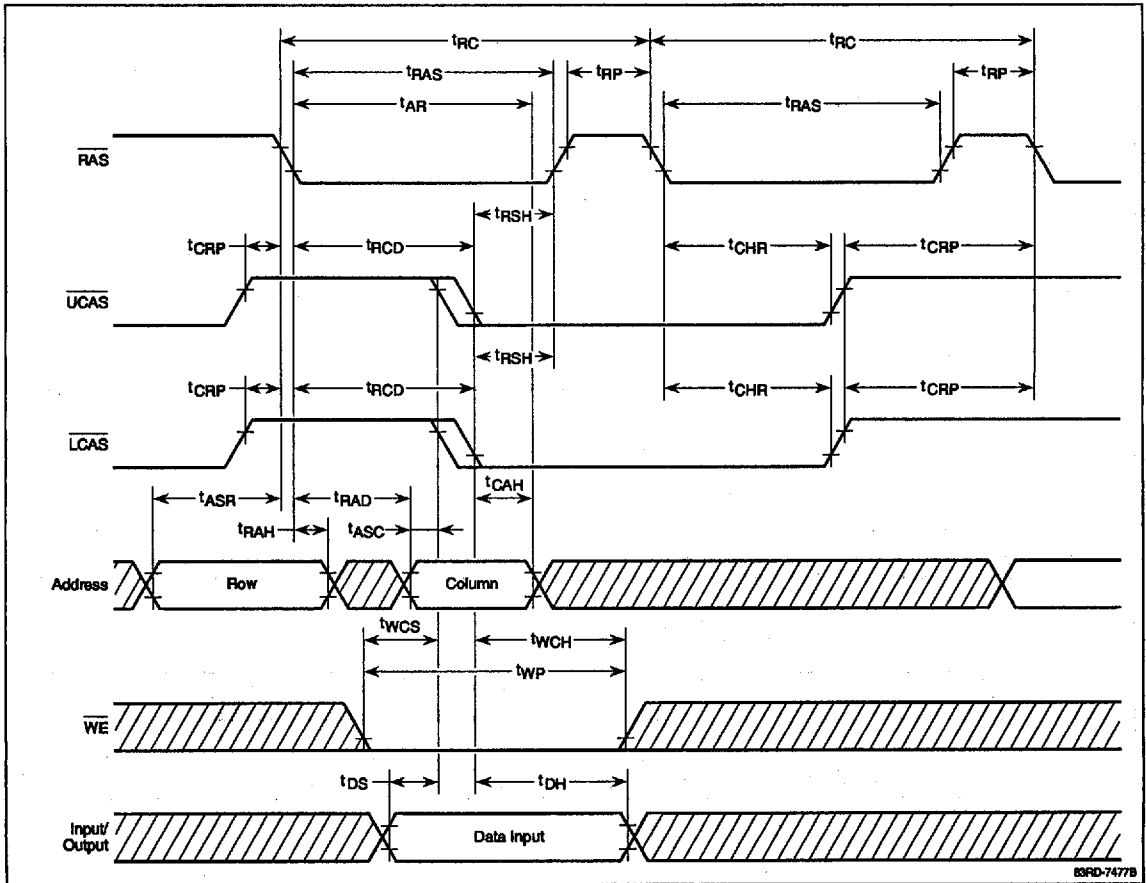
Hidden Refresh Cycle (Word Read Cycle)



83RD-74788

Timing Waveforms (cont)

**Hidden-Refresh Cycle (Word Write Cycle)**



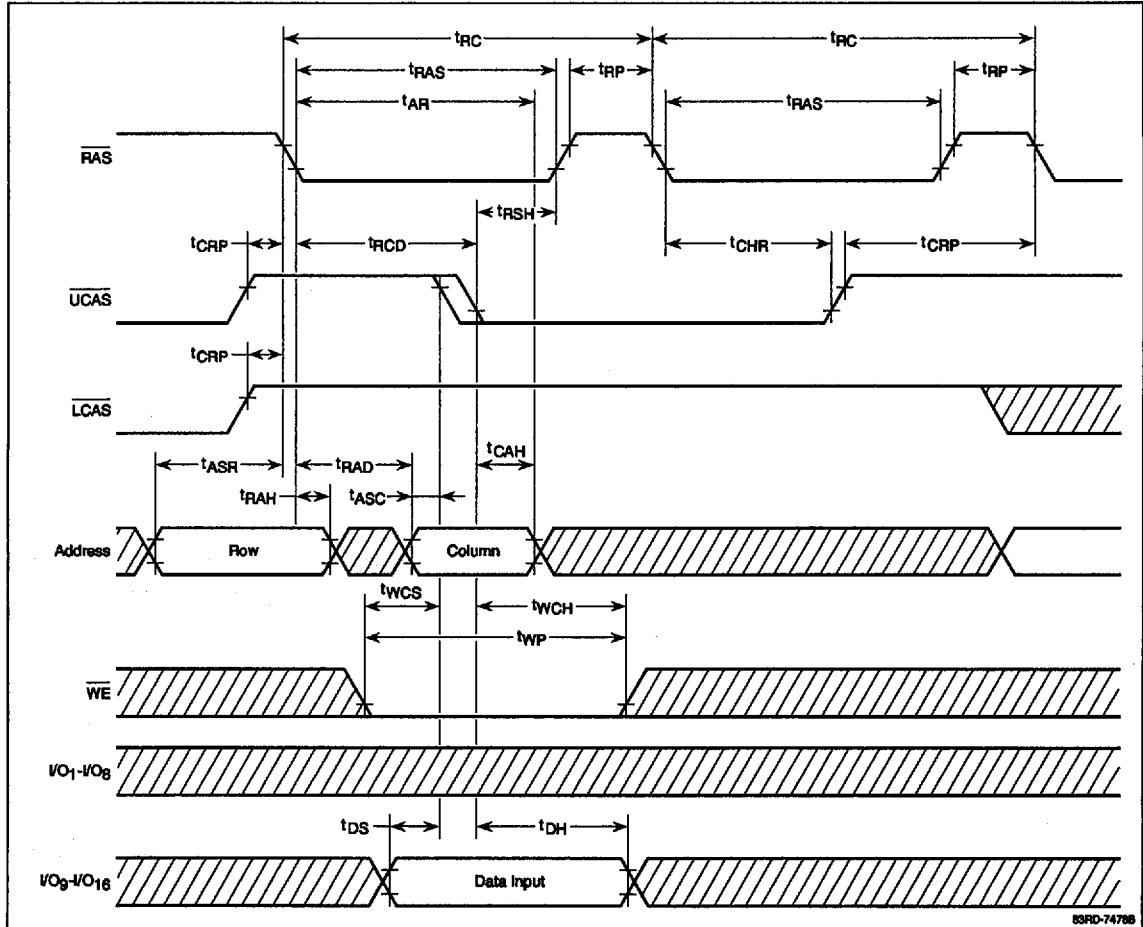
7c

**μPD424260A/L, 42S4260A/L**



**Timing Waveforms (cont)**

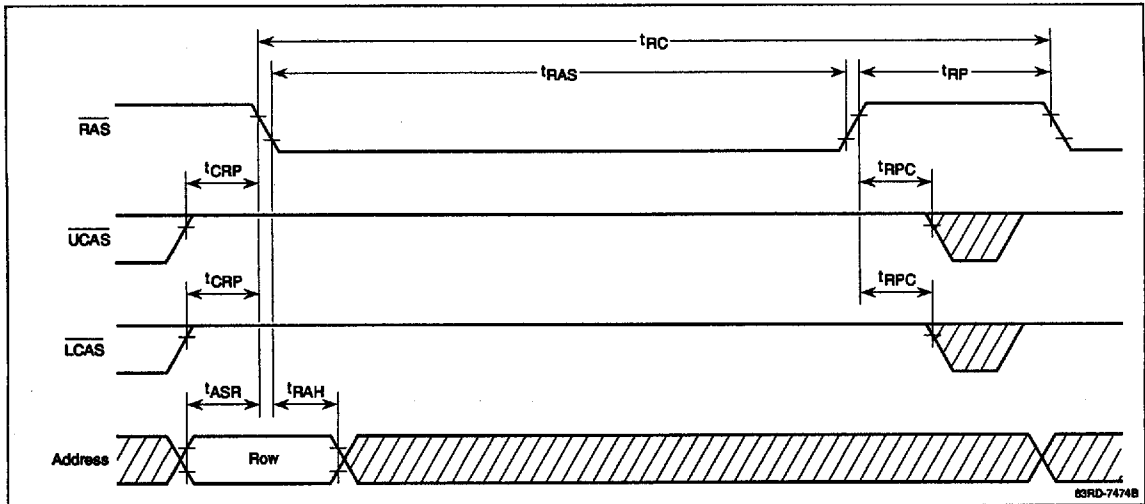
**Hidden-Refresh Cycle (Byte Write Cycle)**





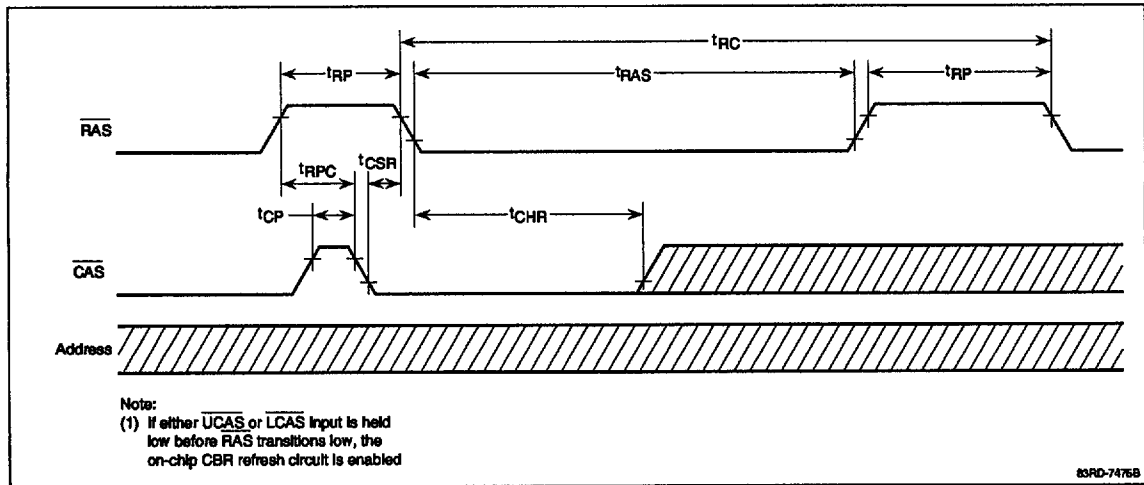
Timing Waveforms (cont)

**RAS-Only Refresh Cycle**



83RD-7474B

**CAS Before RAS Refresh Cycle**



Note:  
 (1) If either  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$  input is held low before  $\overline{\text{RAS}}$  transitions low, the on-chip CBR refresh circuit is enabled

83RD-7475B

7c

**$\mu$ PD424260A/L, 42S4260A/L****NEC****Timing Waveforms (cont)****CBR Self-Refresh Cycle**