National Semiconductor

COP8FG Family
8-Bit CMOS ROM Based Microcontrollers with 8k to 32k Memory, Two Comparators and USART

General Description

Note: COP8FG devices are 15 MHz versions of the COP8SG devices.

The COP8FGx5 Family ROM based microcontrollers are highly integrated COP8™ Feature core devices with 8k to 32k memory and advanced features including Analog comparators, and zero external components. These single-chip CMOS devices are suited for more complex applications requiring a full featured controller with larger memory, low EMI, two comparators, and a full-duplex USART. COP8FGx7 devices are 100% form-fit-function compatible 8k or 32k OTP (One Time Programmable) versions for use in production or development.

Erasable windowed versions are available for use with a range of COP8 software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 15 MHz CKI with 0.67 µs instruction cycle, 14 interrupts, three multi-function 16-bit timer/counters with PWM, full duplex USART, MICROWIRE/PLUS™, two analog comparators, two power saving HALT/IDLE modes, MIWU, idle timer, on-chip R/C oscillator, high current outputs, user selectable options (WATCHDOG™, 4 clock/oscillator modes, power-on-reset), 4.5V to 5.5V operation, program code security, and 28/40/44 pin packages.

Devices included in this datasheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature
COP8FGE5	8k ROM	256	24/36/40	28 DIP/SOIC, 40 DIP, 44 PLCC/QFP	-40 to +85°C
COP8FGG5	16k ROM	512	24/36/40	28 DIP/SOIC, 40 DIP, 44 PLCC/QFP	-40 to +85°C
COP8FGH5	20k ROM	512	24/36/40	28 DIP/SOIC, 40 DIP, 44 PLCC/QFP	-40 to +85°C
COP8FGK5	24k ROM	512	24/36/40	28 DIP/SOIC, 40 DIP, 44 PLCC/QFP	-40 to +85°C
COP8FGR5	32k ROM	512	24/36/40	28 DIP/SOIC, 40 DIP, 44 PLCC/QFP	-40 to +85°C
COP8FGE7	8k OTP EPROM	256	24/36/40	28 DIP/SOIC, 40 DIP, 44 PLCC/QFP	-40 to +85°C
COP8FGR7	32k OTP EPROM	512	24/36/40	28 DIP/SOIC, 40 DIP, 44 PLCC/QFP	-40 to +85°C
COP8FGR7-Q3	32k EPROM	512	24/36/40	28 DIP/SOIC, 40 DIP, 44 PLCC/QFP	Room Temp.

Key Features

- Low cost 8-bit microcontroller
- Quiet Design (low radiated emissions)
- Multi-Input Wakeup pins with optional interrupts (8 pins)
- Mask selectable clock options
  - — Crystal oscillator
  - — Crystal oscillator option with on-chip bias resistor
  - — External oscillator
  - — Internal R/C oscillator
- Internal Power-On-Reset — user selectable
- WATCHDOG and Clock Monitor Logic — user selectable
- Eight high current outputs
- 256 or 512 bytes on-board RAM
- 8k to 32k ROM or OTP EPROM with security feature

CPU Features

- Versatile easy to use instruction set
- 0.67 µs instruction cycle time
- Fourteen multi-source vectored interrupts servicing
  - — External interrupt / Timers T0 — T3
  - — MICROWIRE/PLUS Serial Interface
  - — Multi-Input Wake Up
  - — Software Trap
  - — USART (2; 1 receive and 1 transmit)
  - — Default VIS (default interrupt)
- 8-bit Stack Pointer SP (stack in RAM)
- Two 8-bit Register Indirect Data Memory Pointers
- True bit manipulation
- BCD arithmetic instructions

Peripheral Features

- Multi-Input Wakeup Logic
- Three 16-bit timers (T1 — T3), each with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event Counter mode
  - — Input Capture mode
- Idle Timer (T0)
- MICROWIRE/PLUS Serial Interface (SPI Compatible)
- Full Duplex USART
- Two Analog Comparators

I/O Features

- Software selectable I/O options (TRI-STATE® Output,Push-Pull Output, Weak Pull-Up Input, and High Impedance Input)
- Schmitt trigger inputs on ports G and L
- Eight high current outputs
- Packages: 28 SO with 24 I/O pins, 40 DIP with 36 I/O pins, 44 PLCC and PQFP with 40 I/O pins

Fully Static CMOS Design

- Low current drain (typically < 4 µA)
- Two power saving modes: HALT and IDLE

Temperature Range

- −40°C to +85°C

Development Support

- Windowed packages for DIP and PLCC
- Real time emulation and full program debug offered by MetaLink Development System

Block Diagram

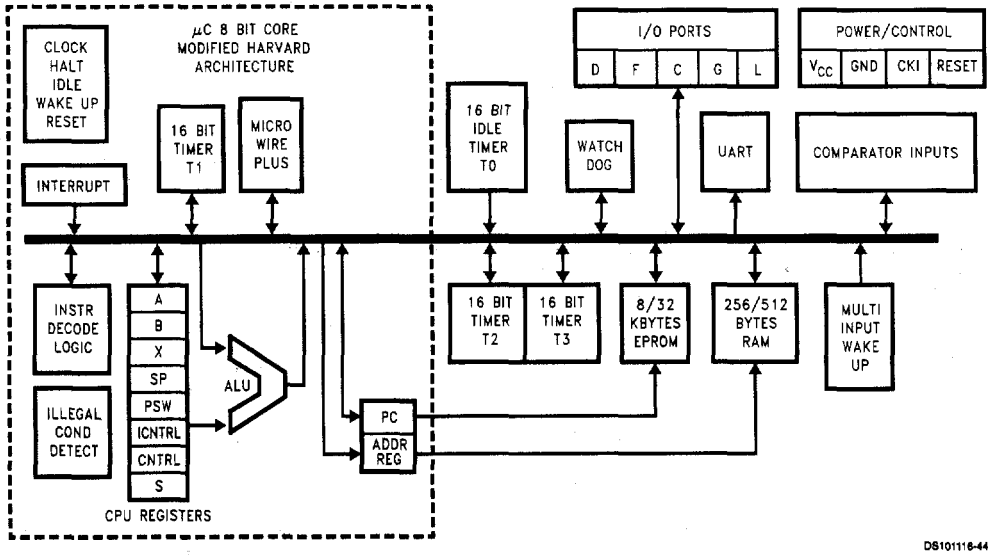


FIGURE 1. COP8FGx Block Diagram

1.0 Device Description

1.1 ARCHITECTURE

The COP8 family is based on a modified Harvard architecture, which allows data tables to be accessed directly from program memory. This is very important with modern microcontroller-based applications, since program memory is usually ROM or EPROM, while data memory is usually RAM. Consequently data tables need to be contained in non-volatile memory, so they are not lost when the microcontroller is powered down. In a modified Harvard architecture, instruction fetch and memory data transfers can be overlapped with a two stage pipeline, which allows the next instruction to be fetched from program memory while the current instruction is being executed using data memory. This is not possible with a Von Neumann single-address bus architecture.

The COP8 family supports a software stack scheme that allows the user to incorporate many subroutine calls. This capability is important when using High Level Languages. With a hardware stack, the user is limited to a small fixed number of stack levels.

1.2 INSTRUCTION SET

In today's 8-bit microcontroller application arena cost/performance, flexibility and time to market are several of the key issues that system designers face in attempting to build well-engineered products that compete in the marketplace. Many of these issues can be addressed through the manner in which a microcontroller's instruction set handles processing tasks. And that's why COP8 family offers a unique and code-efficient instruction set — one that provides the flexibility, functionality, reduced costs and faster time to market that *today's microcontroller based products require.*

Code efficiency is important because it enables designers to pack more on-chip functionality into less program memory space. Selecting a microcontroller with less program memory size translates into lower system costs, and the added security of knowing that more code can be packed into the available program memory space.

1.2.1 Key Instruction Set Features

The COP8 family incorporates a unique combination of instruction set features, which provide designers with optimum code efficiency and program memory utilization.

Single Byte/Single Cycle Code Execution

The efficiency is due to the fact that the majority of instructions are of the single byte variety, resulting in minimum program space. Because compact code does not occupy a substantial amount of program memory space, designers can integrate additional features and functionality into the microcontroller program memory space. Also, the majority instructions executed by the device are single cycle, resulting in minimum program execution time. In fact, 77% of the instructions are single byte single cycle, providing greater code and I/O efficiency, and faster code execution.

1.2.2 Many Single-Byte, Multifunction Instructions

The COP8 instruction set utilizes many single-byte, multifunction instructions. This enables a single instruction to accomplish multiple functions, such as DRSZ, DCOR, JID, LD (Load) and X (Exchange) instructions with post-incrementing and post-decrementing, to name just a few examples. In many cases, the instruction set can simultaneously execute as many as three functions with the same single-byte instruction.

JID: (Jump Indirect); Single byte instruction; decodes external events and jumps to corresponding service routines (analogous to "DO CASE" statements in higher level languages).

LAID: (Load Accumulator-Indirect); Single byte look up table instruction provides efficient data path from the program memory to the CPU. This instruction can be used for table lookup and to read the entire program memory for checksum calculations.

RETSK: (Return Skip); Single byte instruction allows return from subroutine and skips next instruction. Decision to branch can be made in the subroutine itself, saving code.

AUTOINC/DEC: (Auto-Increment/Auto-Decrement); These instructions use the two memory pointers B and X to efficiently process a block of data (analogous to "FOR NEXT" in higher level languages).

1.2.3 Bit-Level Control

Bit-level control over many of the microcontroller's I/O ports provides a flexible means to ease layout concerns and save board space. All members of the COP8 family provide the ability to set, reset and test any individual bit in the data memory address space, including memory-mapped I/O ports and associated registers.

1.2.4 Register Set

Three memory-mapped pointers handle register indirect addressing and software stack pointer functions. The memory data pointers allow the option of post-incrementing or post-decrementing with the data movement instructions (LOAD/EXCHANGE). And 15 memory-maped registers allow designers to optimize the precise implementation of certain specific instructions.

1.3 EMI REDUCTION

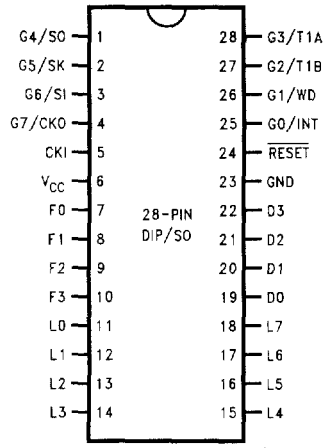
The COP8FGx5 family of devices incorporates circuitry that guards against electromagnetic interference — an increasing problem in today's microcontroller board designs. National's patented EMI reduction technology offers low EMI clock circuitry, gradual turn-on output drivers (GTOs) and internal I_{CC} smoothing filters, to help circumvent many of the EMI issues influencing embedded control designs. National has achieved 15 dB–20 dB reduction in EMI transmissions when designs have incorporated its patented EMI reducing circuitry.

1.4 PACKAGING/PIN EFFICIENCY

Real estate and board configuration considerations demand maximum space and pin efficiency, particularly given today's high integration and small product form factors. Microcontroller users try to avoid using large packages to get the I/O needed. Large packages take valuable board space and increases device cost, two trade-offs that microcontroller designs can ill afford.

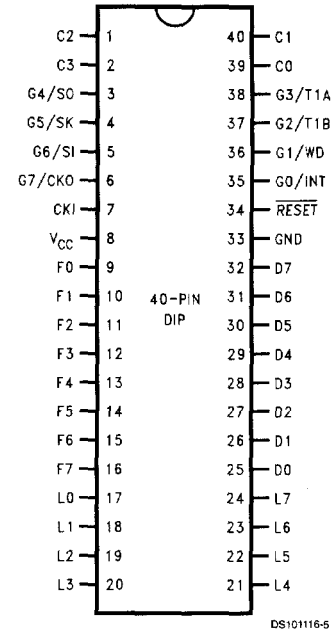
The COP8 family offers a wide range of packages and do not waste pins: up to 90.9% (or 40 pins in the 44-pin package) are devoted to useful I/O.

Connection Diagrams



Note 1: X = E for 8k, G for 16k,
H for 20k, K for 24k, R for 32k
Y = 5 for ROM, 7 for OTP

Top View
Order Number COP8FGXY28M8
See NS Package Number M28B
Order Number COP8FGXY28N8
See NS Package Number N28A
Order Number COP8FGR728Q3
See NS Package Number D28JQ



Top View
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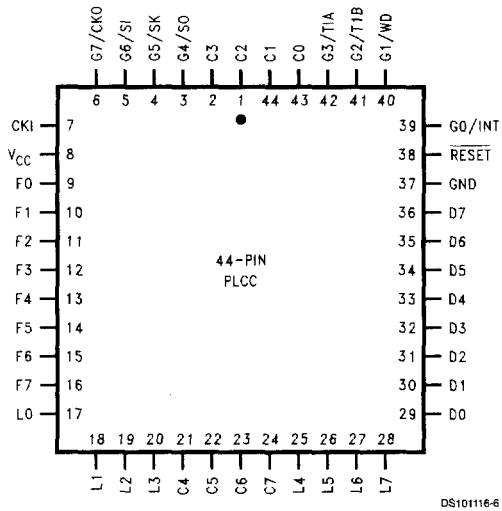
See NS Package Number N40A
Order Number COP8FGR540Q3
See NS Package Number D40KQ



Top View
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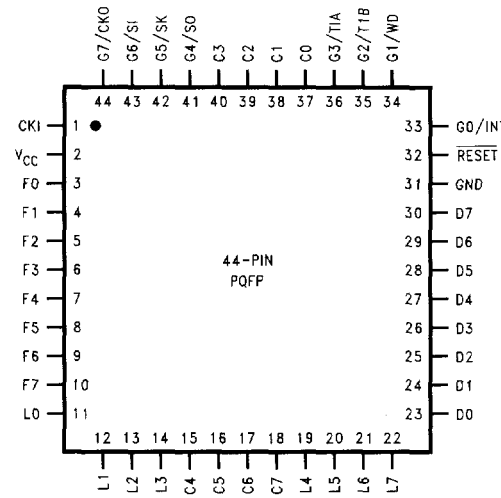
See NS Package Number V44A
Order Number COP8FGR744J3
See NS Package Number EL44C



Top View
Order Number COP8FGXYVEJ8
See NS Package Number VEJ44A

FIGURE 2. Connection Diagrams

Connection Diagrams (Continued)

Pinouts for 28 -, 40- and 44-Pin Packages

Port	Type	Alt. Fun	28-Pin SO	40-Pin DIP	44-Pin PLCC	44-Pin PQFP
L0	I/O	MIWU	11	17	17	11
L1	I/O	MIWU or CKX	12	18	18	12
L2	I/O	MIWU or TDX	13	19	19	13
L3	I/O	MIWU or RDX	14	20	20	14
L4	I/O	MIWU or T2A	15	21	25	19
L5	I/O	MIWU or T2B	16	22	26	20
L6	I/O	MIWU or T3A	17	23	27	21
L7	I/O	MIWU or T3B	18	24	28	22
G0	I/O	INT	25	35	39	33
G1	I/O	WDOUT*	26	36	40	34
G2	I/O	T1B	27	37	41	35
G3	I/O	T1A	28	38	42	36
G4	I/O	SO	1	3	3	41
G5	I/O	SK	2	4	4	42
G6	I	SI	3	5	5	43
G7	I	CKO	4	6	6	44
D0	O		19	25	29	23
D1	O		20	26	30	24
D2	O		21	27	31	25
D3	O		22	28	32	26
D4	O		29	33	27	
D5	O		30	34	28	
D6	O		31	35	29	
D7	O		32	36	30	
F0	I/O		7	9	9	3
F1	I/O	COMP1IN−	8	10	10	4
F2	I/O	COMP1IN+	9	11	11	5
F3	I/O	COMP1OUT	10	12	12	6
F4	I/O	COMP2IN−		13	13	7
F5	I/O	COMP2IN+		14	14	8
F6	I/O	COMP2OUT		15	15	9
F7	I/O			16	16	10
C0	I/O			39	43	37
C1	I/O			40	44	38
C2	I/O			1	1	39
C3	I/O			2	2	40
C4	I/O				21	15
C5	I/O				22	16
C6	I/O				23	17
C7	I/O				24	18
V_{CC}			6	8	8	2
GND			23	33	37	31
CKI	I		5	7	7	1
$\overline{\text{RESET}}$	I		24	34	38	32

* G1 operation as WDOUT is controlled by ECON bit 2.

2.1 Ordering Information

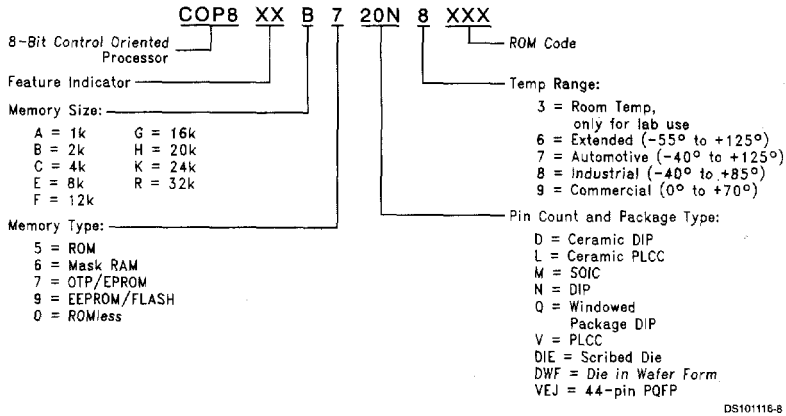


FIGURE 3. Part Numbering Scheme