

# TC5091AP

C<sup>2</sup>MOS DIGITAL INTEGRATED CIRCUIT  
SILICON MONOLITHIC

## TC5091AP PENTAPHASIC INTEGRATION 8-BIT A/D CONVERTER

The TC5091AP is a pentaphasic integration 8-bit A/D converter of high precision and low power consumption. The 8-bit output data can be taken out in the form of time-shared higher order 4 bits and lower order 4 bits on four 3-state data output. Either the higher order bits or the lower order bits can be selected by RSEL input. This output system is designed specifically considering interface to 4-bit CPU.

Further, since this converter has an analog multiplexer capable of selecting the input data up to six channels, an over-range flag, and a serial clock output function, it is used for a variety of applications.

### FEATURES:

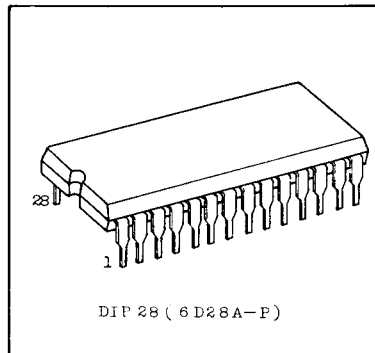
- High precision :  $\pm$ LSB(Max.)
- Low power consumption: 10mW(Typ.) @ ( $V_{DD}=5V$ ,  $f_{OSC}=1MHz$ )
- Single power supply :  $V_{DD}=5\pm 1.5V$
- High-speed conversion: 2ms(Max.) @  $f_{OSC}=1.5MHz$
- 6-channel analog multiplexer contained
- Reference clock oscillation circuit contained (CR oscillation)
- 3-state output with output latch
- TTL/CMOS compatible digital Input/Output
- Offset automatic correction

### APPLICATIONS:

- Various control instruments (for temperature, humidity, pressure, etc.)
- Home electric appliances
- Electrical wiring apparatuses
- Battery-driven instruments

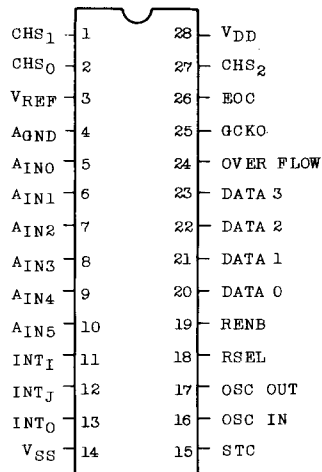
### ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	$V_{DD}$	$V_{SS}-0.5 \sim V_{SS}+8$	V
Input Voltage	$V_{IN}$	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	$V_{OUT}$	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Reference Supply Voltage	$V_{REF}$	$V_{AGND} \sim V_{DD}+0.5$	V
Analog Ground Voltage	$V_{AGND}$	$V_{SS}-0.5 \sim V_{REF}$	V
DC Input Current	$I_{IN}$	$\pm 10$	mA
Power Dissipation	$P_D$	300	mW
Operating Temperature Range	$T_{opr}$	-40 ~ 85	°C
Storage Temperature Range	$T_{stg}$	-65 ~ 150	°C



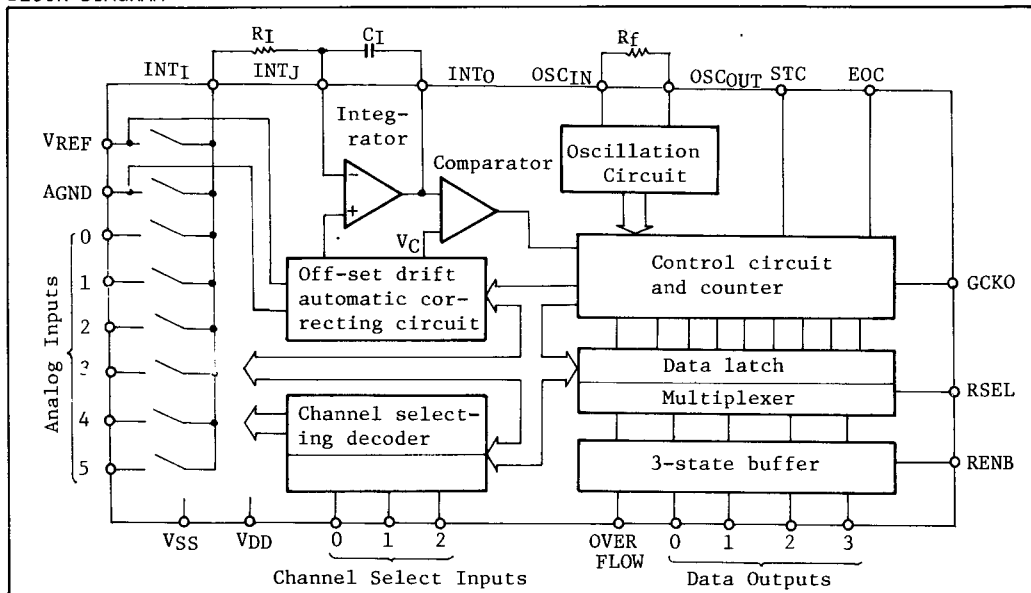
DIP 28 (6 D28A-P)

### PIN ASSIGNMENT

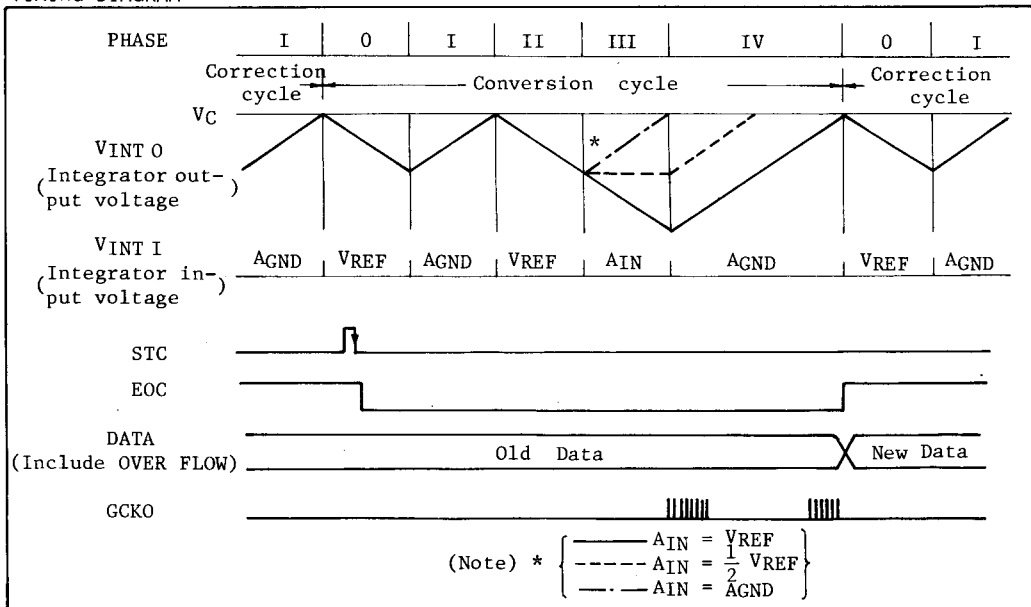


(TOP VIEW)

BLOCK DIAGRAM



TIMING DIAGRAM



## FUNCTION OF EACH PIN

PIN No.	SYMBOL	NAME & FUNCTION	PIN No.	SYMBOL	NAME & FUNCTION																																				
1	CHS 1	(Channel Select Inputs) Address inputs to select analog inputs, which consist of three terminals of CHS0 <sup>~</sup> 2. These select inputs are taken into the internal latch by the falling edge of STC inputs. Test mode should not be used.	16	OSC IN	I/O for reference clock oscillation. Clock oscillation can be made by means of external resistance. Clock can be supplied from outside through input of OSC IN.																																				
			17	OSC OUT																																					
2	CHS 0	TRUTH TABLE OF MULTIPLEXER <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>CHS2</th> <th>CHS1</th> <th>CHS0</th> <th>ON channel</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> <td>VREF*</td> </tr> <tr> <td>L</td> <td>L</td> <td>H</td> <td>AGND*</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> <td>AIN<sub>0</sub></td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>AIN<sub>1</sub></td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>AIN<sub>2</sub></td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> <td>AIN<sub>3</sub></td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> <td>AIN<sub>4</sub></td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> <td>AIN<sub>5</sub></td> </tr> </tbody> </table> * Test Conditions	CHS2	CHS1	CHS0	ON channel	L	L	L	VREF*	L	L	H	AGND*	L	H	L	AIN <sub>0</sub>	L	H	H	AIN <sub>1</sub>	H	L	L	AIN <sub>2</sub>	H	L	H	AIN <sub>3</sub>	H	H	L	AIN <sub>4</sub>	H	H	H	AIN <sub>5</sub>	18	RSEL	(Read Select) Input to select the higher order 4 bits or the lower order 4 bits to 4-bit data output. "H": Output of the higher order 4 bits. "L": Output of the lower order 4 bits.
			CHS2	CHS1	CHS0	ON channel																																			
			L	L	L	VREF*																																			
			L	L	H	AGND*																																			
			L	H	L	AIN <sub>0</sub>																																			
			L	H	H	AIN <sub>1</sub>																																			
			H	L	L	AIN <sub>2</sub>																																			
			H	L	H	AIN <sub>3</sub>																																			
			H	H	L	AIN <sub>4</sub>																																			
			H	H	H	AIN <sub>5</sub>																																			
19	RENB	(Read Enable) Data read signal. "H": The data 0 <sup>~</sup> 3 and overflow can be output. "L": The output above is at high impedance.																																							
3	VREF	(Reference Voltage) Reference voltage supplying terminal, which performs as full-scale voltage of AIN.	20	DATA 0	(3-state Parallel Data Outputs) Conversion data output. The data 0 is LSB, and the data 3 is MSB.																																				
			21	DATA 1																																					
			22	DATA 2																																					
			23	DATA 3																																					
4	AGND	(Analog Ground) Electrical potential to determine "zero point" of AIN.	24	OVERFLOW	In case of overrange or underrange, "H" level is output and the output is 3-state output.																																				
5	AIN 0	(Analog Input) Analog input terminals, by which AIN selected by CHS inputs are integrated. Input voltage range is AGND <sup>~</sup> VREF.	25	GCKO	(Gated Clock Output) Pulses of number equivalent to the conversion data are output during conversion (356 pulses at full scale)																																				
6	AIN 1																																								
7	AIN 2																																								
8	AIN 3																																								
9	AIN 4																																								
10	AIN 5																																								
11	INT I	(Integrator Input, Integrator Junction, Integrator Output) Integrator consists of external resistor R <sub>I</sub> and external capacitor C <sub>I</sub> .	26	EOC	(End of Conversion) Conversion endig signal. EOC goes to "L" level at the fall of STC, and returns to "H" level at the end of conversion.																																				
12	INT J																																								
13	INT O																																								
14	VSS	(Digital Ground) Normally 0V	27	CHS 2	(Channel Select Input) Refer to Pins 1 and 2.																																				
15	STC	(Start Conversion) Conversion starting signal. Conversion starts at the falling edge.	28	VDD	(Power Supply) 5V ± 1.5V																																				

## FUNCTIONAL DESCRIPTION

## (1) System Description (Pentaphasic Integration)

The operation of the TC5091AP is composed of the correction cycle and the conversion cycle as shown in the timing chart. While the power is switched on, the repetition of correction cycle and conversion cycle enables the TC5091AP to make A/D conversion under the optimum conditions at all times. The operation flowchart is shown in Fig. 1.

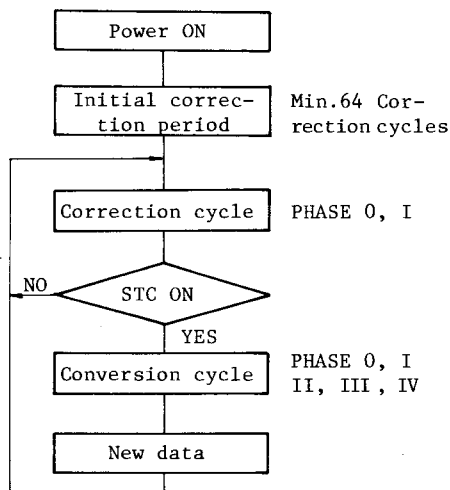


Fig. 1 Operation Flowchart

## (a) Initial correction period

The internal state of this LSI is reasonably unsettled at the time when the power is switched on; therefore, the initial correction cycle is required before stable converting operation becomes possible.

The correction cycle automatically corrects conversion error caused by offset voltage of the integrator or the like, and is composed of the period (PHASE 0) for which  $V_{REF}$  is integrated and the period (PHASE I) for which AGND is integrated.

Since system correction is performed in steps at the end of this PHASE I, 64 correction cycles ( $64 \times 1024 \cdot T_{OSC}$ ) are required as the initial correction period. ( $T_{OSC}$  denotes one clock cycle.)

(b) Conversion cycle

If the initial correction cycle period is completed, normal conversion becomes possible.

When STC input is given, (although the correction cycle in PHASE 0 or PHASE I is in operation at this time), the correction operation stops, and the conversion cycle starts.

In other words, even if STC input is given, this LSI performs the same operation as the correction cycle until PHASE I is completed; but it does not perform the correction at the time of completion of PHASE I, and shifts to PHASE II. Therefore, attention should be given to the fact that PHASE I prior to PHASE II does not act as correction cycle.

When STC input is given, the LSI integrates analog input in PHASE III through PHASE I and PHASE II, performing digital conversion in PHASE IV. When the LSI completes digital conversion in PHASE IV, the output is turned to the new data and the LSI returns to the correction cycle.

(c) Correction cycle

When the next STC input is given between completion of arbitrary conversion cycle (at the time of completion of PHASE IV) and completion of one correction cycle ( $1024 \cdot T_{OSC}$ ), no correction is substantially made. Therefore, in case the STC input is consecutively given, another STC should be given after the lapse of one correction cycle at the earliest from completion of PHASE IV. When the STC input is given during conversion (While EOC is at "L" level), the STC cannot be accepted.

(d) Constant of integration

The  $R_I$  and  $C_I$  composing the integrator should be selected to satisfy the following equation.

$$R_I C_I = (0.9 \sim 2.5) \cdot \frac{V_{REF}}{V_{DD}} \cdot \frac{10^3}{f_{OSC}} [S]$$

Attention should be paid to the fact that, when the external R oscillation is used,  $f_{OSC}$  has  $\pm 30\%$  variations in regard to the typ. value in Fig. 5 due to variations in sample and temperature characteristic.

In other words, if the typ. value in Fig. 5 is denoted by  $f_{R-TYP}$ , the  $R_I$  and  $C_I$  should be selected according to the following equation.

$$R_I C_I = (1.2 \sim 1.75) \cdot \frac{V_{REF}}{V_{DD}} \cdot \frac{10^3}{f_{R-TYP}} [S]$$

(2) Output Data Mode

TRUTH TABLE

RENB	ANALOG INPUT	DIGITAL OUTPUTS								OVER FLOW
		RSEL = "L"				RSEL = "H"				
		DATA 0	DATA 1	DATA 2	DATA 3	DATA 0	DATA 1	DATA 2	DATA 3	
L	Don't Care	High Impedance								
H	$\sim \frac{1}{2}LSB$	L	L	L	L	L	L	L	H	H
H	$\frac{1}{2}LSB \sim \frac{1}{2}LSB$	L	L	L	L	L	L	L	L	L
H	$\frac{1}{2}LSB \sim \frac{3}{2}LSB$	H	L	L	L	L	L	L	L	L
H	.....	Straight Binary								
H	"FS" - $\frac{5}{2}LSB \sim$ "FS" - $\frac{3}{2}LSB$	L	H	H	H	H	H	H	H	L
H	"FS" - $\frac{3}{2}LSB \sim$ "FS" - $\frac{1}{2}LSB$	H	H	H	H	H	H	H	H	L
H	"FS" - $\frac{1}{2}LSB \sim$	H	H	H	H	H	H	H	H	H

Note : • ACND = 0V                      • 1LSB = "FS"/256  
 • "FS" ..... Full Scale (=VREF)

8-bit digital data is output on four data lines after having been divided into the higher order 4 bits and the lower order 4 bits. Either the higher order bits or the lower order bits can be selected by RSEL.

### (3) System Clock Oscillation Circuit

For oscillating reference clock the oscillation circuit is composed of external resistors as shown in Fig. 2.

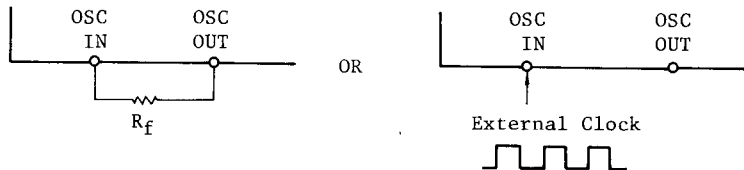


Fig. 2 Clock Supplying Methods

### (4) Timings for STC-EOC and EOC-DATA

- o Time ( $t_{SE}$ ) from the fall of STC to the fall of EOC.

$$t_{SE} = \frac{1}{2} T_{OSC} \sim \frac{3}{2} T_{OSC}$$

- o Time ( $t_{DE}$ ) from the out of DATA output to the rise of EOC

$$t_{DE} = \frac{1}{2} T_{OSC}$$

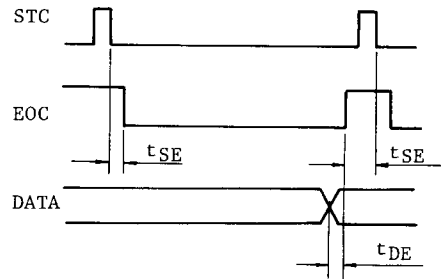


Fig. 3 Timing Chart of STC, EOC

- o Min. time ( $t_{ES}$ ) from the rise of EOC to the acceptance of another STC.

$$t_{ES} = \frac{1}{2} T_{OSC} \sim \frac{3}{2} T_{OSC}$$

(5) GCKO Output (Gated Clock Output)

During the conversion (PHASE IV), the pulses of number equivalent to the values of digital data can be obtained on GCKO output.

The output pulse has the frequency corresponding to four times of reference clock as shown in Fig. 4, and is synchronized with the rising edge of OSC OUT.

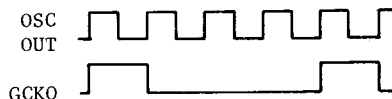


Fig. 4 Timing Chart of GCKO Output

(6) Timing for STC Input and CHS Input

STC signal is taken in synchronously with the internal clock. Therefore, if  $T_{OSC}$  denotes one clock cycle of OSC terminal, the pulse width of more than  $(2 \cdot T_{OSC})$  is required.

Since the data of  $CHS_{0\sim 2}$  are also latched in synchronously with the internal clock, the CHS signal at least requires the hold time of  $(T_{OSC} + 50ns)$  or more after the fall of STC.

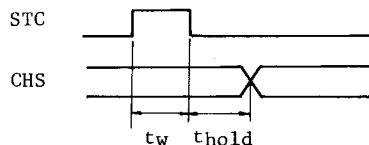


Fig.5 Timing Chart of Control Input

NOTE :  $t_w > 2 \cdot T_{OSC}, t_{hold} > T_{OSC} + 50ns$

## RECOMMENDED OPERATING CONDITIONS (V<sub>SS</sub> = 0V)

ITEM	SYMBOL		MIN.	TYP.	MAX.	Unit
Supply Voltage	VDD		3.5	5	6.5	V
Input Voltage	VIN		0	-	VDD	V
Reference Voltage	VREF		3	-	VDD	V
Analog Ground Voltage	VAGND		0	0	1	V
Integral Resistor	RI		0.4	-	2	MΩ
Integral Capacitor	CI	(Note)	-	-	-	-
Oscillatory Resistance	Rf	VDD = 5V	10	-	-	MΩ

Note: Refer to the operating consideration (1) for determining the values of RI and CI respectively.

The ripples of VDD and VREF should be held down to less than 1/256 of the respective absolute values in view of precision.

## ELECTRICAL CHARACTERISTICS (V<sub>SS</sub> = 0V)

ITEM	SYM-BOL	TEST CONDITION	VDD (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Output High Voltage	VOH	IOUT  < 1 μA VIN = VSS, VDD	5	4.95	-	4.95	5.00	-	4.95	-	V
Output Low Voltage	VOL	IOUT  < 1 μA VIN = VSS, VDD	5	-	0.05	-	0.00	0.05	-	0.05	V
Output High Current	IOH	VOH = 4.0V VIN = VSS, VDD *	5	-1.2	-	-1.0	-2.0	-	-0.7	-	mA
Output Low Current	IOL	VOL = 0.4V VIN = VSS, VDD *	5	2.4	-	2.0	4.0	-	1.6	-	mA
Input High Voltage	VIH	*	5	2.4	-	2.4	-	-	2.4	-	V
Input Low Voltage	VIL	*	5	-	0.8	-	-	0.8	-	0.8	V
Output Disable Current	IDH IDL	VOH = 6.5V VOL = 0V *	6.5	-	±0.5	-	±10 <sup>-4</sup>	±0.5	-	±5	μA
Input Current	I <sub>IH</sub> I <sub>IL</sub>	VIH = 6.5V VIL = 0V *	6.5	-	±0.3	-	±10 <sup>-5</sup>	±0.3	-	±1	μA
Analog Switch Input Leak Current	I <sub>OFF</sub>	VIH = 6.5V VIL = 0V	6.5	-	±0.3	-	±10 <sup>-5</sup>	±0.3	-	±1	μA
Operating Consumption Current	IDD (opr.)	fOSC = 1 MHz	5	-	-	-	1.8	3	-	-	mA
Reference Supply Consumption Current	I <sub>REF</sub>	VREF = 5V AGND = 0V	5	-	-	-	0.3	0.6	-	-	mA

\* Applicable to digital input/output. Not applicable to analog input/output and OSC<sub>IN</sub>/OSC<sub>OUT</sub>.

SWITCHING CHARACTERISTICS (V<sub>DD</sub> = 5V, V<sub>SS</sub> = 0V, T<sub>a</sub> = 25°C, C<sub>L</sub> = 50pF)

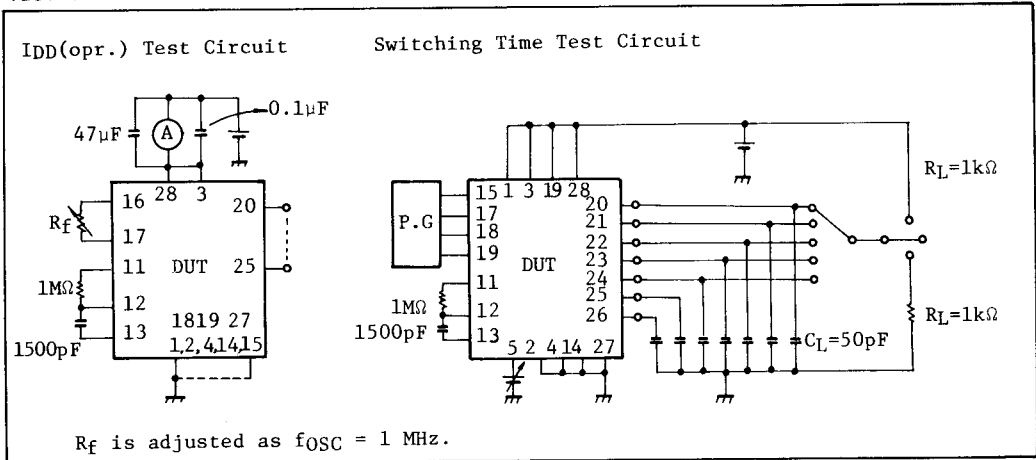
ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t <sub>TLH</sub>		-	50	100	ns
Output Fall Time	t <sub>THL</sub>		-	40	100	
(Low-High) Propagation Delay Time	t <sub>pLH</sub>	OSC <sub>OUT</sub> -GCKO	-	200	400	
(High-Low) Propagation Delay Time	t <sub>pHL</sub>		-	150	400	
(Low-High) Propagation Delay Time	t <sub>pLH</sub>	RSEL("L"→"H")-DATA OUT	-	180	400	
(High-Low) Propagation Delay Time	t <sub>pHL</sub>		-	150	400	
(Low-High) Propagation Delay Time	t <sub>pLH</sub>	RSEL("H"→"L")-DATA OUT	-	380	700	
(High-Low) Propagation Delay Time	t <sub>pHL</sub>		-	300	700	
Output Enable Time	t <sub>ZL</sub> t <sub>ZH</sub>		-	80	250	
Output Disable Time	t <sub>LZ</sub> t <sub>HZ</sub>		-	280	500	
Max. Clock Frequency	f <sub>MAZ</sub> ∅	OSC Input	1.5	3.0	-	
Min. Clock Frequency	f <sub>MIN</sub> ∅	OSC Input	-	-	100	kHz
Input Capacity	C <sub>IN</sub>	Digital Input	-	4	-	pF
Analog Input Capacity	C <sub>IN</sub>	A <sub>0</sub> ~ A <sub>5</sub>	-	7	-	pF
3-State Output Capacity	C <sub>OUT</sub>		-	8	-	pF

SYSTEM CHARACTERISTICS (T<sub>a</sub> = -40 ~ 85°C)

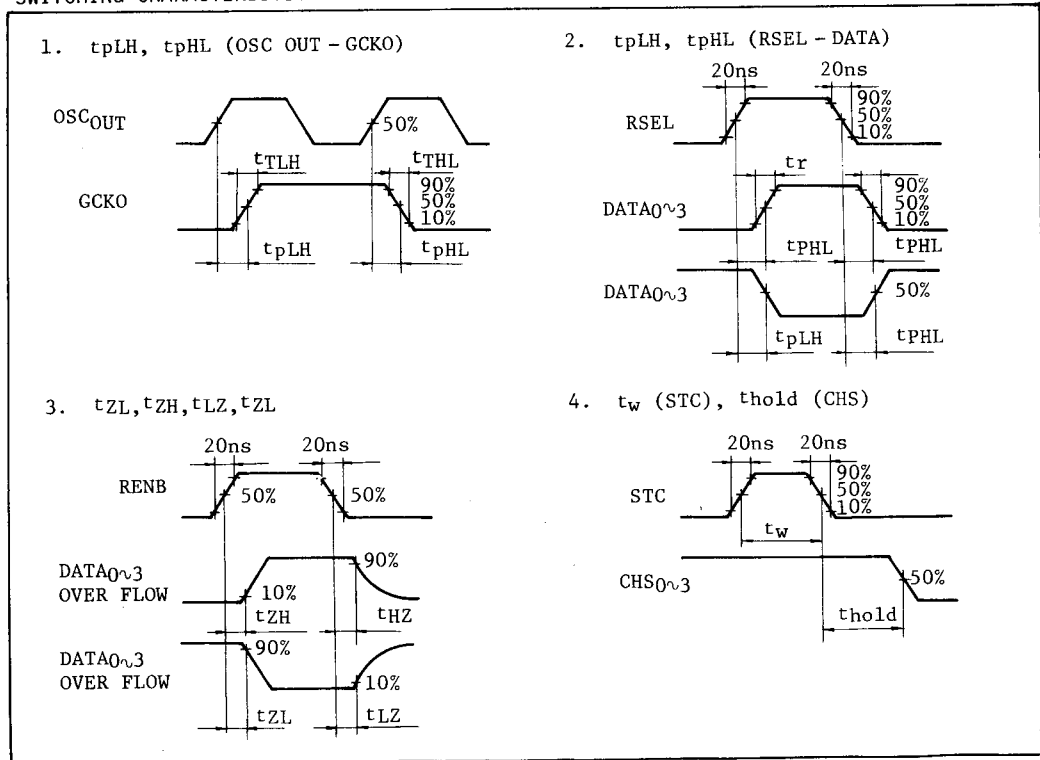
ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Zero Point Error	E <sub>ZP</sub>	V <sub>REF</sub> = V <sub>DD</sub> = 5V V <sub>AGND</sub> = 0V	-	± 1/4	± 1/2	LSB
Full Scale Error	E <sub>FS</sub>		-	± 1/4	± 1	
Nonlinearity			-	± 1/4	± 1	
STC Min. Pulse Width	t <sub>w</sub>		-	-	2 / f <sub>OSC</sub>	s
CHS Min. Hold Time	t <sub>hold</sub>	STC = CHS <sub>0</sub> ~2	-	-	10 / f <sub>OSC</sub> + 50	ns
Conversion Time	t <sub>conv.</sub>	A <sub>IN</sub> = 0 ~ FS	10 <sup>3</sup> / f <sub>OSC</sub>	-	3.1x10 <sup>3</sup> / f <sub>OSC</sub>	s

\* f<sub>OSC</sub> : OSC terminal clock frequency [Hz], FS : Full Scale voltage, V<sub>DD</sub> level

## TEST CIRCUIT



## SWITCHING CHARACTERISTICS TEST WAVEFORMS



STANDARD CHARACTERISTICS CHARTS

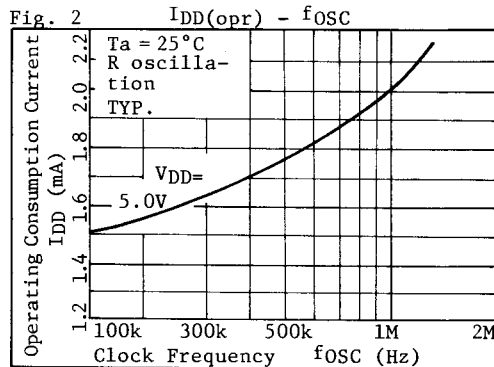
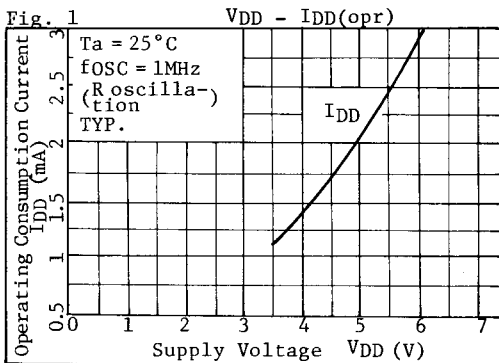


Fig. 3 P-channel Output Buffer Drain Current Characteristics

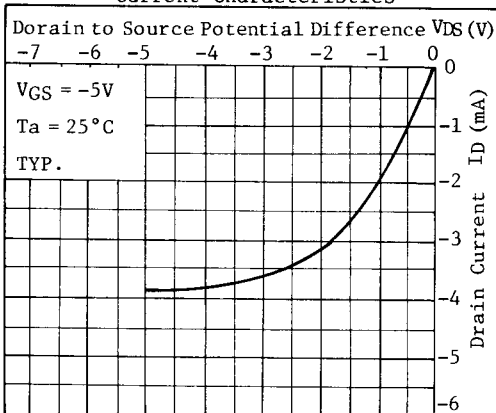


Fig. 4 N-channel Output Buffer Drain Current Characteristics

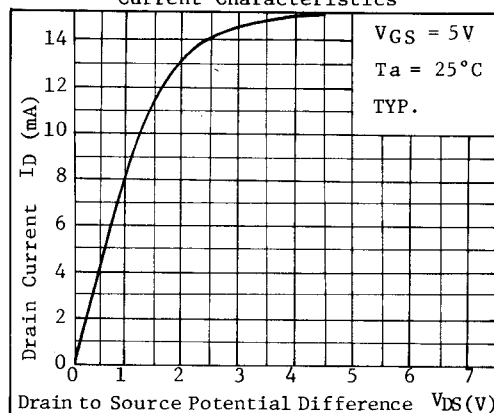


Fig. 5  $R_f - f_{osc}$

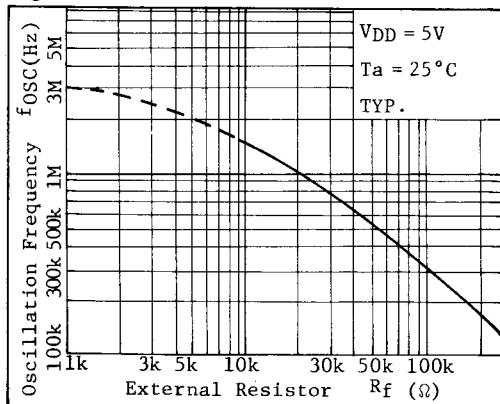


Fig. 6  $f_{osc} - V_{DD}$

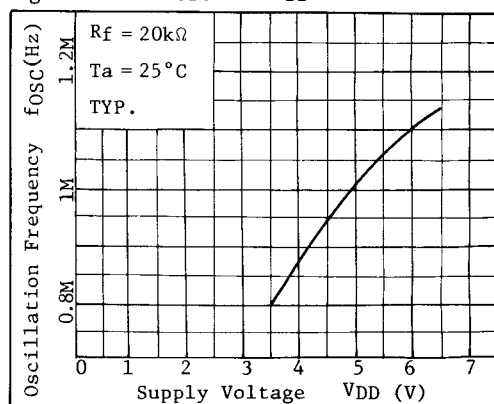


Fig. 7  $t_{pd} - V_{DD}$  (RENB-DATA)

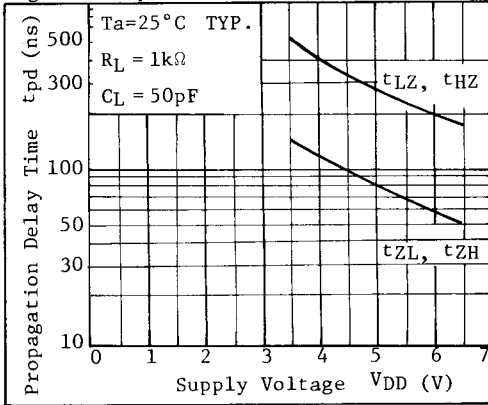


Fig. 8  $t_{pd} - V_{DD}$  (RSEL (L→H)-DATA)

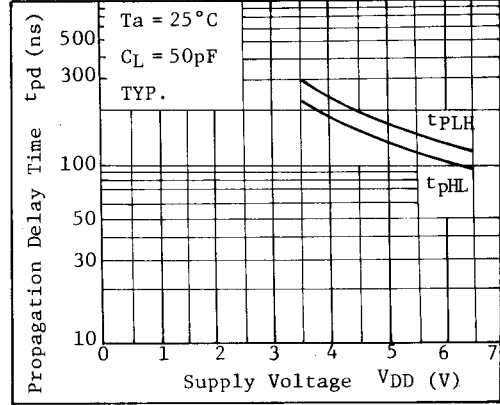


Fig. 9  $t_{pd} - V_{DD}$  (RSEL (H→L)-DATA)

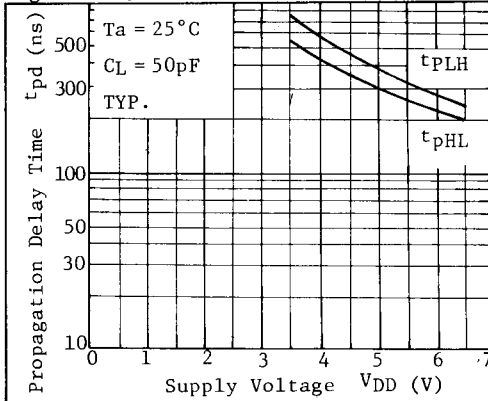


Fig. 10  $t_{pd} - V_{DD}$  (OSCOU - GCKO)

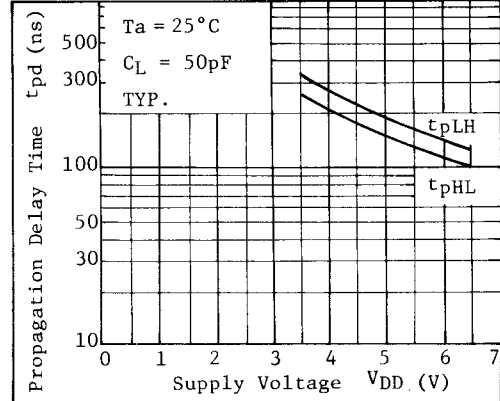
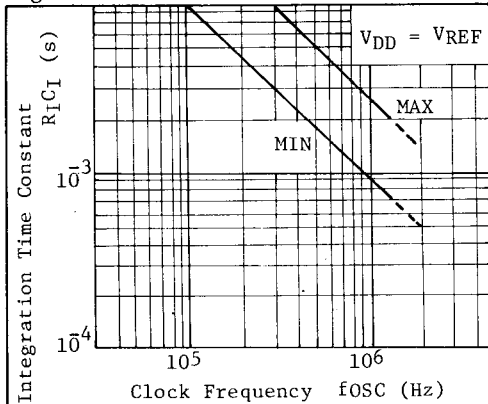


Fig. 11  $R_I C_I - f_{OSC}$



(Note)

The characteristics at left have been prepared for reference at the time of determination of an integrator time constant according to the equation of

$$(R_I C_I = (0.9 \sim 2.5) \cdot \frac{V_{REF}}{V_{DD}} \cdot \frac{10^3}{f_{OSC}} \text{ (s)})$$

for determining  $R_I \cdot C_I$ .

In case of the determination of  $R_I$  and  $C_I$ , the product, or the value, of  $R_I$  and  $C_I$  is required to be within the range of MIN. to MAX. as shown in left figure after due consideration of dispersion.