MAS6116

Stereo Digital Volume Control

- **Signal Voltage up to ± 18V**
- **Gain range from -111.5dB to +15.5dB**
- **Small step sizes 0.5dB**
- **THD 0.0002% in balanced mode**
- **SNR 124dB in balanced mode**

DESCRIPTION

MAS6116 is an ultra low noise stereo volume control IC for high end audio systems. It can work with input signals as high as ± 18 V but operates from a single +5V supply with minimal power.

It has a serial interface that controls two audio channels independently. The gain of each channel can be programmed from -111.5dB to +15.5dB in small 0.5dB steps. It is highly linear, especially in single channel balanced configuration with just 0.0002% THD.

Audible “Clicks” on gain changes are eliminated by changing gains only during a zero crossing in the input signal.

A peak detection circuit allows easy monitoring of the output signal.

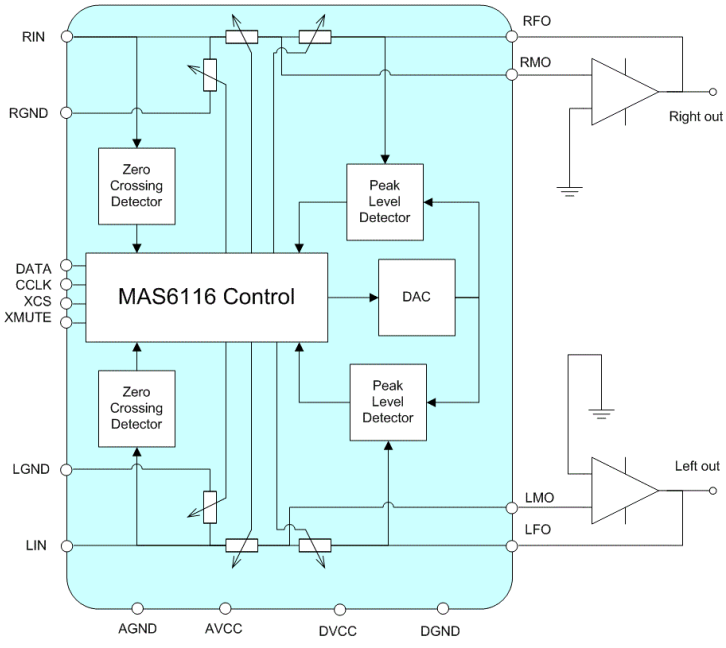
The MAS6116 is available in a 16 pin SOIC package. Its performance is guaranteed over a temperature range of -30°C to +85°C.

FEATURES

- Input signal voltage up to ± 18V
- Gain range from -111.5dB to +15.5dB
- Small and equal gain step size 0.5dB
- 0.0002% THD in balanced mono configuration
- Dynamic range 121 dB stereo configuration
- Two independent channels
- Zero cross detection for gain changes
- Power on/off transient suppression
- Signal peak level detection with adjustable reference
- Instant gain change option
- Hardware and software mute function
- Single +5V operation
- Low power consumption 12mW

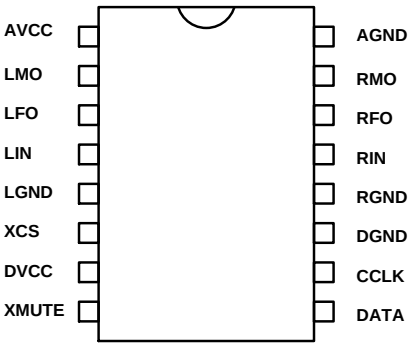
APPLICATION

- High End Audio Systems
- Consumer Audio /Entertainment Systems
- Mixing Desks
- Audio Recording Equipment



PIN CONFIGURATIONS

SO16



PIN DESCRIPTION

Pin Name	Pin SO16	Type	Function
AVCC	1	P	Power Supply, for Analog
LMO	2	AI	External Amplifier Negative Input (Left)
LFO*	3	AI	Feedback Signal from External Amplifier Output (Left)
LIN*	4	AI	Input, Left Channel
LGND	5	AI	Signal Ground, Left Channel
XCS	6	DI	Chip Select Input of Serial Interface
DVCC	7	P	Power Supply, for Digital
XMUTE	8	DI	Mute Input
DATA	9	DIO	Data Input and Output of Serial Interface, Tristate
CCLK	10	DI	Clock Input of Serial Interface
DGND	11	G	Ground for Digital
RGND	12	AI	Signal Ground, Right Channel
RIN*	13	AI	Input, Right Channel
RFO*	14	AI	Feedback Signal from External Amplifier Output (Right)
RMO	15	AI	External Amplifier Negative Input (Right)
AGND	16	G	Ground for Analog

P = Power supply, G = Supply ground, A = Analog, D = Digital, I = Input, O = Output
*) Note: These pins have limited ESD protection. See *Absolute Maximum Ratings* on page 10 for further details.

GENERAL DESCRIPTION

Main features

The MAS6116 is designed for high-end audio systems that require high output voltages. In many audio preamplifiers it's an advantage to get a lot of voltage swing out from the unit, close to +/-15V signal levels. In most competing devices an op-amp is needed after the volume controller to get these levels since the IC can not work with those high input signal levels. For such a system not only the signal is amplified but the noise as well. With the MAS6116 high signal levels can be used everywhere inside the pre-amplifier and MAS6116 can then operate with input signals up to +/- 18V and used as an attenuator. Very little noise usually comes out from the pre-amplifier and the beauty is that the noise depends on the volume level. When listening at a lower volume levels the noise is always inaudible. To improve the system performance even further the MAS6116 can be used in a balanced configuration with one MAS6116 per channel.

The levels of the left and right analog channels are set by the serial interface. Both channels can be programmed independently. The channel gains can be programmed from -111.5 dB to +15.5 dB with 0.5 dB resolution. The code for -112 dB (00_{HEX}) activates mute for maximum attenuation. MAS6116 operates from a single +5V supply and accepts analog input signal levels up to ±18V.

MAS6116 has a zero cross detect function that changes the channel gain only when a zero crossing has been detected in the input signal. This eliminates clicking sounds from the output signal when the gain is changed. The zero cross detection circuit is also equipped with a timeout function to make sure the gain value is updated even when there is no input signal.

Channel gains can also be changed instantly without using the zero cross detect function. This can be done with dedicated instant gain change commands specified in *Register Description* on page 8. Using this feature to change channel gains in large increments is not recommended because it may cause large transients in the output signal. See chapter *Changing the gain of the channels* and chapter *Write operation status register* for further details.

The XMUTE pin in MAS6116 always uses the zero cross detection and timeout functions when entering to or returning from the MUTE state. This prevents fast transients from occurring in the output signal.

Serial interface

Control information is written into or read back from the internal register via the serial control port. The serial control port consists of a bi-directional pin for data (DATA), chip select pin (XCS) and control clock (CCLK) and supports the serial communication protocol. All control instructions require two bytes of data; address byte and control/data byte. The bits in the address and control/data byte are always written and read MSB bit first.

To shift the data in CCLK must be pulsed 16 times when XCS is low. The data is shifted into the serial input register on the rising edges of CCLK pulses. The first 8 bits contain address information. The second byte contains the control word. XCS must return to high after the second byte. That is, after the 16th CCLK XCS must be returned to high. See chapter Serial interface timing diagram on page 14. See also figure 1 example of serial interface signals during Normal write to both channels (command CBh=%1100 1011, don’t care bits 1) with written byte AAh=%1010 1010.

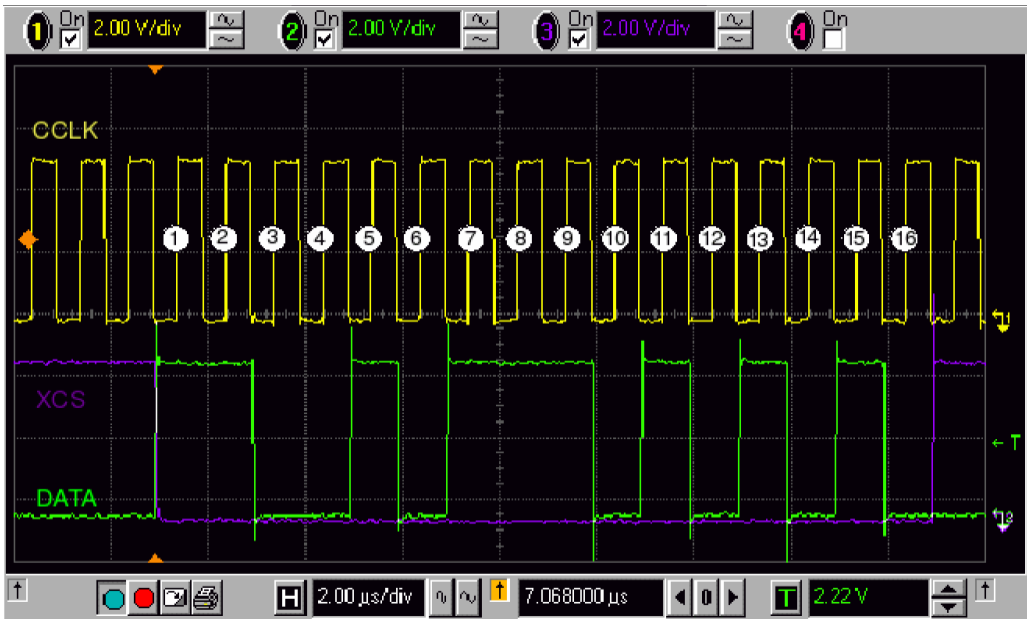


Figure 1. Normal write to both channels (command CBh=%1100 1011, don't care bits 1) with written byte AAh=%1010 1010.

The same process takes place for reading the information. XCS will remain low for next 16 CCLK pulses. The first 8 bits containing read address are shifted in on the rising edges of the 8 CCLK pulses. MAS6116 starts to drive first read bit to DATA line at falling edge of the 8th CCLK pulse. Thus controller should release the DATA line between rising and falling edges of the 8th CCLK pulse to avoid race situation. The controller can read the bits on the rising edge of CCLK pulses. The first bit is read on the rising edge of the 9th CCLK pulse. MAS6116 shifts a new bit to DATA line at each new falling edge of the CCLK line. The last bit is read on the rising edge of the 16th CCLK pulse. After minimum hold time (THLCHS) the XCS must be returned to high. When XCS is high, the DATA pin is in high impedance state, which enables DATA pins of other devices to be connected together. See figure 2 example of serial interface signals during Read left channel (command EFh=%1110 1111, don't care bits 1) with read byte AAh=%1010 1010.

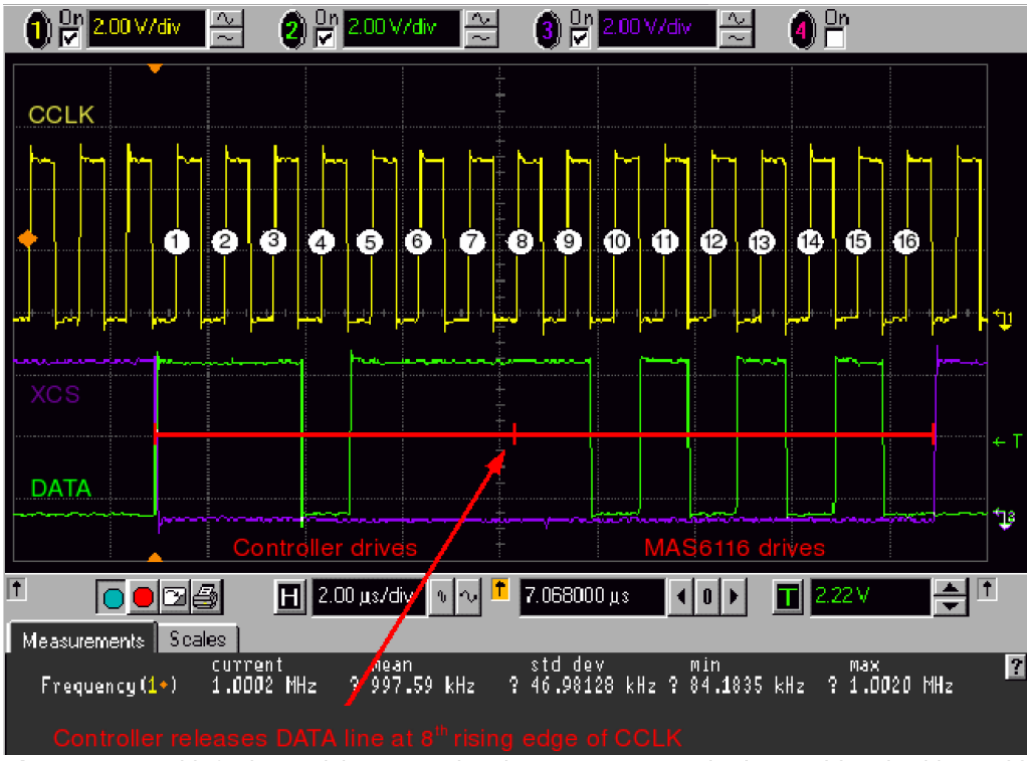


Figure 2. Read left channel (command EFh=%1110 1111, don't care bits 1) with read byte AAh=%1010 1010.

On the PCB board the same DATA and CCLK lines can be routed to every MAS6116 chip. If the XCS-pin is not active (low), DATA pin of that chip is in high-impedance state. This allows using a simple PCB board for multi-channel audio systems.

The device may be operated with a constant CCLK signal (see figure 1 and 2 examples), or the CCLK signal may be stopped between commands (see figure 3). The CCLK signal may be stopped in either high or low state. If the CCLK is stopped between commands, care must be taken to ensure that the chip receives exactly 16 rising clock edges while XCS is low and that there are no timing violations. See figure 3 signal example of Normal write to both channels (command 48h=%0100 1000, don't care bits 0) with written byte E0h=%1110 0000 and having the CCLK is stopped between commands.

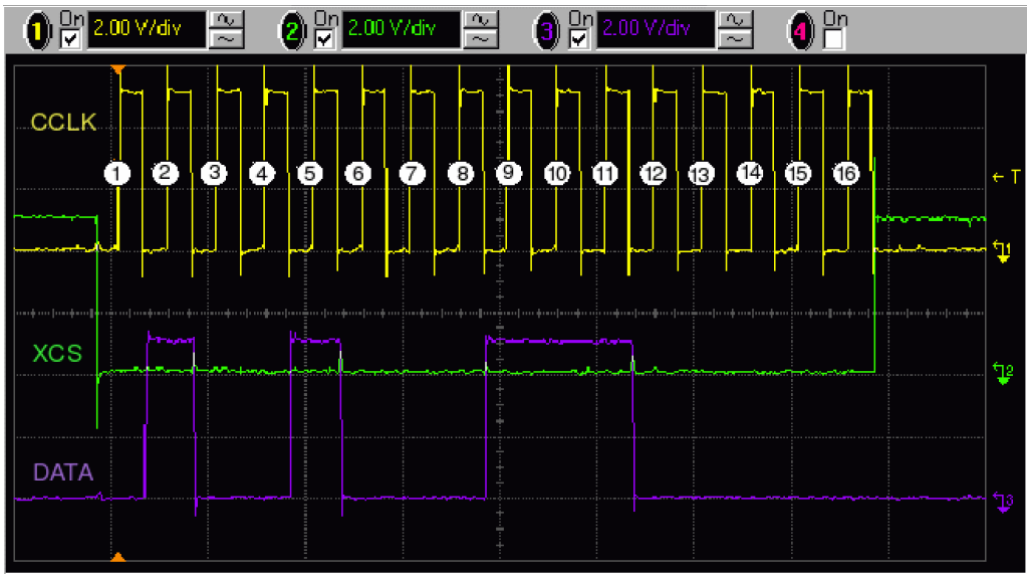


Figure 3. Normal write to both channels (command 48h=%0100 1000, don't care bits 0) with written byte E0h=%1110 0000 and the CCLK is stopped between commands.

The write command 48h in figure 3 is ambiguous with command CBh in figure 1 since their only difference is selecting don't care bits 0 or 1 respectively.

GENERAL DESCRIPTION

Operating modes

When power is first applied, the Power-On Reset circuit (POR) initializes the control registers and sets MAS6116 into mute state, ignoring the state of the XMUTE pin. The activation of the device requires that XMUTE pin is high and a control byte with a greater than the default value (00_{HEX}) is written in the gain register. It is possible to return to the mute state either by setting XMUTE pin low or writing zero (00_{HEX}) to the gain register. Setting the XMUTE pin low will mute both channels. Setting the XMUTE pin back high will return the channels to previously written gain values. The zero cross detector function is used when entering and returning from the mute state to prevent large transients in the output signal (see chapter *Changing the gain of the channels*).

The device has a special test mode register, which is used only for internal testing of the device. It is strongly recommended not to change the default value (00_{HEX}) of the test register during normal operation. For device testing the XMUTE pin is bi-directional. When the test register bit 1 is set to high, XMUTE pin is in output mode. In the test mode internal signals can be directed to the XMUTE pin. Note: In the test mode both analog outputs are in mute state and the device will not allow new gain values to be written in the gain registers. An exception to this is the force latch command specified in table *Test Register CR5 Description*, which can be used to instantly change the gain of both channels. This function is intended to be used in the test mode only, and it is recommended to use the commands specified in *Register Description* to instantly change the channel gains.

Changing the gain of the channels

When a new gain value is written to the gain register the device will activate the zero crossing detection and delay generator for the selected channel. MAS6116 will wait until a rising edge of the input signal is detected to change the gain value. This is done to ensure that no audible clicks are produced to the output signal during the gain change operation. The zero cross detection circuit has also a timeout delay generator that will force the gain change. The delay generator generates a typical delay of 22 ms.

If a new gain value is written before the previous write operation has finished, the previously written value will be overwritten and will not be set to the output. If it is desired that each gain value is set to the output, it is recommended to read the status bit from the write operation status register (CR6) or wait for at least 30 ms before the next gain change instruction.

Both channels can be programmed independently with separate commands. In this case the gain values will be set to the output in the order of writing. Both channels can also be programmed to the same value by writing only one instruction (see the *Register Description* on page 8).

Note: Due to the input signal dependency of the zero cross detection circuits the order of the gain changes may differ from the order of writing to the registers if the input signals to the channels are different. This applies to all instructions that use the zero cross detection and timeout functions, i.e. instructions that are not labeled as “instant” in the register description.

The new gain value can be set instantly to the output by using the instant gain change function. By using this command function the gain is set to the output instantly after the write operation has finished, without waiting for a zero cross to occur in the input signal or a delay to pass. The gains can be set independently to both channels using different commands, or both channels can be set to the same gain value by using a single command. Using the instant gain change function to change the gain value in larger than 0.5 dB steps may produce audible clicks to the output signal.

GENERAL DESCRIPTION

Peak level detection

MAS6116 has a 8-bit digital-to-analog converter (DAC) used to monitor the peak level of the output signal. The reference value is programmed using the serial interface and the same reference value is used for both channels. The reference value V REF can be calculated using the following formula.

VREF = (0.0036 + 0.0145 · CODE) · AVCC

where CODE is the decimal value of the control byte (0...255) and AVCC is the analog supply voltage of the MAS6116 device. With nominal analog supply voltage of 5V the reference value is

VREF = 18mV + 72.5mV · CODE

When a positive peak signal level at the output exceeds the V REF value, bits 0 and 1 of the status register are set (see register description). When set, the register contents will remain high until the value of the status register has been read.

Write operation status register

MAS6116 features a status register that can be used to determine if the channel registers are ready to accept new gain values. The status register bits 0 and 1 are set high at the start of a gain write operation, and are set back low when the new gain value has been set to the output. This happens when a positive zero crossing is detected in the input signal or the timeout delay has passed.

It is allowed to write a new gain value to a channel that is busy (i.e. waiting for a zero cross in the input signal). The new value will overwrite the previous one and the timeout delay will be reset. This means that the previously written gain value will not be set to the channel gain registers. To prevent this from happening it is recommended to read the write operation status register prior to setting a new gain value to determine if the write operation can be safely executed.

REGISTER DESCRIPTION

Register	Address Byte								Data Byte	
	7	6	5	4	3	2	1	0	msb…lsb	Function
Write Operation Status CR6	X	1	0	1	0	R	X	X	Output code 00000000 00000001 00000010 00000011	 Both channels ready Right channel busy Left channel busy Both channels busy
Peak Detector Status CR4	X	1	0	1	1	R	X	X	Output code 00000000 00000001 00000010 00000011	 No overload Right overload Left overload Both overload
Peak Detector Reference CR3	X	1	1	0	0	R/W	X	X	Input code 11111111 11111110 11111101 • • 00000010 00000001 00000000	DAC output, Note 1. VREF(255) VREF(254) VREF(253) • • VREF(2) VREF(1) VREF(0)
Left Channel Gain CR2	X	1	1	0	1	R/W	X	X	Input code 11111111 11111110 11111101 • • 11100000 00000010 00000001 00000000	Gain dB +15.5 +15.0 +14.5 • • 0.0 -111.0 -111.5 Mute
Right Channel Gain CR1	X	1	1	1	0	R/W	X	X	Input code 11111111 11111110 11111101 • • 11100000 00000010 00000001 00000000	Gain dB +15.5 +15.0 +14.5 • • 0.0 -111.0 -111.5 Mute
Test Mode, CR5	X	1	1	1	1	R/W	X	X	Reserved	
Normal Write, Both	X	1	0	0	1	W	X	X	Write to both gain registers	
Instant Write, Left (CR2)	X	0	1	0	1	W	X	X	Instant gain set to left channel	
Instant Write, Right (CR1)	X	0	1	1	0	W	X	X	Instant gain set to right channel	
Instant Write, Both	X	0	1	1	1	W	X	X	Instant gain set to both channels	

Note 1. Reference voltage is calculated from VREF = (0.0036 + 0.0145 • CODE) • AVCC

Address byte bits:

- Bit 2 is read/write bit (1=read, 0=write).
- Bits marked as X are don't care bits.
- The instant write commands write values to CR1 and CR2 registers for right and left channels respectively. These values can be read by using the specified read commands for CR1 and CR2 registers.

Data byte bits:

- All registers are set to their default values 00_{HEX} except CR3 which is set to FF_{HEX} during power-on reset.
- Default value for all bits is zero (00_{HEX}).

POWER-ON RESET

MAS6116 has a Power-On Reset circuit (POR) that ensures that the circuit is set to a known state when power is applied. The device can be activated as described in chapter *Operating modes* after the POR delay has passed.

In addition MAS6116 has a supply voltage monitoring circuit that monitors the digital supply voltage (DVCC) level. If the digital supply voltage drops below the specified level, the circuit is set to RESET state. The voltage monitoring circuit is functional only when sufficient analog supply voltage (AVCC) is present.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POR delay	T_{POR}	From DVCC=5V to POR rising edge		450		µs
Monitored DVCC level	V_{mon}	Measured from DGND		2.8		V
AVCC level to enable DVCC monitoring	V_{AVCC}	Measured from AGND	2.5			V

ABSOLUTE MAXIMUM RATINGS

All voltages with respect to ground.

Parameter	Symbol	Conditions	Min	Max	Unit
Signal Voltage	RIN, RFO, LIN, LFO		-20	+20	V
Positive Supply Voltage	AVCC, DVCC		-0.5	+6.0	V
All other pins	DATA, CLK, XCS, XMUTE	Note 2.	-0.3	AVCC +0.3	V
Storage Temperature	TS		-55	+125	°C
Operating Temperature	TA		-40	+95	°C
ESD Rating (JEDEC JS-001-2017)	V_{HBM}	Pins 3 (LFO), 4 (LIN), 13 (RIN) and 14 (RFO)	500		V
		All other pins	1000		

Note 2. Pin voltage must not exceed +6V under any circumstances.
Operation at maximum conditions will not damage the part but performance cannot be guaranteed. Stresses beyond those listed may cause permanent damage to the device.

RECOMMENDED OPERATION CONDITIONS

(AVCC=+5.0 V, AGND=0 V, TA=+25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal Voltage	RIN, RFO, LIN, LFO		-18		+18	V
Virtual Ground Voltage	RMO, LMO		-0.1	0	+0.1	V
Positive Supply Voltage	AVCC,DVCC		4.5	5	5.5	V
Negative Supply Voltage	AGND,DGND			0		V
Signal Grounds	LGND,RGND			0		V
Operating Temperature	TA		-30	+25	+85	°C

ANALOG CHARACTERISTICS

◆ Analog Inputs/Outputs

(AVCC=+5.0 V, AGND=0 V, TA=+25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input impedance	RIN	Average impedance, note 3.	7	10	13	kΩ
Input capacitance	CIN	For any gain value		2		pF
Input offset voltage	VIH	External OpAmp, Gain = 15.5 dB Note 4.		0.23		mV
Supply current	IVCC	AVCC+DVCC		0.6	2.2	mA
Power supply rejection ratio[1]	PSRR	From AVCC		80		dB

Note 3. Average input impedance is calculated as an average of the impedance measured for all gain values.
Note 4. Output offset voltage depends on external opamp and selected gain. Low input offset voltage and input bias current opamp is recommended to be used for minimum output offset.

ANALOG CHARACTERISTICS

◆ Gain Control

(AVCC=+5.0 V, AGND=0 V, TA=+25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Gain range	G		-111.5		+15.5	dB
Step size	D			0.5		dB
Absolute gain	GABS	Absolute gain value with setting G=255	+15	+15.5	+16	dB
Gain step error	DE	Relative to GABS, note 5.	-0.5	0	0.5	dB
Gain match error[1]	ME	Between channels, note 6.	-0.2	0	0.2	dB
Mute attenuation	MATT	AC measurement	96			dB

Note 5. Gain value for each gain setting is measured as AC measurement relative to GABS assuming a gain step size of 0.5dB. Gain settings 65…255 are tested in production. Gain error for lower gain settings is guaranteed by design only.
Note 6. Gain mismatch is tested in production for gain settings 90…255. Mismatch for lower gain settings is guaranteed by design only.

◆ Audio Performance

(AVCC=+5.0 V, AGND=0 V, TA=+25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Noise	N	Vin = 0V, Vout with OP2277, A-weighting gain=0dB gain=-40dB gain=-60dB gain=mute		 11 3.7 2.2 1.8		µVrms
Total harmonic distortion of balanced circuit	THD_{BAL}	Vin=1Vrms, gain=0dB, fin=1kHz		0.0002		%
		Vin=0.5Vrms, gain=0dB, fin=1kHz		0.0003		%
Total harmonic distortion of unbalanced circuit	THD	Vin=1Vrms, gain=0dB, fin=1kHz		0.0063		%
		Vin=0.5Vrms, gain=0dB, fin=1kHz		0.0034		%
Dynamic Range	DR	A-weighted Noise, gain=0dB unbalanced circuit balanced circuit		 121 124		dB
Crosstalk	CR	Between channels, Vin = 5Vrms, gain= 0dB, fin = 1kHz	-100			dB

ANALOG CHARACTERISTICS

◆ Peak Level Detection

(AVCC=+5.0 V, AGND=0 V, TA=+25ºC unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Peak detector minimum level	VMIN	PD reference = 0	0	18	500	mV
Peak detector maximum level	VMAX	PD reference = 255	18	18.5	20	V
Peak detector step size	VSTEP		60	72.5	90	mV

◆ Zero Cross Detection Timeout

(AVCC=+5.0 V, AGND=0 V, TA=+25ºC unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Zero cross detection timeout	TDEL		15	22	30	ms

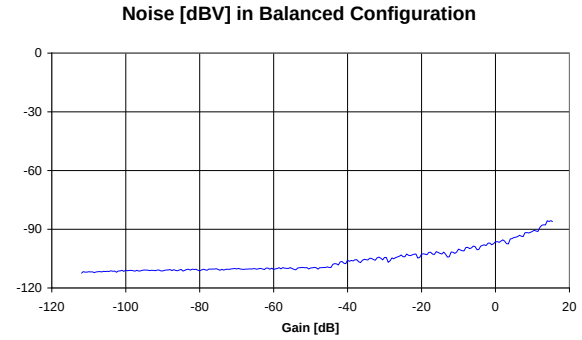


Figure 1. A-Weighted Noise in Balanced Configuration (gain=0dB)

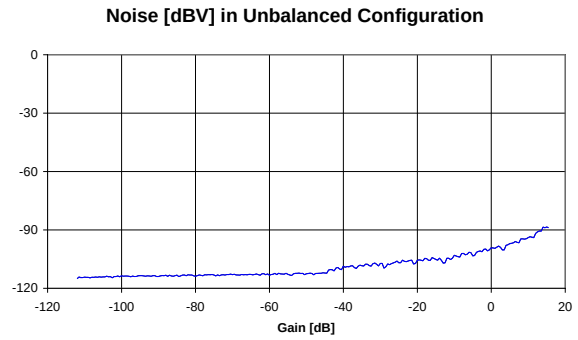


Figure 2. A-Weighted Noise in Unbalanced Configuration (gain=0dB)

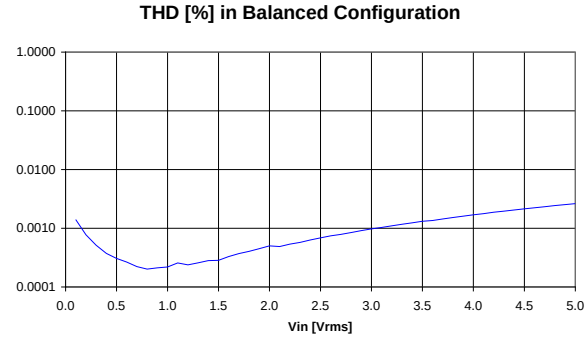


Figure 3. THD in Balanced Configuration (fin=1kHz, gain=0dB)

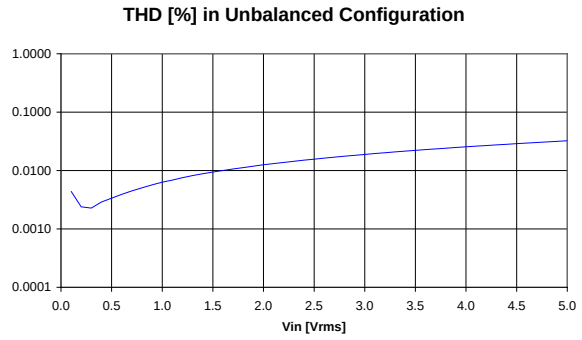


Figure 4. THD in Unbalanced Configuration (fin=1kHz, gain=0dB)

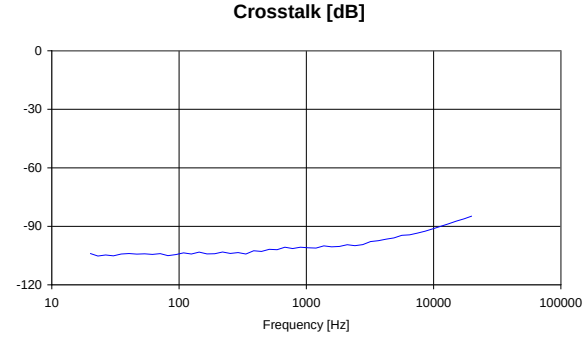


Figure 5. Crosstalk Measurement (Vin=5Vrms, gain=0dB)

DIGITAL CHARACTERISTICS

◆ Digital Inputs/Outputs

(AVCC=+5.0 V, AGND=0 V, TA=+25°C unless otherwise noted)

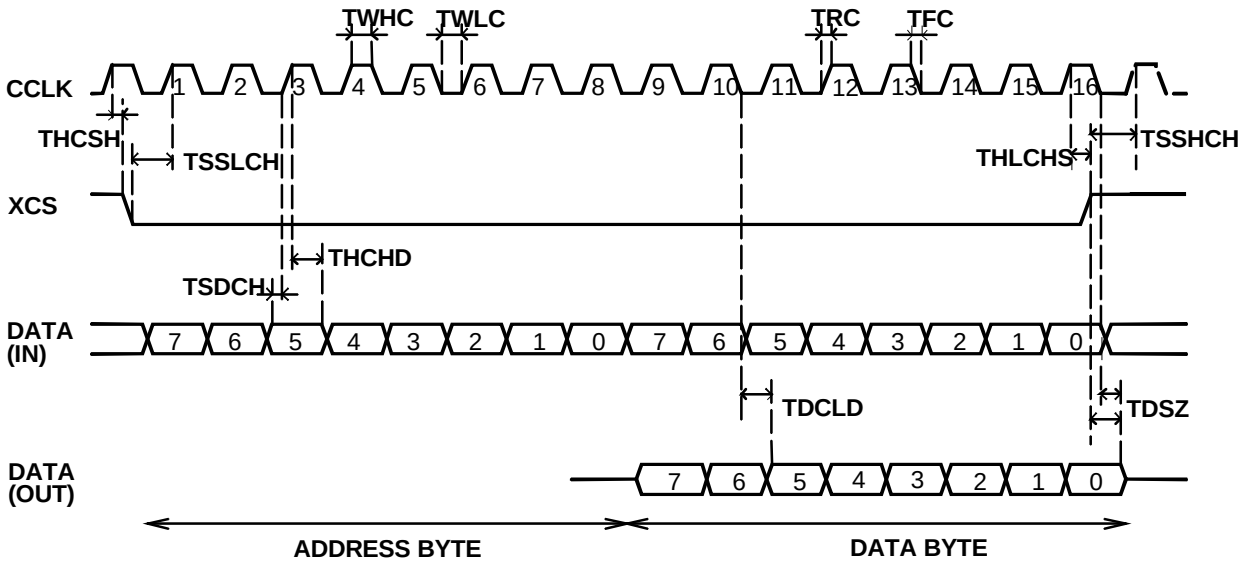
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input low voltage	VIL	All digital inputs, DC			0.3* DVCC	V
Input high voltage	VIH	All digital inputs, DC	0.7* DVCC			V
Output low voltage	VOL	All digital outputs, IL=2mA			0.3* DVCC	V
Output high voltage	VOH	All digital outputs, IH=-2mA	0.7* DVCC			V

◆ Serial Interface Timing

(AVCC=+5.0 V, AGND=0 V, TA=+25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency of CCLK	FCCLK				10	MHz
Period of CCLK high	TWHC	Measured from VIH to VIH	50			ns
Period of CCLK low	TWLC	Measured from VIL to VIL	50			ns
Rise time of CCLK	TRC	Measured from VIL to VIH			100	ns
Fall time of CCLK	TFC	Measured from VIH to VIL			100	ns
Hold time, CCLK high to XCS low	THCSH		20			ns
Setup time, XCS low to CCLK high	TSSLCH		100			ns
Setup time, valid CI to CCLK high	TSDCH		100			ns
Hold time, CCLK high to invalid CI	THCHD		100			ns
Delay time, CCLK low to valid CI	TDCLD	Load=100pF			50	ns
Delay time, XCS high or 8th CCLK low to invalid CI	TDSZ	Load=3.3kΩ	50		150	ns
Hold time, 16th CCLK high to XCS high	THLCHS		200			ns
Setup time, XCS high to CCLK high	TSSHCH		200			ns

SERIAL INTERFACE TIMING



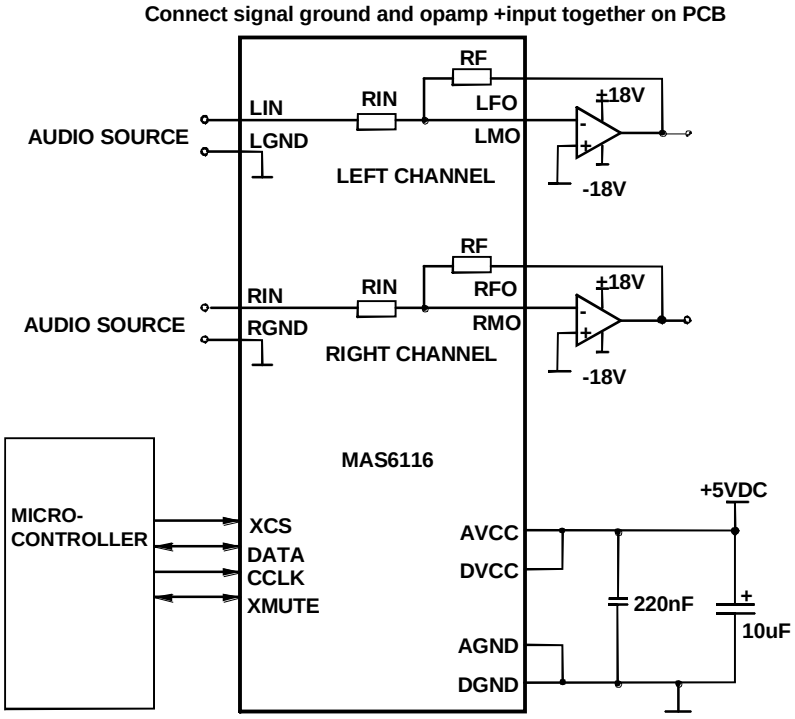
APPLICATION INFORMATION

Following general recommendations apply for MAS6116 applications.

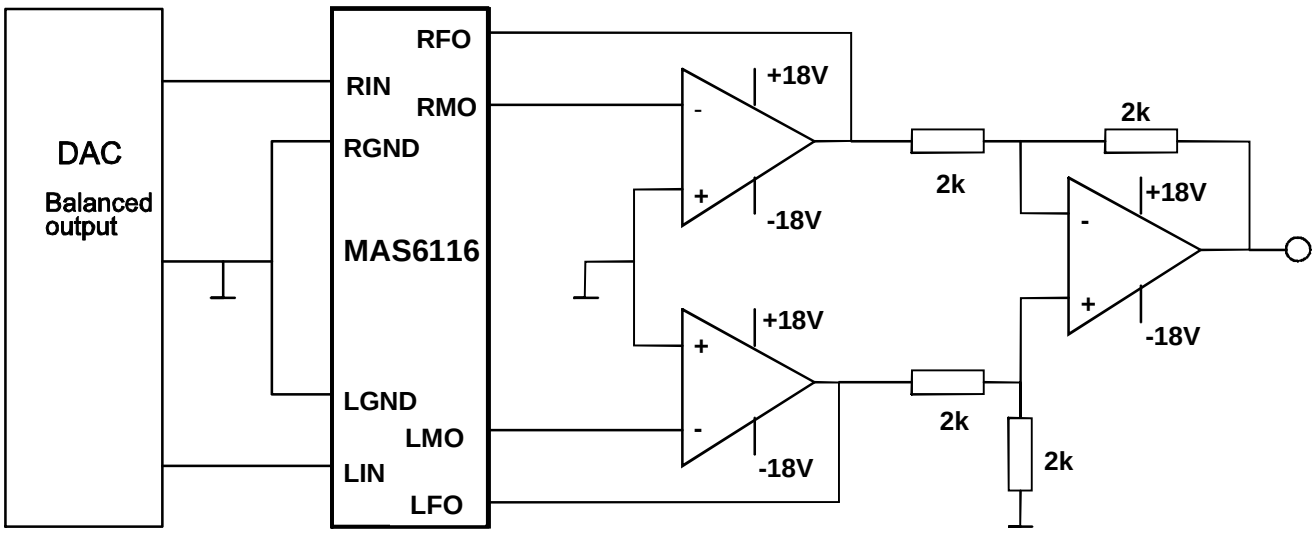
1) All four ground pins LGND, RGND, AGND and DGND have to have low ohmic connection to the same physical ground net. Any potential difference between these ground nets may potentially trigger destructive latch-up phenomena.
2) Keep audio input signals off until the MAS6116 has proper supply voltages.
3) In power up provide +5V supply voltage for the MAS6116 before supplying power to the external operational amplifiers. In power down turn off powers in reverse order i.e. turn off last +5V supply voltage. This power up / down procedure guarantees that MAS6116 provides always proper feedback loop for the operational amplifier circuit signals.
4) The LMO and RMO virtual ground pin voltages should be kept within ±100mV from ground potential. To guarantee this it is possible to add external Shottky diodes in both directions from LMO and RMO to ground.

APPLICATION INFORMATION

Application Note 1 – Typical application



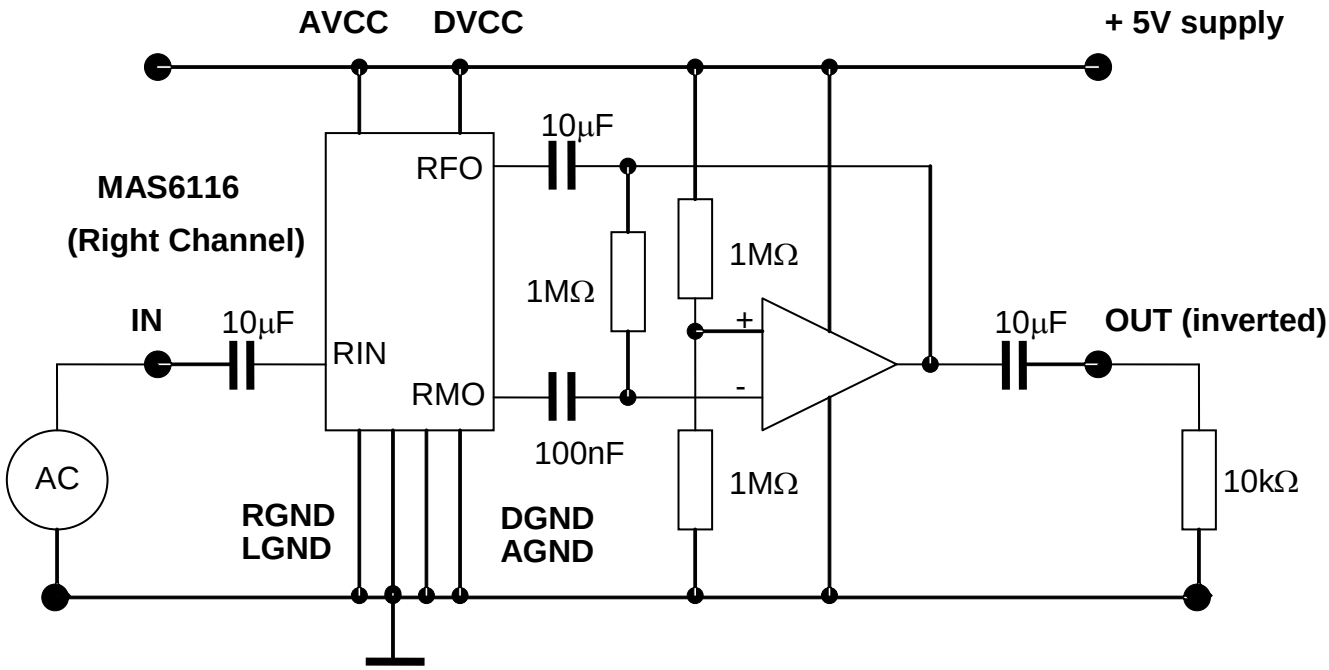
Application Note 2 - Configuration for balanced output DAC (only one channel shown)



APPLICATION INFORMATION

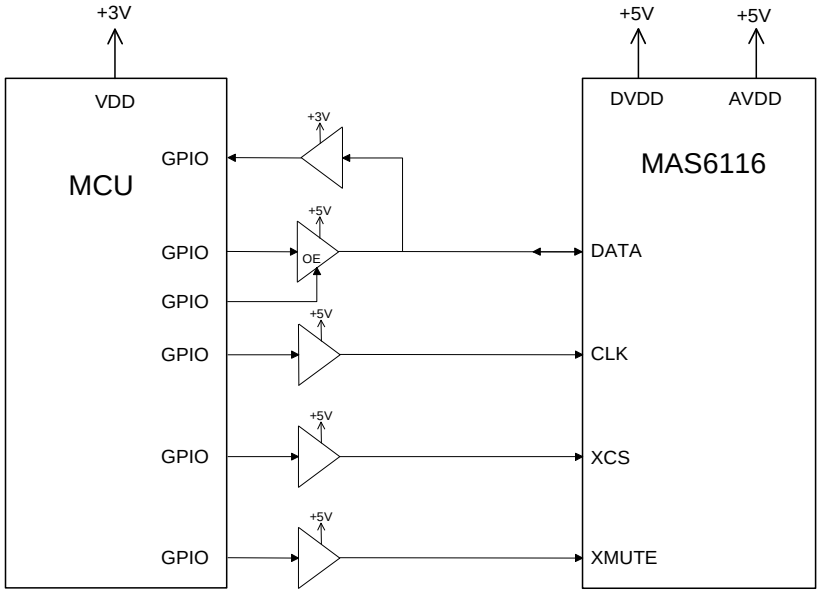
Application Note 3 – Single supply voltage usage

Single supply voltage circuit below is based on signal AC coupling and biasing output opamp in the middle point of supply voltages. Note that only right channel circuit is presented. The left channel circuit would be exactly the same. The component values have been chosen to limit overall lower corner frequency to about 10 Hz.



Application Note 4 – Lower supply voltage MCU communication example 1

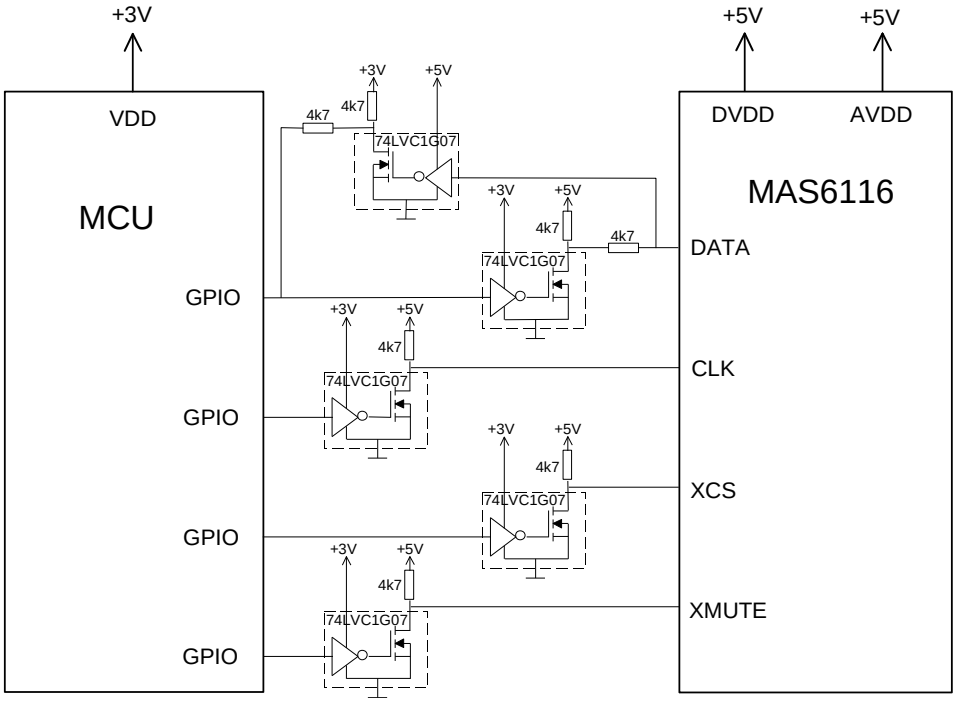
If the serial control interface is driven from an MCU that operates from a lower supply voltage compared to the 5V supply voltage, used by MAS6116, level shifting is needed to get correct digital signal levels in the communication. The bi-directional DATA line requires additionally level shifting in both directions. The figure below shows an example of a serial interface level shifting between 3V and 5V voltage supplies. In this example level shifters with output enable function are used. The output enable function is used to disable the level shifter output when the MAS6116 bi-directional data line direction changes.



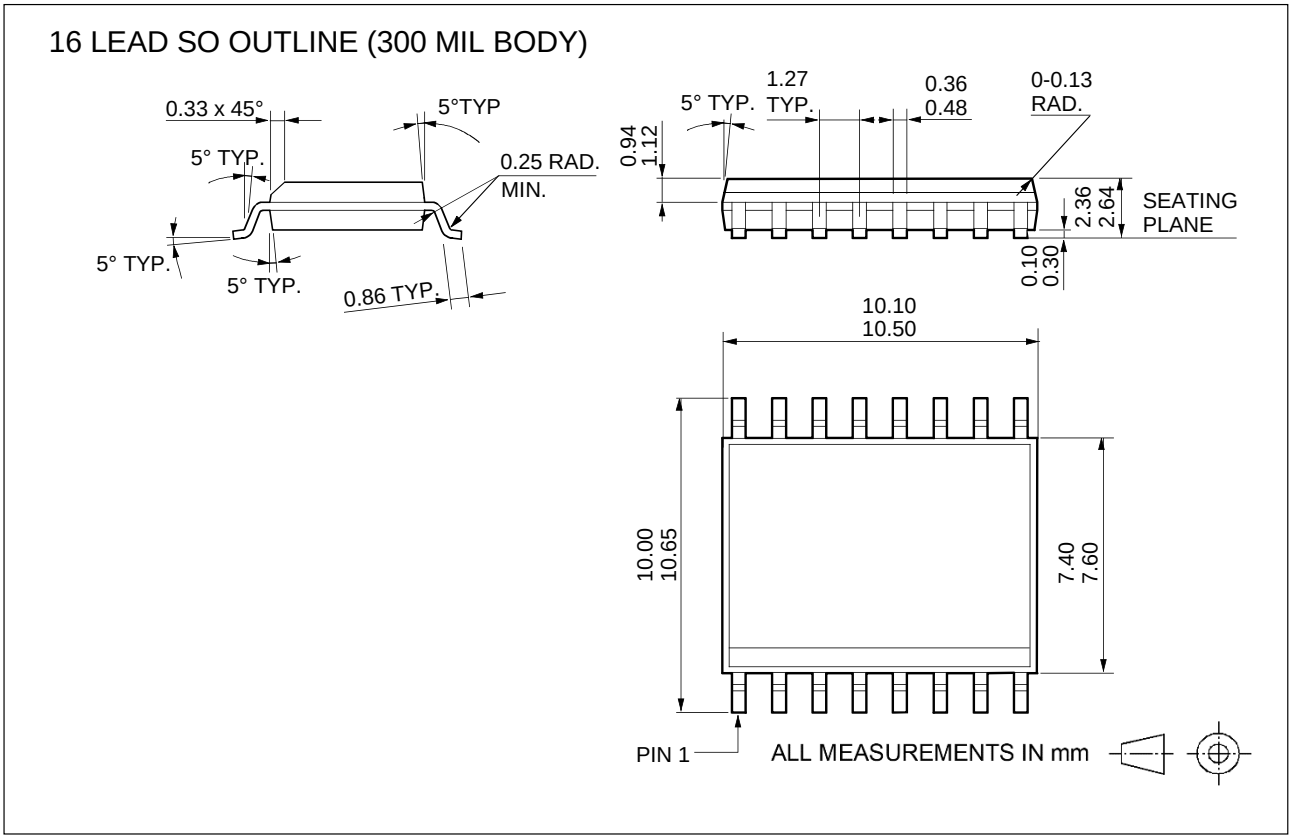
APPLICATION INFORMATION

Application Note 5 – Lower supply voltage MCU communication example 2

A second example where level shifting is needed is shown in the figure below. Open drain buffers are used in the level shifting between 3V and 5V signal levels. In this example the DATA signal line communication is bi-directional also on the MCU side.



SO-16 PACKAGE OUTLINE



All dimensions are in accordance with JEDEC standard MS-013.

SOLDERING INFORMATION

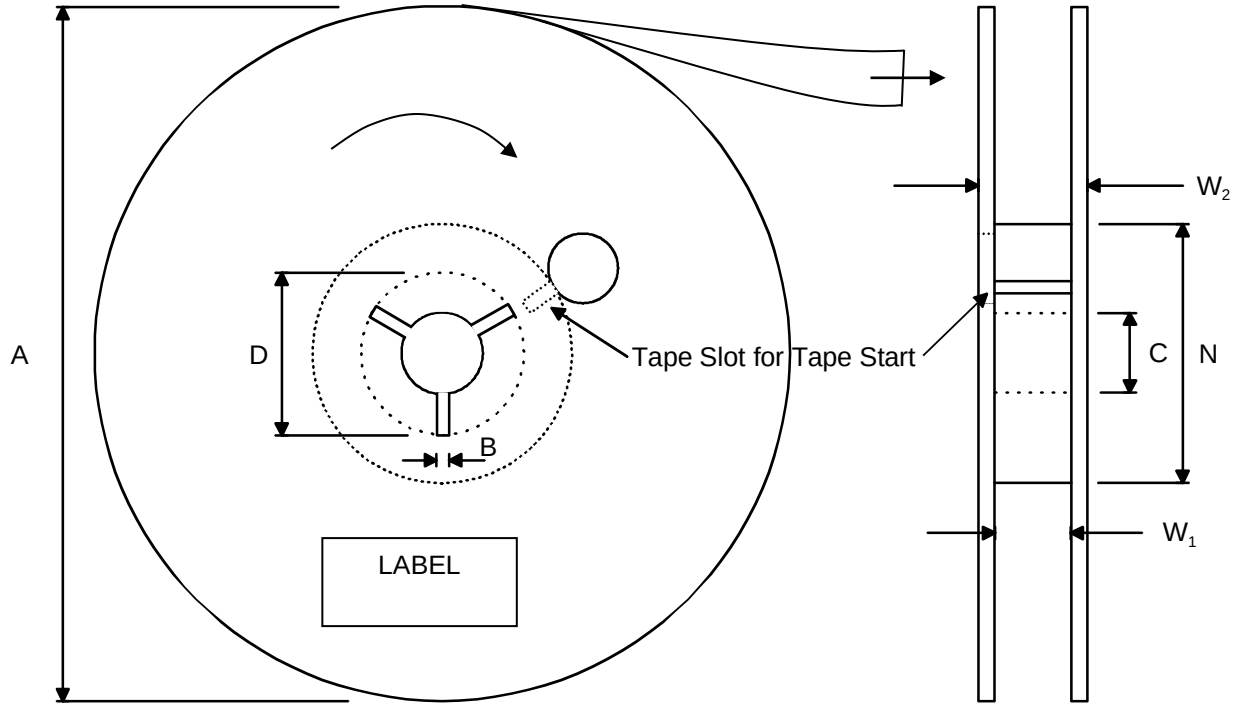
◆ **For Lead-Free / Green**

Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20
Maximum Temperature	260°C
Maximum Number of Reflow Cycles	3
Reflow profile	Thermal profile parameters stated in IPC/JEDEC J-STD-020 should not be exceeded. http://www.jedec.org
Lead Finish	Solder plate 7.62 - 25.4 µm, material Matte Tin

◆ **Rework guideline**

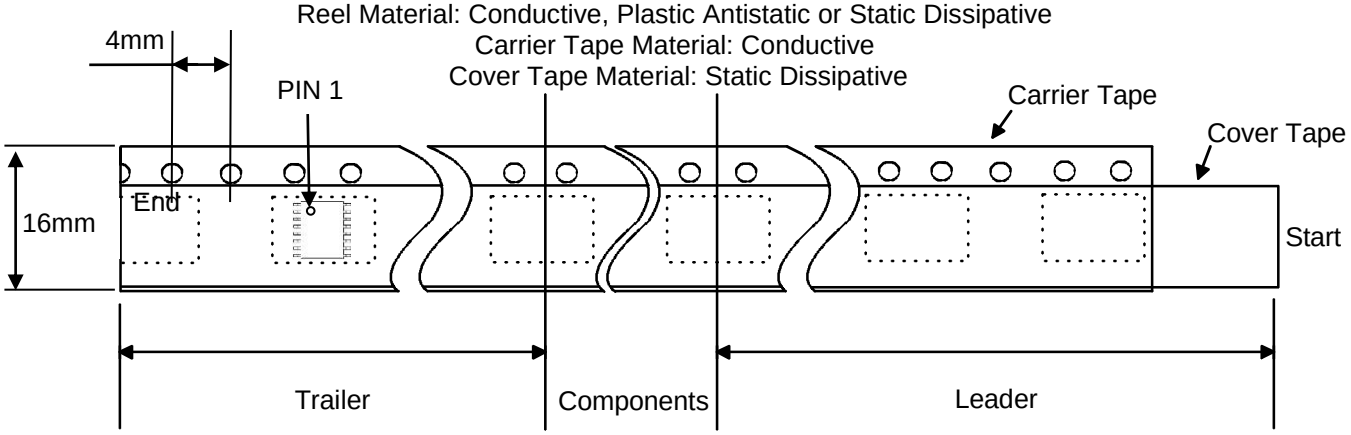
According to JEDEC standard J-STD-020C the moisture sensitivity level (MSL) 3 package SO-16 can withstand maximum 260°C peak temperature for 20-40 seconds. The replacement part needs to be installed within 168 hours after opening of the moisture barrier bag or otherwise the part needs to be re-baked.

REEL SPECIFICATIONS



1000 Components on Each Reel

Reel Material: Conductive, Plastic Antistatic or Static Dissipative
Carrier Tape Material: Conductive
Cover Tape Material: Static Dissipative



Dimension	Min	Nom	Max	Unit
A		330		mm
B	1.5			mm
C		13.0	13.5	mm
D	20.2			mm
N	100			mm
W_1 (measured at hub)	16.4		18.4	mm
W_2 (measured at hub)			22.4	mm
Trailer	500mm, see note			mm
Leader	500mm, see note			mm

Note: consists of empty carrier tape sealed with cover tape

ORDERING INFORMATION

Product Code	Product	Package	Quantity	Comments
MAS6116EA1SA306	MAS6116	16-pin Plastic SOIC, RoHS compliant	1000 pcs/reel in MBB	MBB=Moisture Barrier Bag
MAS6116EA1SA308	MAS6116	16-pin Plastic SOIC, RoHS compliant	47 pcs/tube	MSB0091A Bake recommendation for surface mounted devices

LOCAL DISTRIBUTOR

MICRO ANALOG SYSTEMS OY CONTACTS

Micro Analog Systems Oy
Kutomotie 16
FI-00380 Helsinki, FINLAND

Tel. +358 10 835 1100

http://www.mas-oy.com

NOTICE
Micro Analog Systems Oy (MAS) reserves the right to make changes to the products contained in this data sheet in order to improve the design or performance and to supply the best possible products. MAS assumes no responsibility for the use of any circuits shown in this data sheet, conveys no license under any patent or other rights unless otherwise specified in this data sheet, and makes no claim that the circuits are free from patent infringement. Applications for any devices shown in this data sheet are for illustration only and MAS makes no claim or warranty that such applications will be suitable for the use specified without further testing or modification.
MAS products are not authorized for use in safety-critical applications (such as life support) where a failure of the MAS product would reasonably be expected to cause severe personal injury or death. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of MAS products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by MAS. Further, Buyers must fully indemnify MAS and its representatives against any damages arising out of the use of MAS products in such safety-critical applications.
MAS products are neither designed nor intended for use in military/aerospace applications or environments. Buyers acknowledge and agree that any such use of MAS products which MAS has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.
MAS products are neither designed nor intended for use in automotive applications or environments. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, MAS will not be responsible for any failure to meet such requirements.