February 1990
Edition 2.0

FUJITSU

DATA SHEET

MB98A5090-25/5100-25/5110-25
MASK ROM MEMORY CARD

MASK PROGRAMMABLE READ ONLY MEMORY CARD
512K/1M/2M-BYTE

The Fujitsu MB98A5090/5100/5110 are Mask Programmable Read Only Memory (Mask ROM) cards capable of storing and retrieving large amounts of data. Each Mask ROM card contains multiple MB834200A or MB832000 devices.

The Mask ROM memory circuits are housed in a "credit-card" size 68-pin package. Internally circuitry is protected by metal plates on the top and bottom of the card to help reduced chip damage from electro-static discharge.

Fujitsu memory cards offer the unique ability to be organized in either 8-bit or 16-bit bus configuration at the user side.
All cards offer advantages of portable, low power and high speed operation.

- Card Dimension: 85.6 length x 54.0 width x 3.3 thickness (mm)
- Connector Type: 68-pin Two-Piece (Built-in 68-pin receptacle, 2 row type)
- Complete static operation: No clock required
- TTL compatible inputs/outputs
- Three state outputs
- Single + 5.0V ±5% power supply

CRD-68P-M02

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AVAILABLE ORGANIZATIONS

Part Number	Mounted Memory Device	Access Time	*Memory Organization
MB98A5090-25	MB834200A x 1 pc	250 ns	512K x 8 bit/256K x 16 bit
MB98A5100-25	MB834200A x 2 pcs	250 ns	1M x 8 bit/512K x 16 bit
MB98A5110-25	MB832000 x 8 pcs	250 ns	2M x 8 bit/1M x 16 bit

* Configurable at user side.

ABSOLUTE MAXIMUM RATINGS (see NOTE.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.5 to V_{CC} +0.5	V
Output Voltage	$V_{I/O}$	−0.5 to V_{CC} +0.5	V
Temperature under Bias	T_{BIAS}	−10 to +60	°C
Storage Temperature	T_{STG}	−30 to +70	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Fig. 1 — MB98A5090/5100 BLOCK DIAGRAM

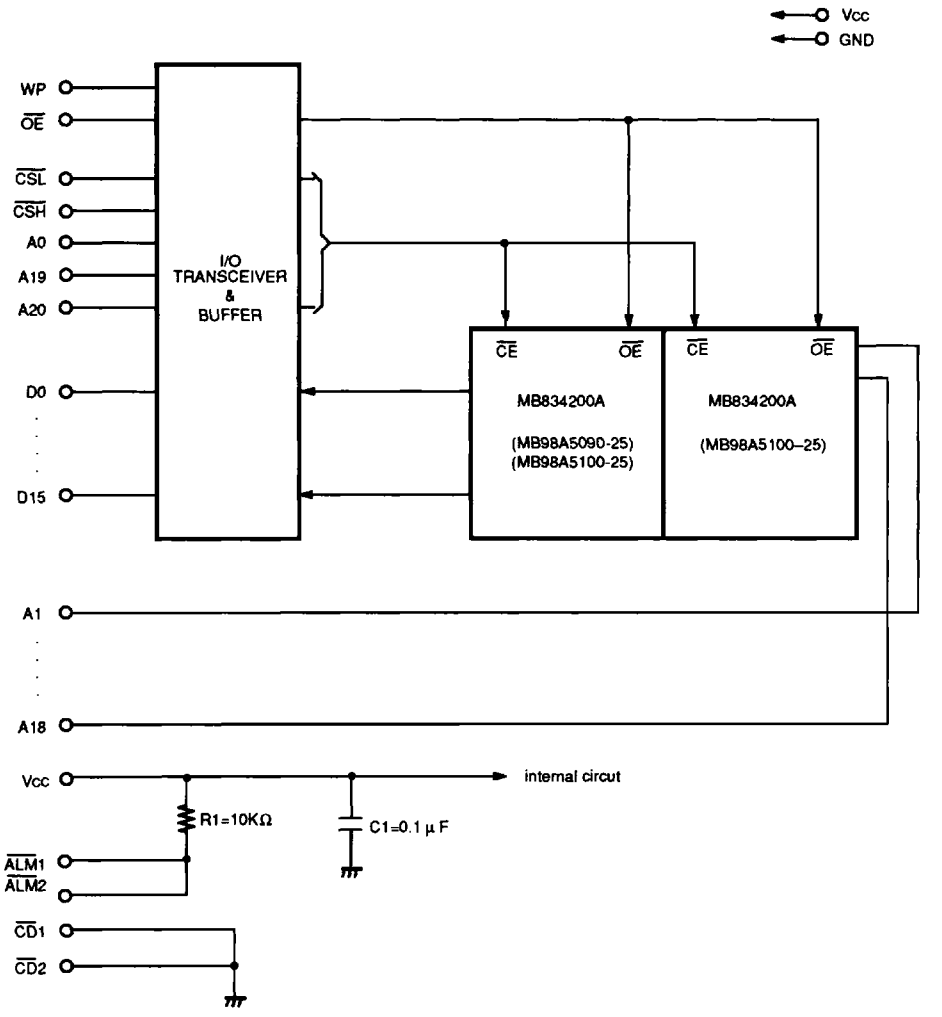
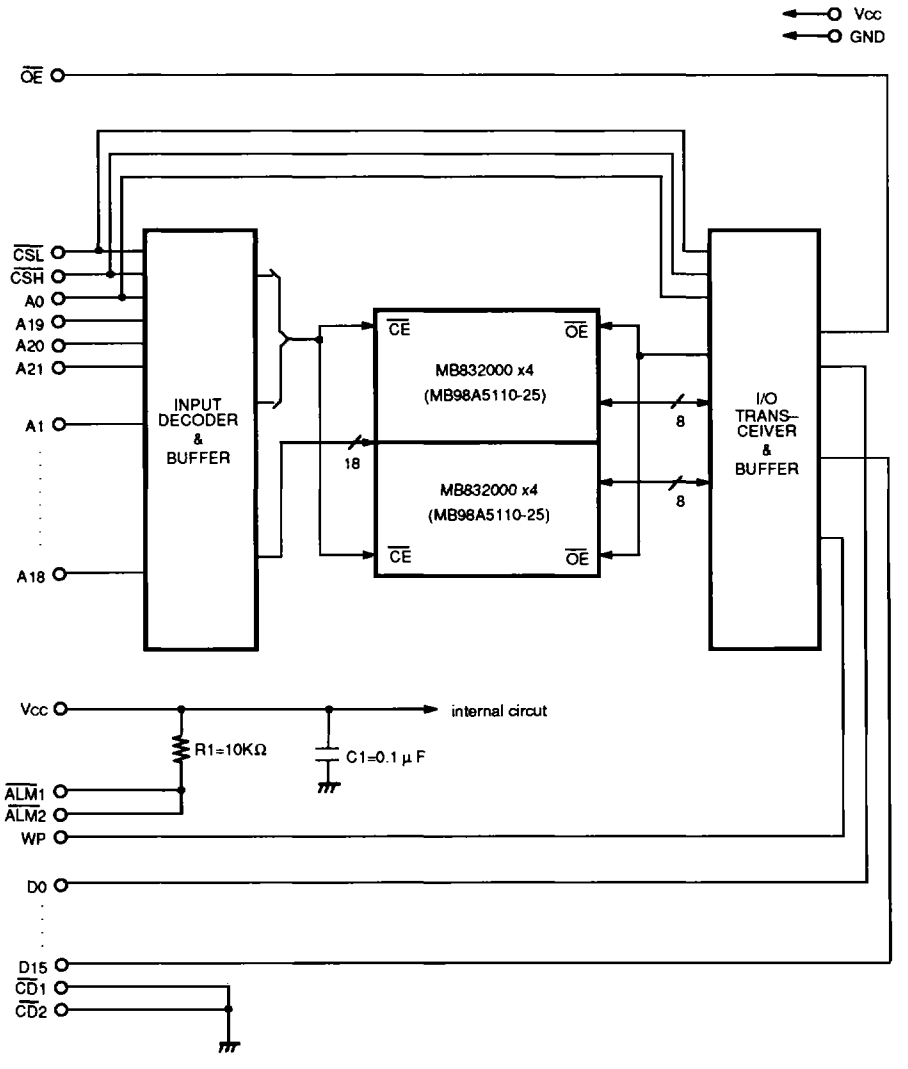


Fig. 2 – MB98A5110 BLOCK DIAGRAM



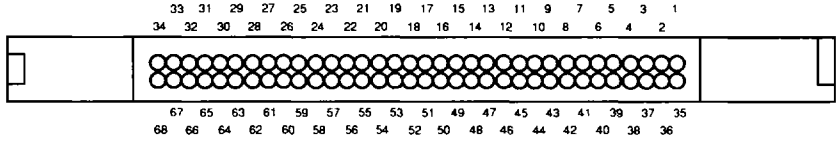
PIN ASSIGNMENTS

MB98A5090	MB98A5100	MB98A5110	Pin No.		MB98A5090	MB98A5100	MB98A5110
GND	GND	GND	1	35	GND	GND	GND
D3	D3	D3	2	36	$\overline{CD1}$	$\overline{CD1}$	$\overline{CD1}$
D4	D4	D4	3	37	D11	D11	D11
D5	D5	D5	4	38	D12	D12	D12
D6	D6	D6	5	39	D13	D13	D13
D7	D7	D7	6	40	D14	D14	D14
$\overline{CSL}$	$\overline{CSL}$	$\overline{CSL}$	7	41	D15	D15	D15
A10	A10	A10	8	42	$\overline{CSH}$	$\overline{CSH}$	$\overline{CSH}$
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	9	43	NC	NC	NC
A11	A11	A11	10	44	NC	NC	NC
A9	A9	A9	11	45	NC	NC	NC
A8	A8	A8	12	46	A17	A17	A17
A13	A13	A13	13	47	A18	A18	A18
A14	A14	A14	14	48	A19 *	A19	A19
NC	NC	NC	15	49	A20 *	A20 *	A20
NC	NC	NC	16	50	NC	NC	A21 *
Vcc	Vcc	Vcc	17	51	Vcc	Vcc	Vcc
NC	NC	NC	18	52	NC	NC	NC
A16	A16	A16	19	53	NC	NC	NC
A15	A15	A15	20	54	NC	NC	NC
A12	A12	A12	21	55	NC	NC	NC
A7	A7	A7	22	56	NC	NC	NC
A6	A6	A6	23	57	NC	NC	NC
A5	A5	A5	24	58	NC	NC	NC
A4	A4	A4	25	59	NC	NC	NC
A3	A3	A3	26	60	NC	NC	NC
A2	A2	A2	27	61	NC	NC	NC
A1	A1	A1	28	62	$\overline{ALM1}$	$\overline{ALM1}$	$\overline{ALM1}$
A0	A0	A0	29	63	$\overline{ALM2}$	$\overline{ALM2}$	$\overline{ALM2}$
D0	D0	D0	30	64	D8	D8	D8
D1	D1	D1	31	65	D9	D9	D9
D2	D2	D2	32	66	D10	D10	D10
WP	WP	WP	33	67	$\overline{CD2}$	$\overline{CD2}$	$\overline{CD2}$
GND	GND	GND	34	68	GND	GND	GND

Note: A19, A20 and A21 pins asterisked (*) should be kept at V_{IL}.

PIN LOCATIONS

Fig. 3 – BOTTOM VIEW (CONNECTOR SIDE)



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PIN DESCRIPTION

Symbol	Pin Name	Input/Output	Function
A0 to A21	Address Input	Input	Address Inputs, A0-A21
D0 to D15	Data Input/Output	Input/Output	Data Inputs/Outputs This data bus size (8-bit or 16-bit) selected with $\overline{CSL}$ and $\overline{CSH}$.
$\overline{CSL}$	Chip Select for Lower Byte	Input	Active Low –Lower byte (D0-D7) is selected for read function. (Refer to FUNCTION TRUTH TABLE.)
$\overline{CSH}$	Chip Select for Upper Byte	Input	Active Low –Upper byte (D8-D15) is selected for read function. (Refer to FUNCTION TRUTH TABLE.)
$\overline{OE}$	Output Enable	Input	Active Low –Output enable for Mask ROM cards
$\overline{CD1}$, $\overline{CD2}$	Card Detect	Output	These pins detect if the card has been correctly inserted. Both pins are tied to GND internally.
WP	Write Protect	Output	This pin outputs high level for Mask ROM cards.
$\overline{ALM1}$, $\overline{ALM2}$	Battery Alarm	Output	Both pins are tied to Vcc internally.
Vcc	Power Supply	–	Power Supply Voltage (+5.0V ±5%)
GND	Ground	–	System Ground
NC	Non Connection	–	

FUNCTION TRUTH TABLE

$\overline{CSH}$	$\overline{CSL}$	A0	$\overline{OE}$	Mode	Data Output	
					D15–D8	D7–D0
H	H	X	X	Standby	High–Z	
H	L	L	L	Read (x8)	High–Z	D_{OUT} (Lower Btye)
H	L	H	L	Read (x8)	High–Z	D_{OUT} (Upper Byte)
L	H	X	L	Read (x8)	D_{OUT} (Upper Btye)	High–Z
L	L	X	L	Read (x16)	D_{OUT}	
X	X	X	H	Output Disable	High–Z	

Definition: H = V_{IH}, L = V_{IL}, X = Either V_{IL} or V_{IH}

ADDRESS CONFIGURATION USING 8-BIT BUS ($\overline{CSH}$ = H, $\overline{CSL}$ = L)

A21 to A0	$\overline{CSH}$	$\overline{CSL}$	D15–D8	D7–D0
00 0000 0000 0000 0000 0000	H	L	High–Z	0 Add.
00 0000 0000 0000 0000 0001	H	L	High–Z	1 Add.
00 0000 0000 0000 0000 0010	H	L	High–Z	2 Add.
00 0000 0000 0000 0000 0011	H	L	High–Z	3 Add.
↓ ↓ ↓ ↓ ↓ ↓	↓	↓	↓ ↓	↓ ↓
11 1111 1111 1111 1111 1100	H	L	High–Z	4194300 Add.
11 1111 1111 1111 1111 1101	H	L	High–Z	4194301 Add.
11 1111 1111 1111 1111 1110	H	L	High–Z	4194302 Add.
11 1111 1111 1111 1111 1111	H	L	High–Z	4194303 Add.

ADDRESS CONFIGURATION USING 8-BIT BUS ($\overline{CSH}$ = L, $\overline{CSL}$ = H)

A21 to A0	$\overline{CSH}$	$\overline{CSL}$	D15–D8	D7–D0
00 0000 0000 0000 0000 000X	L	H	1 Add.	High–Z
00 0000 0000 0000 0000 001X	L	H	3 Add.	High–Z
00 0000 0000 0000 0000 010X	L	H	5 Add.	High–Z
00 0000 0000 0000 0000 011X	L	H	7 Add.	High–Z
↓ ↓ ↓ ↓ ↓ ↓	↓	↓	↓ ↓	↓ ↓
11 1111 1111 1111 1111 100X	L	H	4194297 Add.	High–Z
11 1111 1111 1111 1111 101X	L	H	4194299 Add.	High–Z
11 1111 1111 1111 1111 110X	L	H	4194301 Add.	High–Z
11 1111 1111 1111 1111 111X	L	H	4194303 Add.	High–Z

Definition: X = Either "0" or "1". Even addresses are not available in this mode.

ADDRESS CONFIGURATION USING 16-BIT BUS ($\overline{CSH}$ = L, $\overline{CSL}$ = L)

A21 to A0	$\overline{CSH}$	$\overline{CSL}$	D15–D8	D7–D0
00 0000 0000 0000 0000 000X	L	L	1 Add.	0 Add.
00 0000 0000 0000 0000 001X	L	L	3 Add.	2 Add.
00 0000 0000 0000 0000 010X	L	L	5 Add.	4 Add.
00 0000 0000 0000 0000 011X	L	L	7 Add.	6 Add.
↓ ↓ ↓ ↓ ↓ ↓	↓	↓	↓ ↓	↓ ↓
11 1111 1111 1111 1111 100X	L	L	4194297 Add.	4194296 Add.
11 1111 1111 1111 1111 101X	L	L	4194299 Add.	4194298 Add.
11 1111 1111 1111 1111 110X	L	L	4194301 Add.	4194300 Add.
11 1111 1111 1111 1111 111X	L	L	4194303 Add.	4194302 Add.

Definition: X = Either "0" or "1".

RECOMMENDED OPERATING CONDIITONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4 75	5.0	5.25	V
Ground	GND	0	0	0	V
Ambient Temperature	T_A	0		50	°C

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DC CHARACTERISTICS

(Recommended Operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Standby Supply Current	$\overline{CSL}$ = $\overline{CSH}$ ≥ V_{CC}–0.2V	I_{SB1}		2.0	mA
	$\overline{CSL}$ = $\overline{CSH}$ = V_{IH}	I_{SB2}		10.0	mA
Operating Supply Current	Cycle = Min. Duty = 100%, Iout = 0mA	I_{CC}		100	mA
Input Leakage Current	V_{IN} = 0V to V_{CC}	I_{LI}	–10	10	µA
Output Leakage Current	$V_{I/O}$ = 0V to V_{CC} $\overline{CSL}$ = $\overline{CSH}$ = V_{IH} $\overline{OE}$ = V_{IH} or $\overline{WE}$ V_{IL}	$I_{LI/O}$	–10	10	µA
Input High Voltage		V_{IH}	2.2	V_{CC} +0.3	V
Input Low Voltage		V_{IL}	–0.3	0.8	V
Output High Voltage	I_{OH} = –1.0mA	V_{OH}	2.4		V
Output Low Voltage	I_{OL} = 2.1mA	V_{OL}		0.4	V

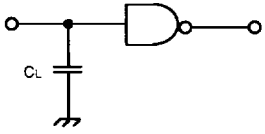
Note: All voltages are referenced to GND

CAPACITANCE

(T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}			45	pF
I/O Capacitance ($V_{I/O}$ = 0V)	C_{OUT}			45	pF

Fig. 4 – AC TEST CONDITIONS



- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: t_T = 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels
  - Input: V_{IL} = 0.8V, V_{IH} = 2.2V
  - Output V_{OL} = 0.8V, V_{OH} = 2.0V
- Output Load: 1TTL gate + C_L (100pF)

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AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	Min	Max	Unit
Address Access Time *1	t_{ACC}		250	ns
Chip Select Accsess Time	t_{CS}		250	ns
Output Enable to Output Valid *1	t_{OE}		120	ns
Output Disable Time *2	t_{DF}		100	ns
Output Hold Time	t_{OH}	0		ns

Note: *1 t_{OE} may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CSL}$, $\overline{CSH}$ without impact on t_{ACC}.

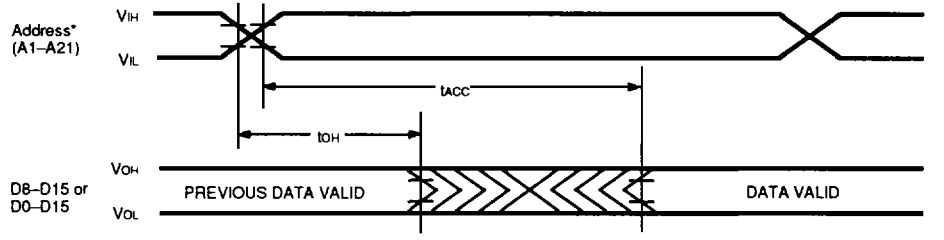
*2 t_{DF} is specified from the rising edge of $\overline{OE}$, $\overline{CSL}$ or $\overline{CSH}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE TIMING DIAGRAM

READ CYCLE 1: $\overline{CSL}$ = V_{IH}, $\overline{CSH}$ = $\overline{OE}$ = V_{IL}: x 8–bit Bus Organization
$\overline{CSL}$ = $\overline{CSH}$ = $\overline{OE}$ = V_{IL}: x 16–bit Bus Organization



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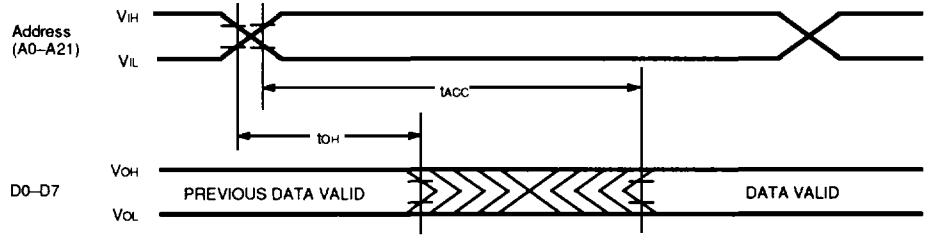
Note: *A0 = Either V_{IL} or V_{IH}.

READ CYCLE 2: $\overline{CSH}$ = V_{IH}, $\overline{CSL}$ = $\overline{OE}$ = V_{IL}: x 8–bit Bus Organization



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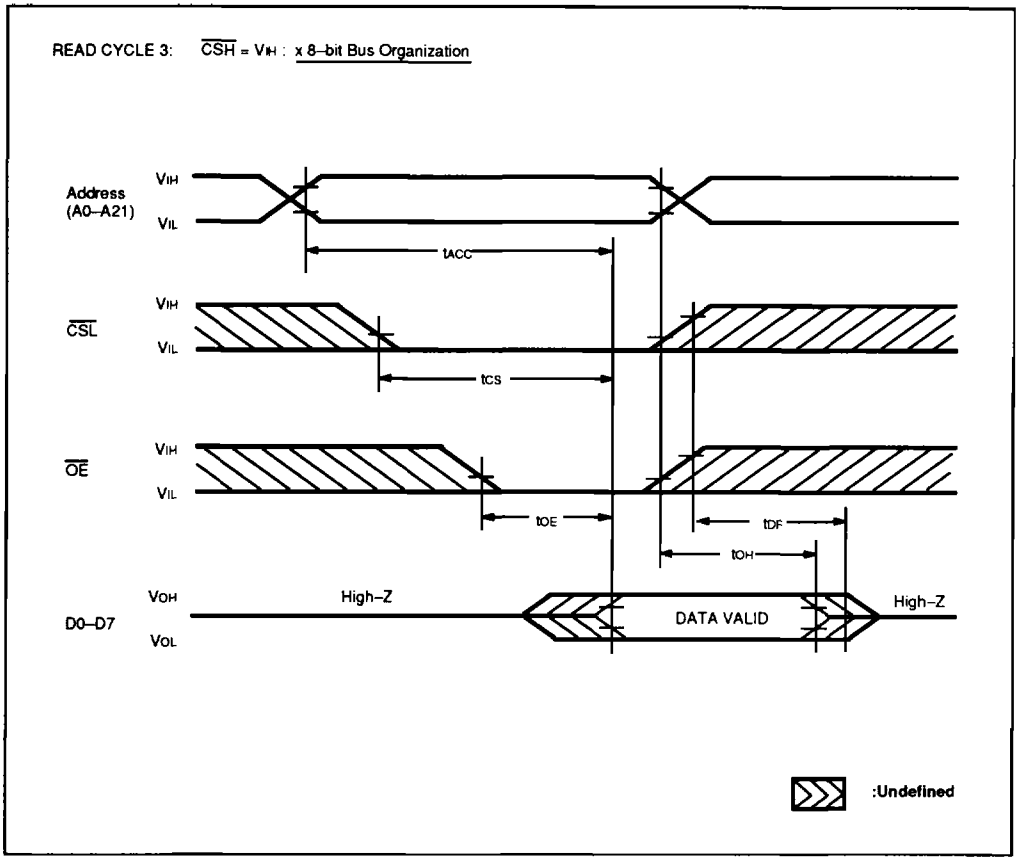
AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

READ CYCLE TIMING DIAGRAM

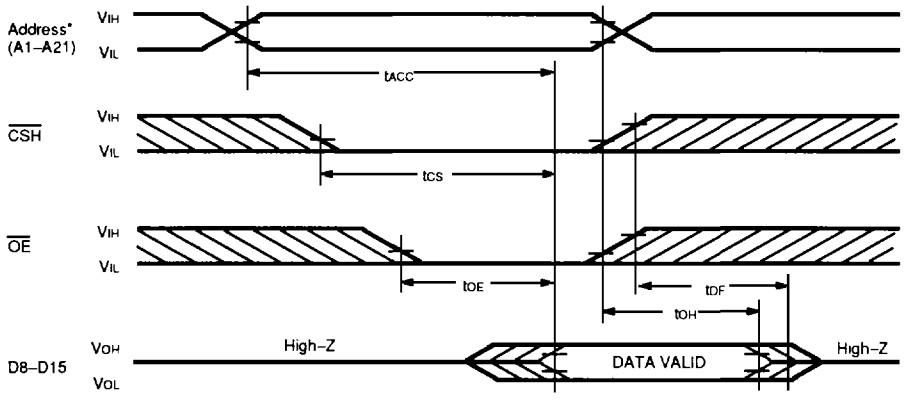


AC CHARACTERISTICS (Continued)

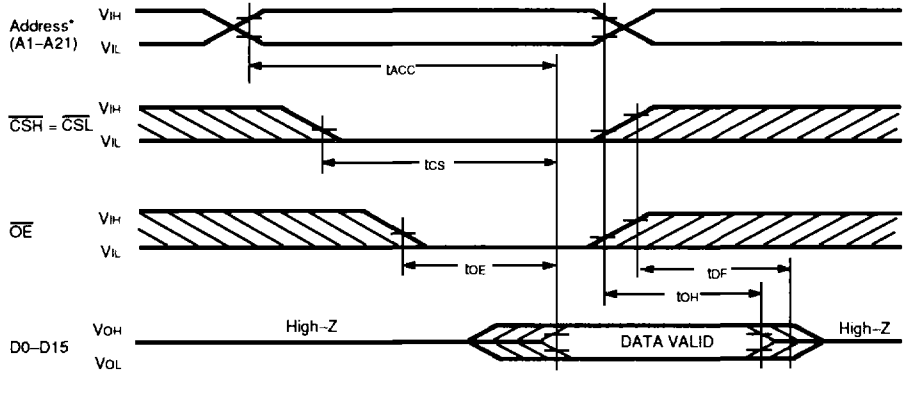
(Recommended operating conditions unless otherwise noted.)

READ CYCLE TIMING DIAGRAM

READ CYCLE 4: $\overline{CSL}$ = V_{IH}: x 8-bit Bus Organization



READ CYCLE 5: $\overline{CSL}$ = $\overline{CSH}$ = V_{IL}: x 16-bit Bus Organization



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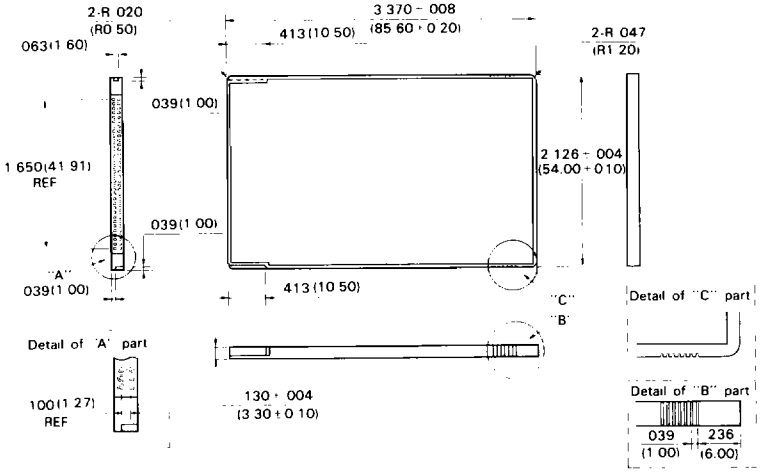
Note: * A0 = Either V_{IL} or V_{IH}.

PACKAGE DIMENSIONS

68-PIN MEMORY CARD
(CASE No.: CRD-68P-M02)



Dimensions in
inches (millimeters)

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