M54491P

CLOCK GENERATOR FOR HDTV

DESCRIPTION

The M54491P is a clock generator for HDTV.
When a frequency not exceeding 100 MHz is applied to the input (f IN), the ECL circuit divider divides it into 1/2, 1/3, 1/4, 1/6, and 1/12, and outputs them.
Each output is a TTL level output, with SKEW not exceeding ± 2 ns

FEATURES

- Divider circuit has the ECL structure.
- Output circuit has the TTL structure.
- f max = 100 MHz.
- Operating supply voltage Vcc = 5.0 ± 0.25 V
- Divided outputs 1/2, 1/3, 1/4, 1/6, 1/12

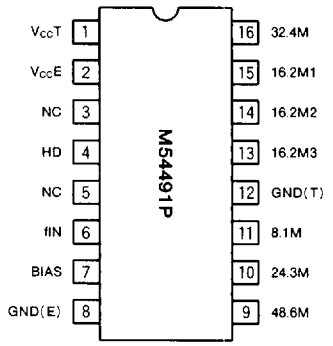
APPLICATION

HDTV

RECOMMENDED OPERATING CONDITION

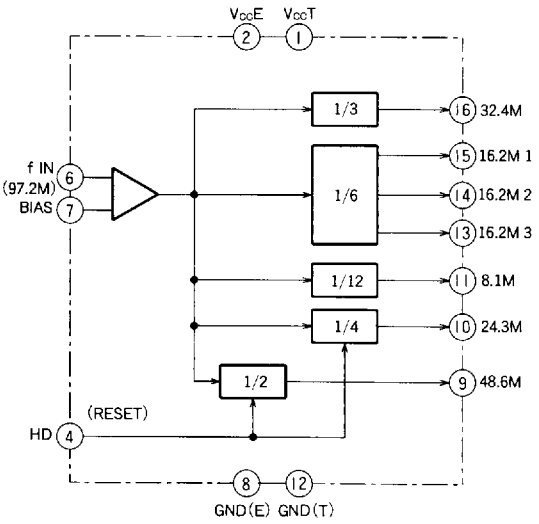
Supply voltage .....4.75 ~ 5.25 V
Output "L" current.....0 ~ 8mA (TTL output)
Pixel Rate.....100 MHz (Max)
Operating temperature..... -10 ~ 70°C

PIN CONFIGURATION

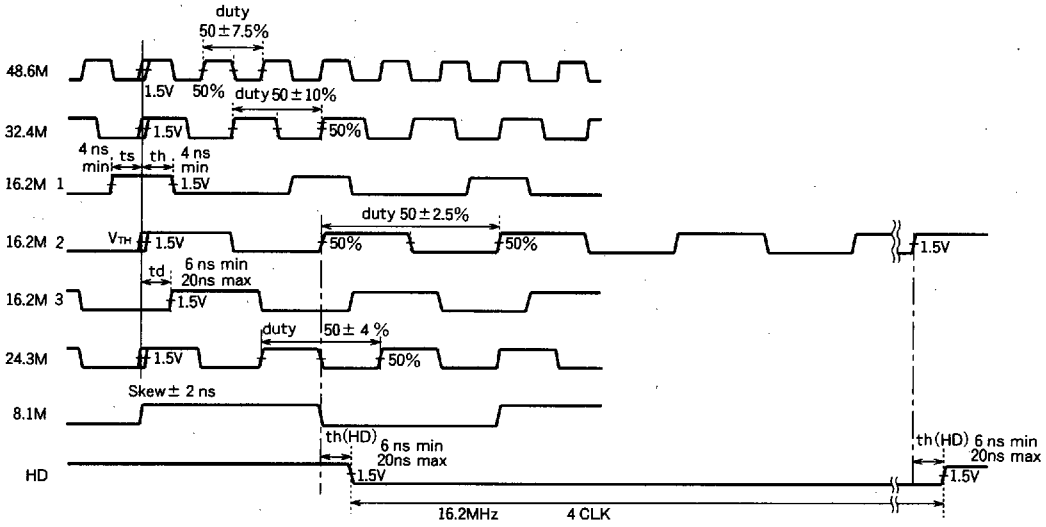


Outline 16P4

BLOCK DIAGRAM



TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CCT} V_{CCE}	Supply voltage	6.5	V
V_I	Input voltage	6.5	V
Pd	Power dissipation	625	mW
Topr	Operating temperature	−20∼70	℃
Tstg	Storage temperature	−40∼150	℃

ELECTRICAL CHARACTERISTICS (Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{IH}	"H" input voltage	4		2.0		V_{CC} +0.3	V
V_{IL}	"L" input voltage	4				0.7	V
I_{IH}	"H" input current	4	V_{CCT}=5.25V V_I=2.7V			20	μA
I_{IL}	"L" input current	4	V_{CCT}=5.25V V_I=0.4V			−200	μA
V_{IC}	Input clamp voltage	4	V_{CCT}=4.75V I_{IC}=−1.0mA		−1.2	−1.6	V
V_{OH}	"H" output voltage	9∼11	V_{CCT}=4.75V I_{OH}=−0.4mA	2.4	3.5		V
V_{OL}	"L" output voltage	13∼16	V_{CCT}=4.75V I_{OL}=8mA		0.35	0.5	V
I_{OS}	Output short-circuit current		V_{CCT}=5.25V V_O=0V	−30		−80	mA
I_{CC}	Supply current	1, 2	V_{CCT}=5.25V V_{CCE}=5.25V	60	90	120	mA

(Typical values are at V_{CCT}=V_{CCE}=5.0V, Ta=25℃.)

SWITCHING CHARACTERISTICS (Ta=−20~70°C, unless otherwise noted)

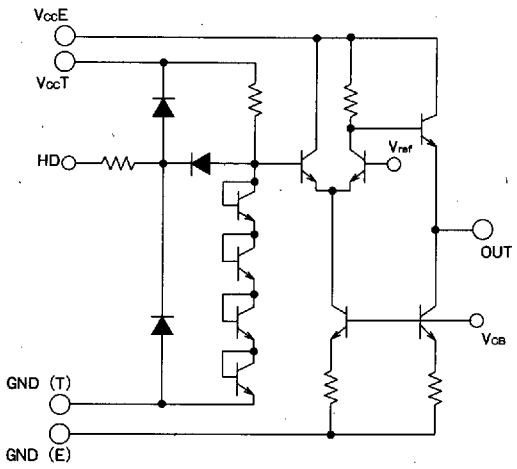
Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min.	Typ.	Max.	
fopr	Operating frequency	6	V_{IN}=−20~4dBm			100	MHz
fduty	Input frequency duty rate	6	f_{IN}=97.2MHz	−5.0	50	+5.0	%
Duty1	Output duty rate	9	$V_{CC}T=V_{CC}E$=4.75~5.25V	−7.5	50	+7.5	%
Duty2	Output duty rate	16	f_{IN}=97.2MHz	−10.0	50	+10.0	%
Duty3	Output duty rate	10	fduty=50±5%	−4.0	50	+4.0	%
Duty4	Output duty rate	14	$V_{TH}1=(V_{OH}+V_{OL})/2$	−2.5	50	+2.5	%
ts	Setup time	15	$V_{CC}T=V_{CC}E$=4.75~5.25V	4.0	10	20	ns
th	Hold time	15	f_{IN}=97.2MHz	4.0	10	20	ns
td	Delay time	13	fduty=50±5%	6.0	10	20	ns
th (HD)	Hold time	4	$V_{TH}2$=1.5V	6.0	10	20	ns
Skew	Output skew	9, 10, 14, 16,		−2.0	0	+2.0	ns

DESCRIPTION OF PIN

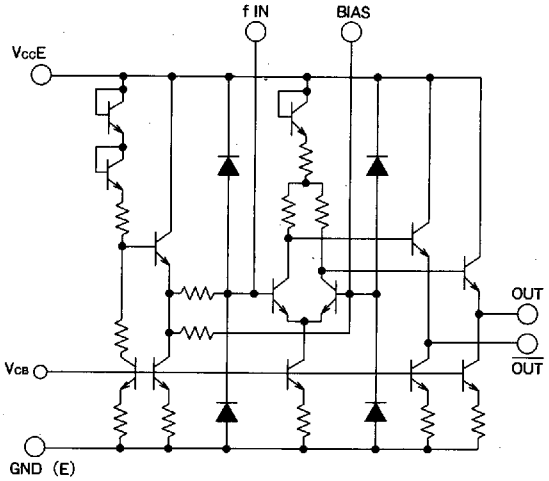
Symbol	Pin No.	Name of pin	Function
$V_{CC}T$ $V_{CC}E$	① ②	Supply voltage (TTL) Supply voltage (ECL)	Supply voltage pin for TTL circuit Apply 5.0±0.5V Supply voltage pin for ECL circuit Apply 5.0±0.5V
GND (T) GND (E)	⑫ ⑧	Grounding (TTL) Grounding (ECL)	GND for TTL circuit Grounding to 0V GND for ECL circuit Grounding to 0V
fIN	⑥	Dividing input	Dividing input pin Apply a frequency of 97.2MHz
BIAS	⑦	Bias	Unite a capacitor of 1000pF via which GND line is connected
HD	④	Reset input	TTL level for reset input
48.6M	⑨	Dividing output	TTL level for dividing output of 48.6MHz Duty : 50±7.5%
24.3M	⑩	Dividing output	TTL level for dividing output of 24.3MHz Duty : 50±4.0%, signal synchronized with 48.6MHz
8.1M	⑪	Dividing output	TTL level for dividing output of 8.1MHz
16.2M1	⑮	Dividing output	TTL level for dividing output of 16.2MHz Signal staying at level "H" for a given period of time before and after the rise edge of 16.2M2
16.2M2	⑭	Dividing output	TTL level for dividing output of 16.2MHz Duty : 50±2.5%, signal synchronized with 48.6MHz
16.2M3	⑬	Dividing output	TTL level for dividing output of 16.2MHz Signal delayed for a given time of 16.2M2
32.4M	⑯	Dividing output	TTL level for dividing output of 32.4MHz Duty : 50±5.0%, signal synchronized with 48.6MHz

INPUT/OUTPUT CIRCUIT DIAGRAM

1 HD input circuit



2 f IN, BIAS input circuit



3 TTL output circuit