MOTOROLA

MC34F19
MC34F19A

Advance Information

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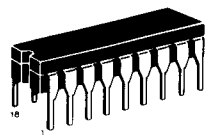
TELEPHONE LINE FEED AND 2- TO 4-WIRE CONVERSION CIRCUIT

. . . designed to replace the hybrid transformer circuit in Central Office, PABX and Subscriber carrier equipment, providing signal separation for two-wire differential to four-wire single-ended conversions and suppression of longitudinal signals at the two-wire input. It provides dc line current for powering the telset, operating from up to a 56 V supply.

- All Key Parameters Externally Programmable
- Current Sensing Outputs Monitor Status of Both Tip and Ring Leads
- On-Hook Power Below 5.0 mW
- Digital Hook Status Output
- Power Down Input
- Ground Fault Protection
- Size and Weight Reduction Over Conventional Approaches
- The sale of this product is licensed under patent No. 4,004,109. All royalties related to this patent are included in the unit price.

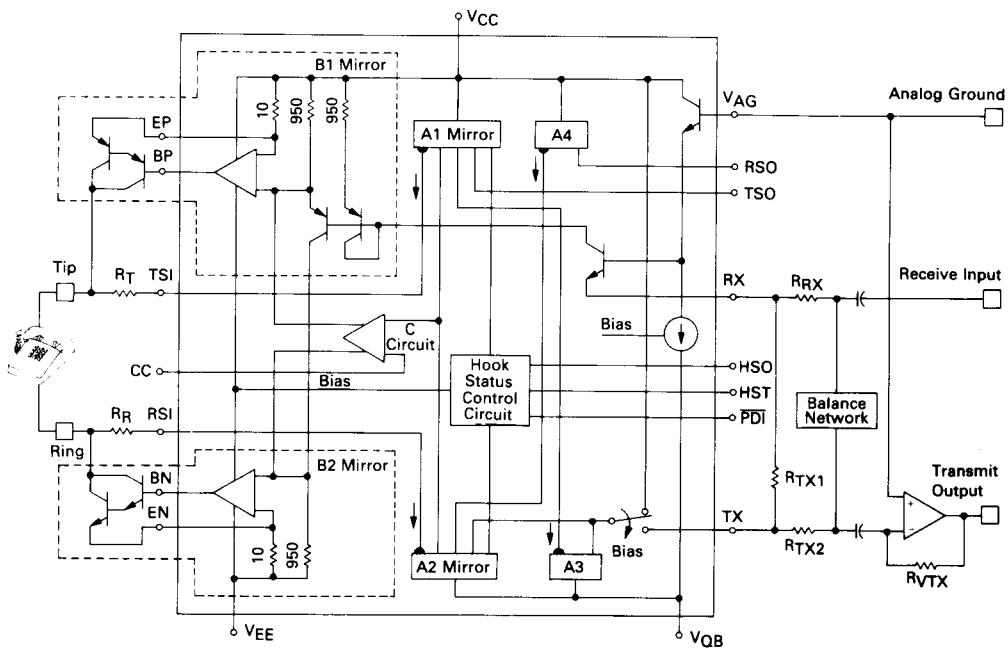
SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

BIPOLAR THIN-FILM INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 726-01

FUNCTIONAL BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

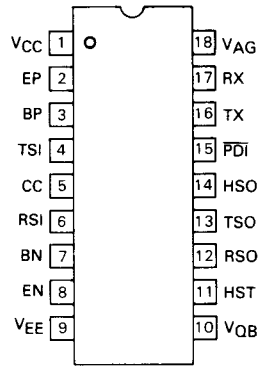
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Voltage (Referenced to V_{CC})	V_{EE} V_{QB}	−60 V_{EE} − 1	Vdc
Sense Current Steady State Pulse — Figure 4	I_{TSI}, I_{RSI}	 100 200	mAdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature (θ_{JA} = 100°C/W Typ)	T_J	150	°C

OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to +70	°C
Loop Current	I_L	20 to 120	mA
Voltage	V_{EE} V_{QB}	−20 to −56 −20 to V_{EE}	Vdc
Analog Ground (I_L = 0 to 60 mA (I_L = 0 to 120 mA)	V_{AG}	 0 to −12 −2.5 to −12	Vdc
Supervisory Output Voltage	V_{RSO}, V_{TSO}, V_{HSO}	−2.0 to −20	Vdc

PIN CONNECTIONS



PIN DESCRIPTIONS

Name	Function
V_{CC}	The most positive supply voltage. This point is Earth Ground in most typical applications.
BP & BN	Are the base drive outputs for the PNP and NPN Darlington transistors.
EP & EN	Are loop current sensing inputs and are connected to the emitter of the PNP & NPN Darlington transistors.
TSI & RSI	Are the tip and ring current sensing inputs. They are low impedance inputs (approximately 600 Ω each) that translate the voltage on tip and ring to a current through Resistors R_T and R_R.
CC	Compensation capacitor input.
V_{EE}	Is the most negative supply voltage.
V_{QB}	Is the quiet battery connection. The voltage on this pin must not go more negative than V_{EE}.
HST	Hook Status Threshold programming resistor input pin. This pin programs the value of loop resistance which determines on-hook or off-hook status.
RSO	Ring Sense current Output. This output reflects the status of the Ring terminal. The current is sourced from this output and is one-sixth I_{RSI}.
TSO	Tip Sense current Output. This output reflects the status of the Tip terminal. The current is sourced from this output and is one-sixth I_{TSI}.
HSO	Hook Status Output. This is a digital output (open collector PNP) that sources current when the loop resistance is less than the threshold resistance value set by R_H.
$\overline{PDI}$	Power-Down Input pin. A logic level "0" powers down the MC34F19.
TX	Transmit current output. This output sinks current proportional to (I_{TSI} + I_{RSI})/2.
RX	Receive input. This input sums the currents from the TX output and signal input. This pin has a low input impedance.
V_{AG}	Analog ground reference supply voltage input.

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ELECTRICAL CHARACTERISTICS (V_{EE} = −48 V, V_{QB} = −48 V, V_{AG} = −6.0 V, R_L = 900 Ω, T_A = 25°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Transhybrid Gain Variation (1.0 kHz @ 0 dBm Input) Transmission/Reception	1	V_{TX}/V_L, V_L/V_{RX}	−0.3	0	+0.3	dB
Transhybrid Rejection (1.0 kHz @ 0 dBm Input) Fixed (1%) Resistor Balance Network Trimmed Balance Network	1	V_{TX}/V_{RX}	 −23 —	 — −55	 — —	dB
Level Linearity (−48 to +3.0 dBm, referenced to output @ 1.0 kHz @ 0 dBm) Transmission Reception	1	 V_{TX}/V_L V_L/V_{RX}	 −0.1 −0.1	 0 0	 +0.1 +0.1	dB
Frequency Response (200–3400 Hz, referenced to output @ 1.0 kHz @ 0 dBm) Transmission Reception	1	 V_{TX}/V_L V_L/V_{RX}	 −0.1 −0.1	 0 0	 +0.1 +0.1	dB
Total Distortion C-Message Filtered	1	V_L/V_{RX} V_{TX}/V_L	— —	−60 −60	— —	dB
Idle Channel Noise	1	V_{TX}	—	—	10	dBrnc0
Termination Resistance Tolerance @ 1.0 kHz	1	ΔP_o	—	—	±5.0	%
Longitudinal Induction — 60 Hz (I_L = 30 to 100 mA, I_{LON} = 35 mA RMS)	2	V_{TX}	—	5.0	—	dBrnc0
Longitudinal Balance MC34F19 (200–3000 Hz) MC34F19A (200–1000 Hz) MC34F19A (3000 Hz)	2	V_{TX}/V_{LON}	 −45 −50 −48	 — — —	 — — —	dB
Propagation Delay	1	T_P, V_{RX} to V_L V_{RX} to I_{TX}	— —	750 1.2	— —	ns μs
Power Dissipation (R_L > 100 MΩ)		P_D	—	1.0	—	mW
Supply Current — On-Hook (V_{EE} = V_{QB} = −56 V, R_L > 100 MΩ)		I_{CC}	—	40	200	μA
Power Supply Noise Rejection (1.0 kHz @ 1.0 V RMS)	3	V_{TX}/v_{ee}	−40	—	—	dB
Quiet Battery Noise Rejection (1.0 kHz @ 1.0 V RMS)	3	V_{TX}/v_{qb}	—	−6.0	—	dB
Sense Current Tip Ring	4	 I_{TSO}/I_{TSI} I_{RSO}/I_{RSI}	 0.15 0.15	 0.17 0.17	 0.19 0.19	mA/mA
Fault Currents — On-Hook Tip to V_{CC} Ring to V_{CC} Tip to Ring Tip & Ring to V_{CC}	1	 I_{Tip} I_{Ring} I_{Loop} I_{Tip} & I_{Ring}	 — — — —	 0 2.5 120 2.5	 — — — —	mA
Analog Ground Current		I_{AG}	—	1.0	10	μA
Power Down Logic Levels		$I_{\overline{PDI}}$ V_{IH} V_{IL}	— −1.2 −20	−1.0 0 —	— — −4.0	μA Vdc Vdc
Hook Status Output Current (R_L < 2.5 kΩ, $\overline{PDI}$ = Logic 1) (R_L > 10 kΩ, or $\overline{PDI}$ = Logic 0)	1	I_{HSO}	 200 —	 400 0	 — 2.0	μA

FUNCTIONAL DESCRIPTION

Referring to the functional block diagram, line-sensing resistors at TSI and RSI convert voltages at the Tip and Ring terminals into currents which are fed into current mirrors* A1 and A2. The output of A1 is mirrored by A3 and summed together with an output of A2 at the TX terminal. Thus, a differential to single-ended conversion is performed from the ac line signals to the TX output.

All the dc current at the TX output is fed back through the RX terminal to the B1 mirror input. The inputs to B1 and B2 are made equal by mirroring the B1 input current to the B2 input through a low gain output (x1) of the B1 mirror. Both B1 and B2 mirrors have high gain outputs (x95) which drive the subscriber lines with balanced currents that are equal in amplitude and 180° out of phase. The feedback from the TX output, through the B-Circuit mirrors, to the subscriber line produces a dc feed resistance significantly less than the loop sensing resistors.

In most line-interface systems, the ac termination impedance is desired to be greater than the dc feed impedance. A differential ac generator on the subscriber loop would be terminated by the dc feed impedance if the total ac current at the TX output were returned to the B1 input along with the dc current. Instead, the MC34F19 system diverts part of the ac current from the B-Circuit mirrors. This decreases the ac feedback current, causing the ac termination impedance at the line interface to be greater than the dc feed impedance.

The ac current that is diverted from the B1 mirror input is coupled to a current-to-voltage converter circuit that has a low input impedance. This circuit consists of an op amp and a feedback resistor external to the MC34F19 which produce the transmit output at the 4-wire interface. The transhybrid transmission gain is programmed by the op amp feedback resistor.

Transhybrid reception is realized by converting the ac coupled receive input voltage to a current through an external resistor at the low impedance RX terminal. This current is summed at RX with the dc and ac feedback current from the A-Circuit mirror and drives the B1 mirror input. The B-Circuit mirror outputs drive the line with balanced ac current proportional to the receive input voltage. The transhybrid reception gain is programmed by the resistor at the RX input.

Since receive input signals are transmitted through the MC34F19 to the 2-wire port, and the 2-wire port signals are returned to the 4-wire transmit output, a means of cancellation must be provided to maintain 4-wire signal separation (transhybrid rejection). Cancellation is complicated because the gain from the receive port to the transmit port depends on the impedance of the subscriber loop. A passive "balance network" is used to achieve transhybrid rejection by cancelling, at the low impedance input to the transmit op amp, the current reflected by the loop impedance to the 4-wire transmit output. For a resistive loop impedance, a single resistor provides the cancellation. For reactive loops, the balance network should be reactive.

Longitudinal (common-mode) currents that may be present on the subscriber lines are suppressed in the MC34F19 by two methods. The first mode of suppression is inherent in the mirror configuration. Positive-going longitudinal currents into Tip and Ring create common-mode voltages that cause a decreasing current through the Tip Sensing resistor and an increasing current through the Ring Sensing resistor. When these equal and opposite signal currents are reflected through the A-Circuit and summed together at TX, the total current at TX remains unchanged. Therefore, the ac currents due to the common-mode signals are cancelled before reaching the transmit output.

The second longitudinal suppression method is dominant, since it limits the amplitude of common-mode voltages that appear at the Tip and Ring terminals. Through an error-detecting circuit, the input of which is a difference current between outputs of A1 and A2, the impedance at Tip and Ring to longitudinal currents is kept very low. This is accomplished with a high gain C-Circuit which produces B1 and B2 output currents that are equal and in phase to cancel the longitudinal line currents. Operation of this circuit does not affect the dc line-current or the processing of normal differential line signals.

The hook-status control circuit supplies the bias currents to activate the B-Circuit op amps and other sections of the MC34F19. If the $\overline{PDI}$ pin is a logic "one," the control circuit senses two outputs from the A1 and A2 mirrors. If both of these output currents are greater than the preprogrammed current at the HST terminal, the control circuit supplies currents to power up the SLIC. At the same time it activates a digital status output, HSO.

In addition to the digital hook status output, the condition of Tip and Ring can be monitored at the TSO and RSO outputs of the MC34F19. These outputs source currents proportional to the TSI and RSI input currents respectively, and operate independently of the $\overline{PDI}$ logic input.

The MC34F19 has two negative battery terminals. V_{EE} supplies the high current through the B2 mirror to drive the line. B2 has a high output impedance and battery noise will not be coupled to the line from the V_{EE} terminal. However, V_{QB} is quite sensitive to noise, since the line-sensing resistor is referenced to this pin through the A2 mirror, and should be bypassed with a filter network to guarantee a high rejection of battery noise.

The V_{AG} input also plays a key role in reducing power-supply related noise that can occur when the MC34F19 system is coupled to a switching system. The analog ground isolates the 4-wire receive and transmit signal paths from noise on the system power ground by establishing a common ac signal reference.

*A current mirror is a circuit which behaves as a current controlled, current source. It has a single low-impedance input terminal and one or more high impedance outputs.

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FIGURE 1 — AC TEST CIRCUIT

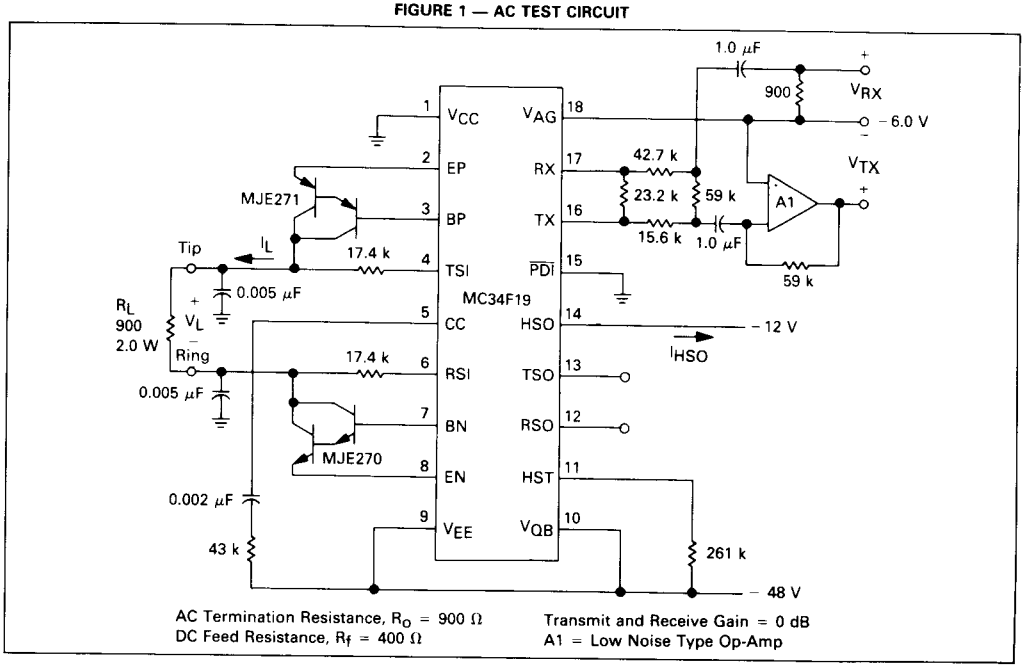

FIGURE 2 — LONGITUDINAL BALANCE TEST CIRCUIT

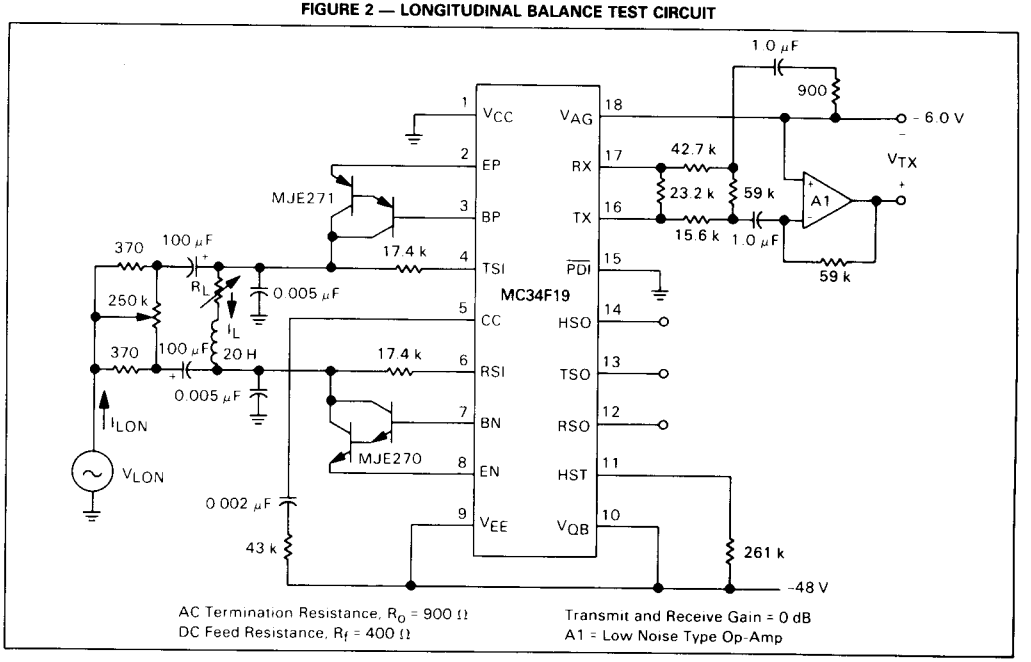

FIGURE 3 — SUPPLY NOISE REJECTION TEST CIRCUIT

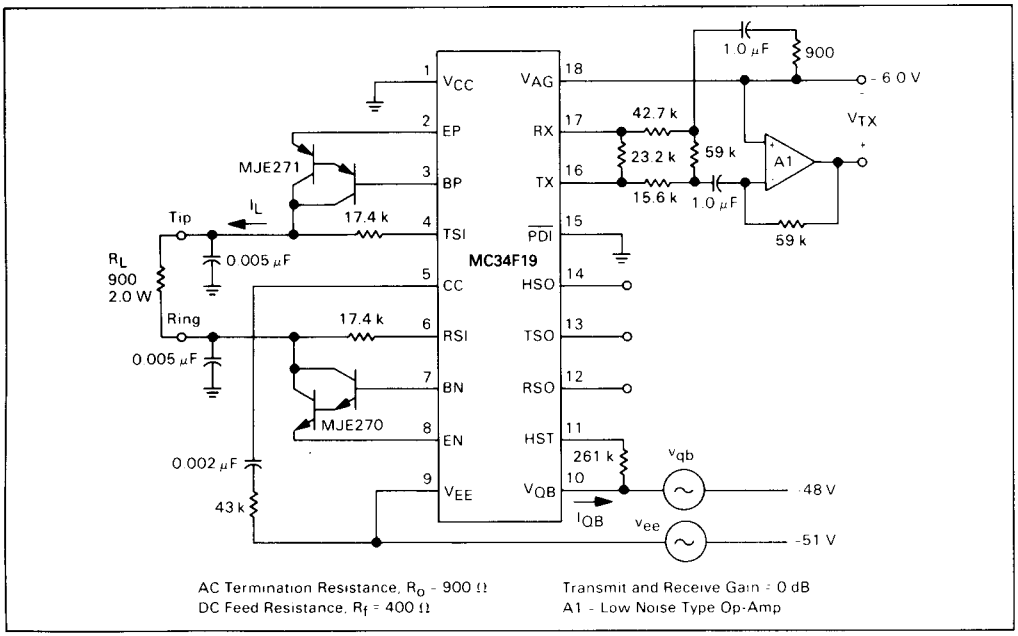

FIGURE 4 — TSO AND RSO SUPERVISORY OUTPUT TEST CIRCUIT

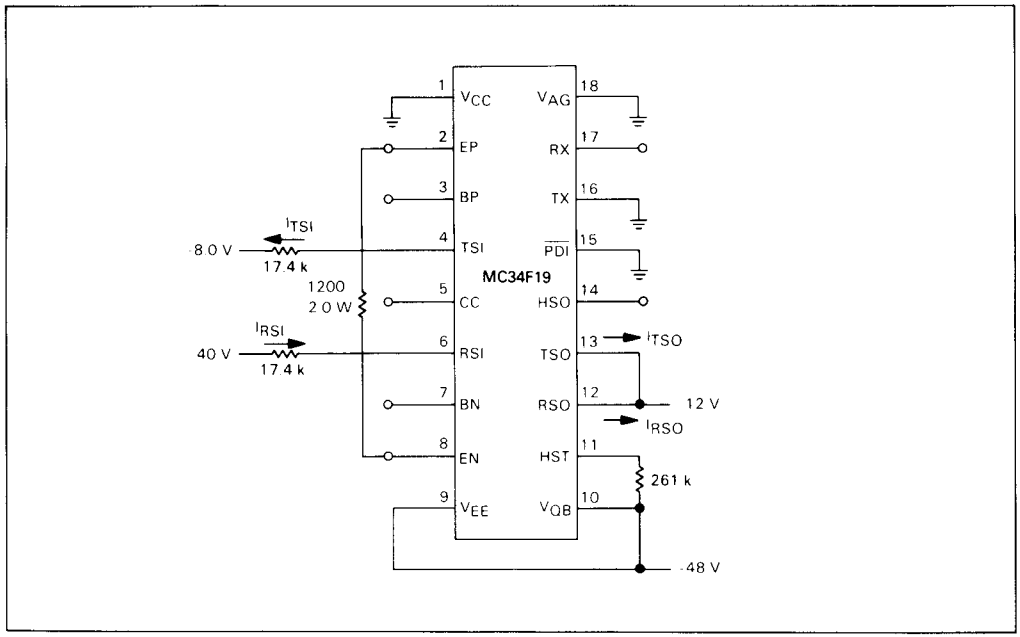

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FIGURE 5 — QUIET BATTERY versus LOOP CURRENT

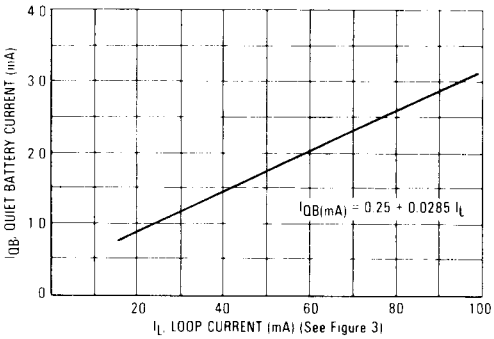
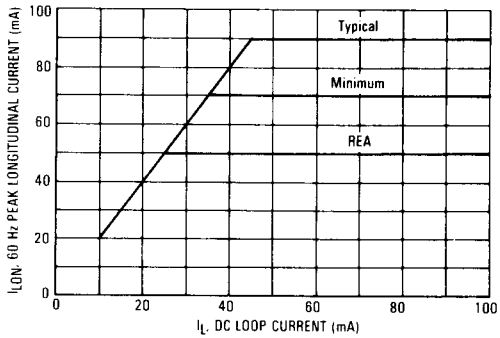


FIGURE 6 — LONGITUDINAL CAPACITY



APPLICATIONS INFORMATION

The Motorola Subscriber Loop Interface Circuit (SLIC) is comprised of a bipolar laser-trimmed integrated circuit, MC34F19, two complimentary Darlington power transistors, MJE270 and 271, a bridge rectifier, MDA220, ten resistors, and five capacitors, as shown in Figure 7. The op amp providing the V_{TX} output may be a separate component or may be one of the two op amps included in the MC14413 or MC14414 PCM filter packages. The circuit of Figure 7 will provide:

- Adjustable resistive dc power feed
- Adjustable maximum loop range
- Adjustable ac termination impedance
- 2-wire balanced to 4-wire single ended conversion
- Adjustable transmit and receive gains
- Independent transhybrid null
- Ring-to-ground, Tip-to-ground, and Ring- and Tip-to-ground fault current limiting (2.5 mA)
- Rejection of longitudinal or common mode interference from dc to greater than 4.0 kHz
- 1500 volt secondary lightning transient protection
- Temporary power-line fault protection
- On-hook power-down (less than 10 mW)
- Floating 4-wire common input for noise rejection
- Hook-status output signal
- Power-down control for subscriber service denial
- Continuous Tip and Ring status monitoring outputs
- Wide battery range (20 V to 56 V)

In addition, the SLIC can provide the following optional features:

- Constant current battery feed
- Current limiting battery feed
- Battery noise suppression
- Adjustable frequency response

DC Characteristics

When the telephone is on-hook, the Tip and Ring terminals of the SLIC are essentially open and the MC34F19 is in a quiescent state. In this condition, current is being supplied to the line only through R_R and R_T and power dissipation in the MC34F19 is limited primarily to leakage currents.

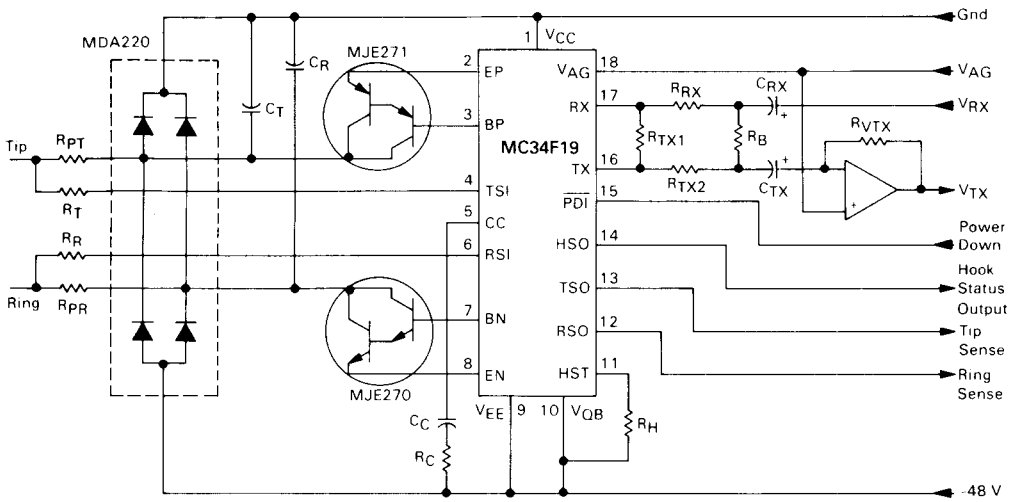
In the off-hook state, the MC34F19 powers itself up and provides current to the line. The off-hook dc feed resistance with which the SLIC drives the line is given by

$$R_F = \frac{(R_R + R_T + 1200)|V_{QB}|}{98\,(|V_{QB}| - 4)} \quad (1)$$

The v alues of R_R and R_T can be derived from equation (1) to provide the desired dc feed resistance once V_{QB} is known.

$$R_R = R_T = \frac{49\,(|V_{QB}| - 4)\,R_F}{|V_{QB}|} - 600 \quad (2)$$

FIGURE 7 — SLIC CIRCUIT



The line-feed current flows between ground and V_{EE}; however, the control electronics is referenced to V_{QB} and ground. Therefore, the dc feed resistance appears to be referenced to V_{QB} and ground.

The matching of R_R and R_T is critical to a number of ac performance parameters as shown in Figures 8, 9 and 10. One percent tolerance or better is recommended for these resistors. In addition, these resistors must withstand any voltage transients on the line. Resistors able to withstand voltage transients of 1000 V or more are recommended.

FIGURE 8 — RETURN LOSS versus TIP/RING RESISTOR MISMATCH

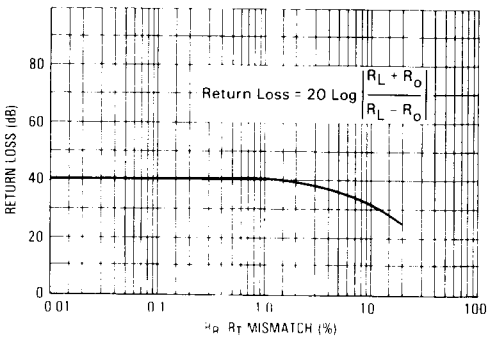
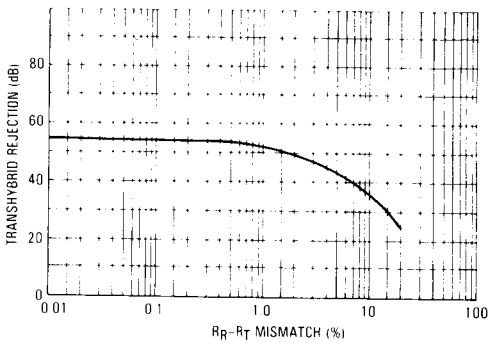


FIGURE 9 — TRANSHYBRID REJECTION versus TIP/RING RESISTOR MISMATCH



Power dissipation on short loops can be significantly reduced by either of two methods of current limiting. The dc feed resistance R_F is shown in equation (1) to be a function of V_{QB} as well as R_T and R_R. The current I_{QB} from the V_{QB} pin is proportional to loop current. Therefore, a resistor R_{QB} placed between the V_{QB} pin and V_{EE} supply will reduce the V_{QB} supply voltage as the loop current increases. This slightly increases the value of R_F while at the same time reducing the effective value of the battery voltage, thereby limiting loop current. Figure 11 can be used to determine the value of R_{QB} that will yield the desired maximum loop current.

FIGURE 10 — IMPEDANCE BALANCE versus TIP/RING RESISTOR MISMATCH

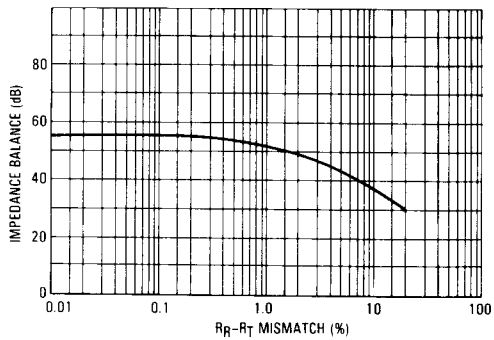


FIGURE 11 — LOOP CURRENT versus LOOP RESISTANCE

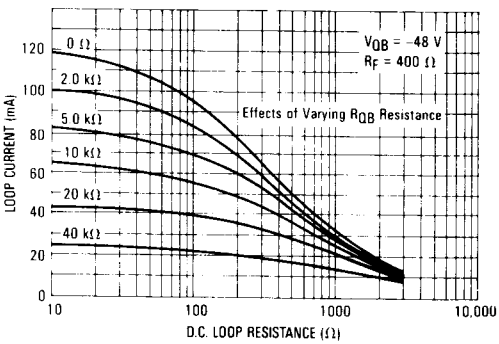


Figure 20 shows how a current regulator device can be used in place of R_{QB} to provide a constant current line-feed characteristic up to the loop resistance where the constant current equals the resistive feed current. At that point, the line-feed will appear resistive. Typical current regulator values for various loop currents are shown in Figure 12. The Motorola 1N5283 series of current regulator diodes are recommended. The current sourced to the current regulator diode in the off-hook mode is:

$$I_{QB} = 0.0285\, I_L + 0.25 + \frac{|V_{QB}| - 4}{R_H} \qquad 3(a)$$

I_L in mA, R_H in kΩ

FIGURE 12 — LOOP CURRENT REGULATION

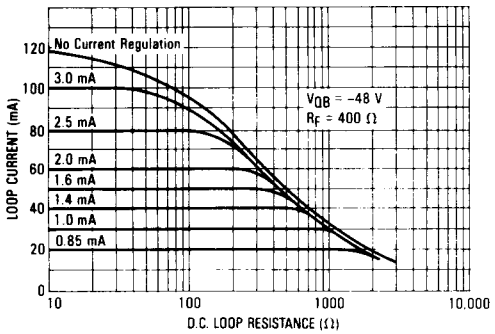


FIGURE 13 — TOTAL SLIC POWER DISSIPATION

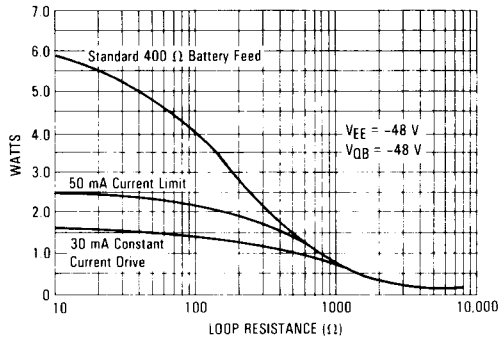


FIGURE 14 — HOOK STATUS DETECTION

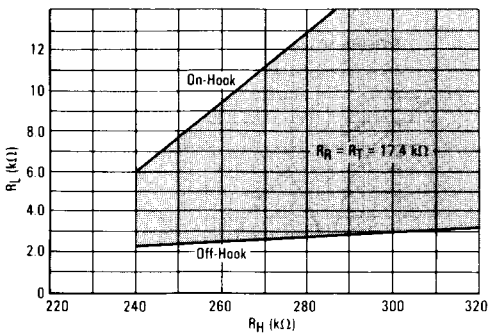
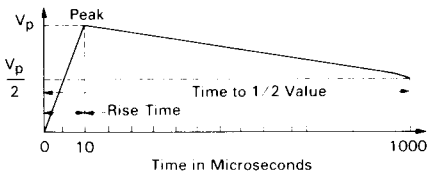


FIGURE 15 — TRANSIENT VOLTAGE WAVE SHAPE



In the on-hook mode the current is:

$$I_{QB} = 2.15\ I_{RSI} + 0.7\ I_{TSI} \qquad 3(b)$$

Figure 13 is a graph of SLIC power dissipation for both 400 Ω resistive battery feed and constant current battery feed, (or current limiting) showing the power savings of constant current techniques.

Either R_{QB} or the current regulator diode and a capacitor to V_{CC} provide an effective means of filtering any noise on the V_{EE} line and prevent it from reaching the V_{QB} pin.

The loop resistances which the SLIC recognizes as on-hook and off-hook are determined by R_H.

$$R_L \text{ (On-Hook)} \geq 0.17\ R_H - (R_R + R_T) \qquad 4(a)$$

$$R_L \text{ (Off-Hook)} \leq 0.011\ R_H - 0.010\ (R_R + R_T) \qquad 4(b)$$

The value of R_H can be selected from Figure 14. All loop resistances below the shaded area at the point where R_H was selected are recognized as off-hook. All loop resistances above the shaded area at the value of R_H are recognized as on-hook. The shaded area represented an undefined region where the hook status output may indicate either on-hook or off-hook due to element tolerances and comparator hysteresis.

Transient Protection

The SLIC shown in Figure 7 will withstand positive or negative voltage transients on Tip and Ring up to 1500 V_{peak} having the waveshape shown in Figure 15. The resistors R_{PT}, R_{PR}, R_T, and R_R must be chosen to withstand such a voltage transient without arching across or failing due to the resulting current surge. The values of R_{PT} and R_{PR} should be between 30 and 50 Ω. Tolerance of 20% is adequate. The values of R_T and R_R are determined per equation (2). The peak currents at RSI and TSI should not exceed 200 mA during these transients.

The circuit of Figure 7 will also withstand crosses to ac power lines of up to 700 V_{RMS} for 11 cycles of the 60 Hz line per REA Form 522a. The ability to withstand continuous power-line crosses is determined mainly by the power handling ability of R_{PT}, R_{PR}, R_T, and R_R. The circuit wiring to the MDA220 diode bridge must be adequate to handle the large voltages and currents caused by transients, as well.

None of the pins on the MC34F19 should be operated more positive than V_{CC} or more negative than V_{EE}. However, under transient conditions, EP and BP may

go up to one volt more positive than V_{CC} and BN, EN, and V_{QB} may go up to one volt more negative than V_{EE} without permanent damage to the MC34F19. When a capacitor is used on the V_{QB} pin in conjunction with R_{QB}, a 1N4001 or similar diode is recommended between V_{EE} and V_{QB}. The diode cathode should be connected to V_{QB}. For single short transients of less than one millisecond, EP and BP may exceed V_{CC} and EN and BN may exceed V_{EE} by up to 30 V.

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Transmission Characteristics

The ac termination impedance R_O of the SLIC is determined by R_T, R_R, and the ratio of R_{TX2} to $R_{TX}1$.

$$R_O = \frac{R_T + R_R + 1200}{1 + 97K_5} \quad (5)$$

$$K_5 = \frac{R_{TX2}}{R_{TX2} + R_{TX1}} \quad (6)$$

The required value of K_5 is derived from equation (5) after choosing R_O.

$$K_5 = \frac{1}{97}\left[\frac{R_T + R_R + 1200}{R_O} - 1\right] \quad (7)$$

The value of R_{TX1} must be selected first to assure that the internal current mirrors in the MC34F19 do not saturate at the minimum voltage provided at V_{QB}. The value of R_{TX1} is determined by:

$$R_{TX1} = \frac{(R_R + R_T + 1200)(|V_{QB}|\ \text{min} - |V_{AG}|\ \text{max} - 6.5)}{|V_{QB}|\ \text{min} - 5.4} \quad (8)$$

If current limiting or constant current-feed is used where the minimum value of V_{QB} may not be known, R_{TX1} is found by:

$$R_{TX1} = \frac{0.01\ L_{L(max)}(R_R + R_T + 600) - |V_{AG}|(max) - 3.9}{0.01\ I_{L(max)}} \quad (9)$$

The value of R_{TX2} may be derived from equation (6).

$$R_{TX2} = \frac{K_5 R_{TX1}}{1 - K_5} \quad (10)$$

Transhybrid reception gain (G_{RX}) from V_{RX} to Tip and Ring is given by:

$$G_{RX} = \frac{95\ R_L\ R_O}{(R_L + R_O)\ R_{RX}} \quad (11)$$

The value of R_{RX} may be calculated to provide the desired G_{RX} for a given R_O and R_L.

$$R_{RX} = \frac{95\ R_L\ R_O}{(R_L + R_O)\ G_{RX}} \quad (12)$$

Transhybrid transmission gain (G_{TX}) from Tip and Ring to V_{TX} is given by:

$$G_{TX} = \frac{1.02\ R_{VTX}\ (1 - K_5)}{R_R + R_T + 1200} \quad (13)$$

The value of R_{VTX} may be calculated to provide the desired G_{TX}.

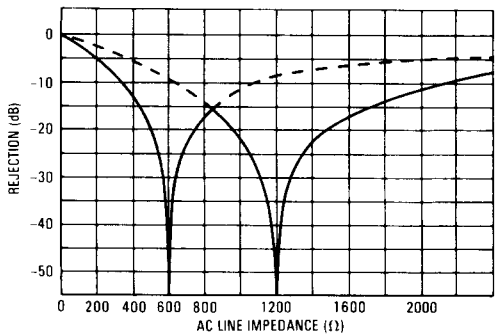
$$R_{VTX} = \frac{(R_R + R_T + 1200)\ G_{TX}}{1.02\ (1 - K_5)} \quad (14)$$

Transhybrid rejection is achieved with the SLIC by taking advantage of the 180° phase reversal of the current at the TX pin with respect to the V_{RX} input. A balance resistor, R_B, is placed between the V_{RX} input and the virtual ground point between C_{TX} and R_{TX2}. The value of this resistor is selected to exactly cancel out the return current from the TX pin and is determined by:

$$R_B = \frac{R_{RX}(1 + 97K_5)(R_O + R_L)}{97(1 - K_5)(R_L)} \quad (15)$$

Maximum rejection will only occur at one value of R_L across Tip and Ring, as shown in Figure 16, for a given value of R_B. Figure 16 shows that more than one value of R_B may be required to provide adequate rejection over wide ranges of loop resistance.

FIGURE 16 — TRANSHYBRID REJECTION



Maximum rejection on a line that is reactive can be obtained with the circuit shown in Figure 17. This will balance any capacitive load on the line, where

$$R_{B1} = \frac{R_{RX}(R_R + R_T + 1200)}{97\ R_L\ (1 - K_5)} \quad (16)$$

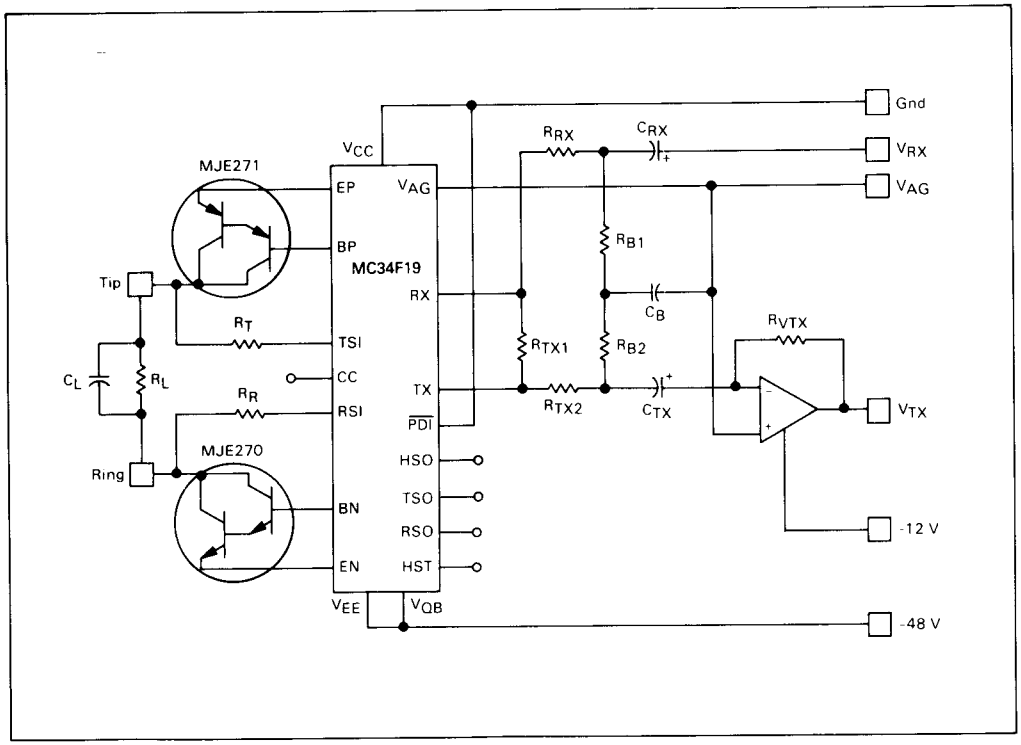
$$R_{B2} = \frac{R_{RX}(R_R + R_T + 1200)}{97\ R_O\ (1 - K_5)} \quad (17)$$

$$C_B = \frac{R_L\ C_L}{R_{B2}} \quad (18)$$

Signaling and Supervision

The $\overline{PDI}$ function shuts off all power to the subscriber with the exception of the small current provided by R_R and R_T. The power-down state occurs when a logic low-level, any voltage more negative than $V_{CC} - 4.0$ V but not exceeding -20 V, is applied to the $\overline{PDI}$ pin.

FIGURE 17 — BALANCE NETWORK FOR REACTIVE LINES



The $\overline{PDI}$ pin is designed to be TTL compatible if the logic power supplies are 0 V and −5.0 V. It is also compatible with CMOS powered from 0 V and −12 V supplies, otherwise a level-shifter is required. If the power-down feature is not desired, this pin can be tied to V_{CC}.

Hook status is indicated by the presence or absence of current at the Hook Status Output (HSO). On-hook status is indicated by no current output at HSO. When an off-hook condition is detected by the MC34F19, the HSO pin sources a dc current of at least 200 μA. A resistor can be used to translate the current into a voltage for further processing by the digital logic. This pin also passes dial pulse information. If the $\overline{PDI}$ pin is at a logic low level, HSO is inactive.

Figures 18 (a), 18 (b), and 18 (c) show suggestions for interfacing with various digital logic levels.

The Tip Sense Output (TSO) and the Ring Sense Output (RSO) both source current that is proportional to the current that flows into and out of their respective inputs — the Tip Sense Input (TSI) and Ring Sense Input (RSI). The output currents are 1/6 that of the input currents. These outputs may be used as full time monitors of the line condition since they remain active even if the MC34F19 is in the power-down state. Figure 19 shows how these outputs can be used for the ring-trip function and ring-fault indicator.

Ringing is the last function to describe on Figure 19. There are several ways of inserting the ringing signals on a line, any one of which the SLIC can be adapted to. Figure 19 shows one method.

When the ringing relay is enabled, the ring side of the SLIC is disconnected. The tip side of the line is connected to a grounded resistor (R_{G1}) to provide a complete signal path for the ring generator signal. While the phone is on-hook, the ringing signal is capacitively coupled to the tip line through the high impedance of the bell ringer and a capacitor in the phone. The dc currents are low and therefore the dc voltage drop

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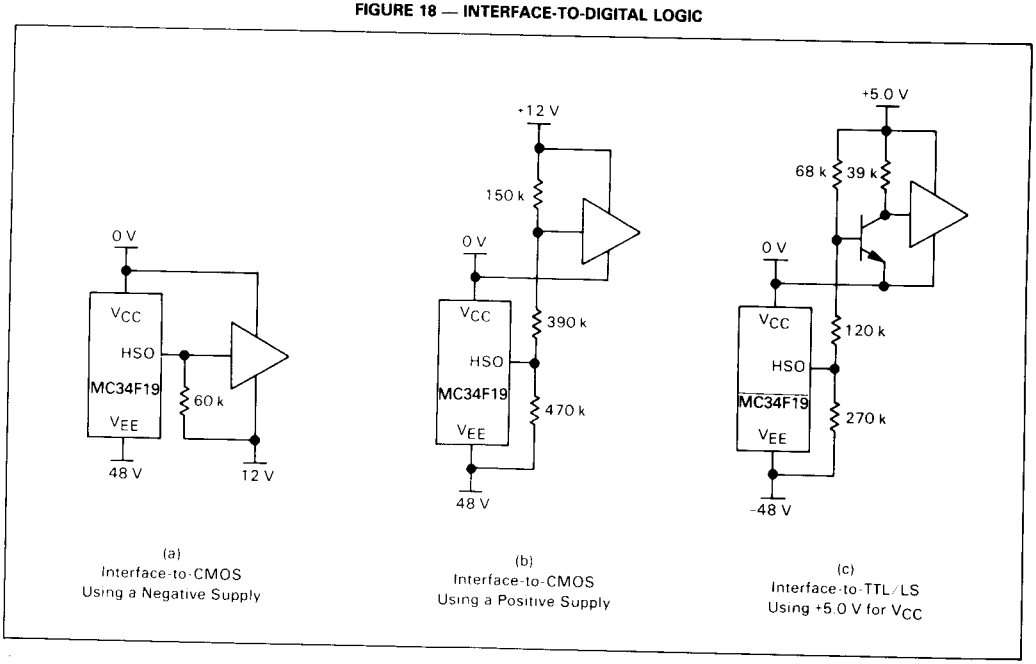
FIGURE 18 — INTERFACE-TO-DIGITAL LOGIC



across R_{G1} is low. When the subscriber goes off-hook, the impedance of the phone drops to a few hundred Ω of dc resistance and R_{G1} gets a large dc current along with a large ac current. The sensing resistor (R_T) will sense this change and the TSO output of the MC34F19 will also reflect this change by an increased voltage drop on the R_{TS} resistor. The capacitor (C_{TS}) will filter the ac component of the signal. A comparator can now be used to determine the hook status and disable the ring delay.

Design Example

This example will illustrate the design procedure for a SLIC to meet the following specifications:

$V_{EE} = -48\ V \pm 6.0\ V$
$V_{AG} = -6.0\ V \pm 1.0\ V$
400 Ω resistive dc feed
Current limiting at 60 mA
Maximum loop resistance of 2500 Ω
900 Ω ac termination resistance
Transmit gain of 0 dB
Receive gain of 0 dB
Balanced for 600 Ω line resistance

The V_{QG} supply will be derived from the −48 V V_{EE} supply through a 1N5305 current regulator diode to provide loop current limiting at 60 mA. The voltage drop across the 1N5305 is less than 2.0 V until it reaches regulation and may be ignored in the calculation of R_T and R_R. C_{QB} is 10 μF at 60 V. From equation (2).

$$R_T = R_R = \frac{49\,(48-4)\,400}{48} - 600$$
$$= 17367\ \Omega$$

The closest standard value with ±1.0% tolerance is 17.4 kΩ. 17.4 kΩ will be used in all the rest of the equations.

The protection resistors (R_{PR} and R_{PT}) should be 30 Ω to 50 Ω. For this example we will use 40 Ω ±20%. C_T and C_R are stabilization capacitors whose values, including line capacity, should be a minimum of 2000 pF.

R_C and C_C are determined by $(R_T + 600)\ C_T = R_C C_C$. 18 kΩ ±5.0% and 2000 pF will be used for R_C and C_C.

The value of R_H is determined from Figure 14. To guarantee off-hook detection at the maximum loop resistance of 2500 Ω, R_H can be 261 kΩ ±1.0%, which is a standard value. A 270 kΩ ±5.0% resistor can be used if the on-hook resistance of the loop is specified larger than 14 kΩ.

To obtain the desired 900 Ω ac termination resistance (R_O), K_5 is first calculated using equation (7).

$$K_5 = \frac{1}{97}\left[\frac{17400 + 17400 + 1200}{900} - 1\right]$$
$$= 0.402$$

The value of R_{TX1} is calculated from equation (9) since V_{QB} is supplied from a current regulator diode.

$$R_{TX1} = \frac{(0.01)(0.06)(17400 + 17400 + 600) - 7 - 3.9}{(0.01)(0.06)}$$

$$= 17233\ \Omega$$

17233 Ω is the largest value of R_{TX1} that can be used. A 16.9 kΩ ±1.0% resistor is the standard value selected. From equation (10), R_{TX2} is now calculated.

$$R_{TX2} = \frac{(0.402)(16900)}{(1 - 0.402)}$$

$$= 11361\ \Omega$$

A 11.3 kΩ ±1.0% resistor is selected. When selecting R_{TX2}, select the nearest standard value lower than the calculated value. This is because C_{TX} adds a small impedance to the value of R_{TX2} and the virtual ground node (negative input to the current to voltage converter) will also add a slight amount of impedance to R_{TX2}. The impedance of the virtual ground point is

$$Z_{in} = \frac{R_{VTX}}{1 + A}$$

where A is the open loop gain of the op amp. At 1.0 kHz, Z_{in} will probably range from 50 Ω to 100 Ω. The C_{TX} capacitor, 1.0 μF (50 V) adds a reactance of 160 Ω to the value of R_{TX2} so the total impedance is:

$$\sqrt{(11300 + 75)^2 + (160)^2} = 11376\ \Omega$$

With the nominal values selected for R_{TX1}, R_{TX2}, C_{TX} and Z_{in}, K_5 nominal value is 0.4007 and R_O nominal value is 903 Ω.

Transhybrid reception gain (G_{RX}) is set to 0 dB (voltage gain of one) by calculating R_{RX} using equation (12). A nominal line resistance (R_L) of 900 Ω will be assumed.

$$R_{RX} = \frac{(95)(900)(903)}{(900 + 903)(1)}$$

$$= 42821\ \Omega$$

A 43.2 kΩ ±1.0% resistor should be used for R_{RX}. Use a 1.0 μF 20 V capacitor for C_{RX}.

Transhybrid transmission gain (G_{TX}) is set for unity gain by calculating R_{VTX}, using equation (13).

$$R_{VTX} = \frac{(17400 + 17400 + 1200)(1)}{(1 - 0.4007)}$$

$$= 60070\ \Omega$$

A 60.4 kΩ ±1.0% resistor should be used for R_{VTX}.

The balance resistor (R_B) is selected to maximize transhybrid rejection with R_L of 600 Ω using equation (15).

$$R_B = \frac{43200\ [1 + 97\ (0.4007)]\ (903 + 600)}{97\ (1 - 0.4007)(600)}$$

$$= 74216\ \Omega$$

A 75 kΩ ±1.0% resistor would be selected.

The digital Hook Status Output resistor (R_{HS}) is determined from a consideration of the type of logic with which the output must interface and the power supply voltages of that logic. Assuming CMOS at V_{DD} = 0 V and V_{SS} = 12 V, then

$$R_{HS} = \frac{V_{SS}}{I_{HS}}$$

$$= \frac{12\ V}{200\ \mu A}$$

$$= 60\ k\Omega$$

A 62 kΩ ±5.0% resistor is suitable.

The complete SLIC design is shown in Figure 20, along with the codec, filter, time-slot assigner/channel controller, and reference voltage needed for a complete line circuit.

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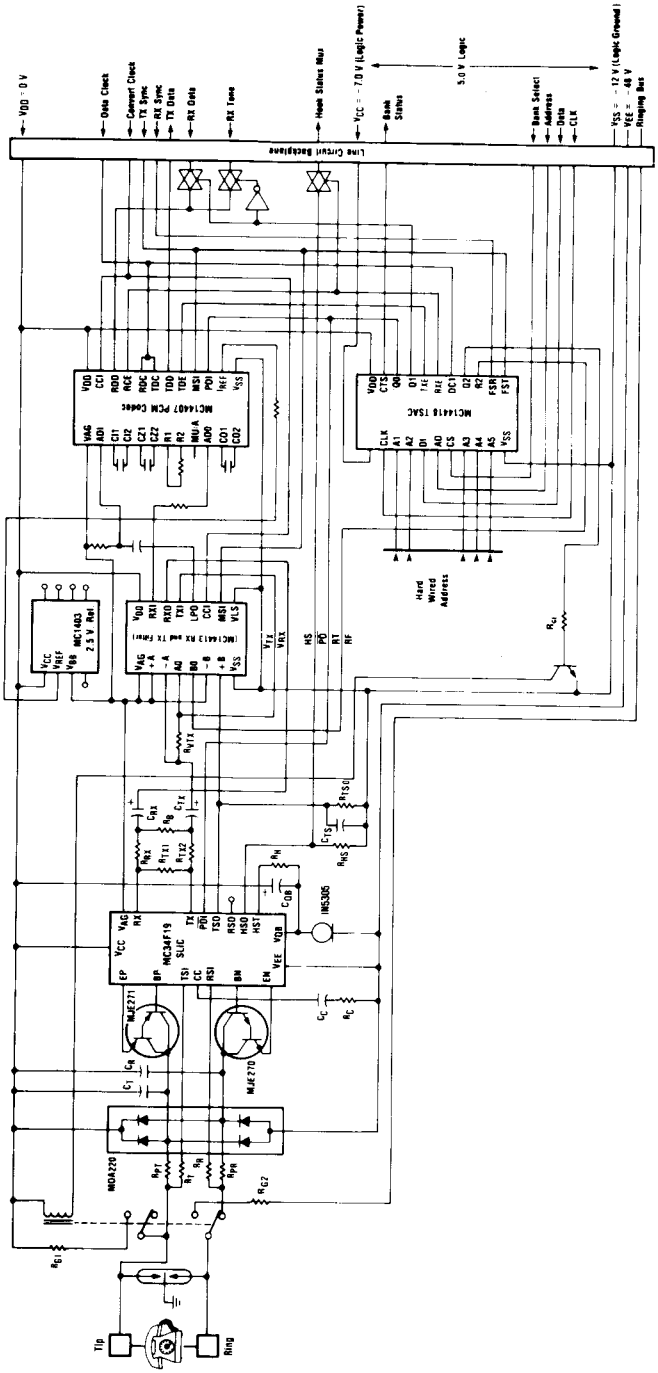

FIGURE 20 — LINE CIRCUIT USING SLIC, FILTER, CODEC AND TSAC

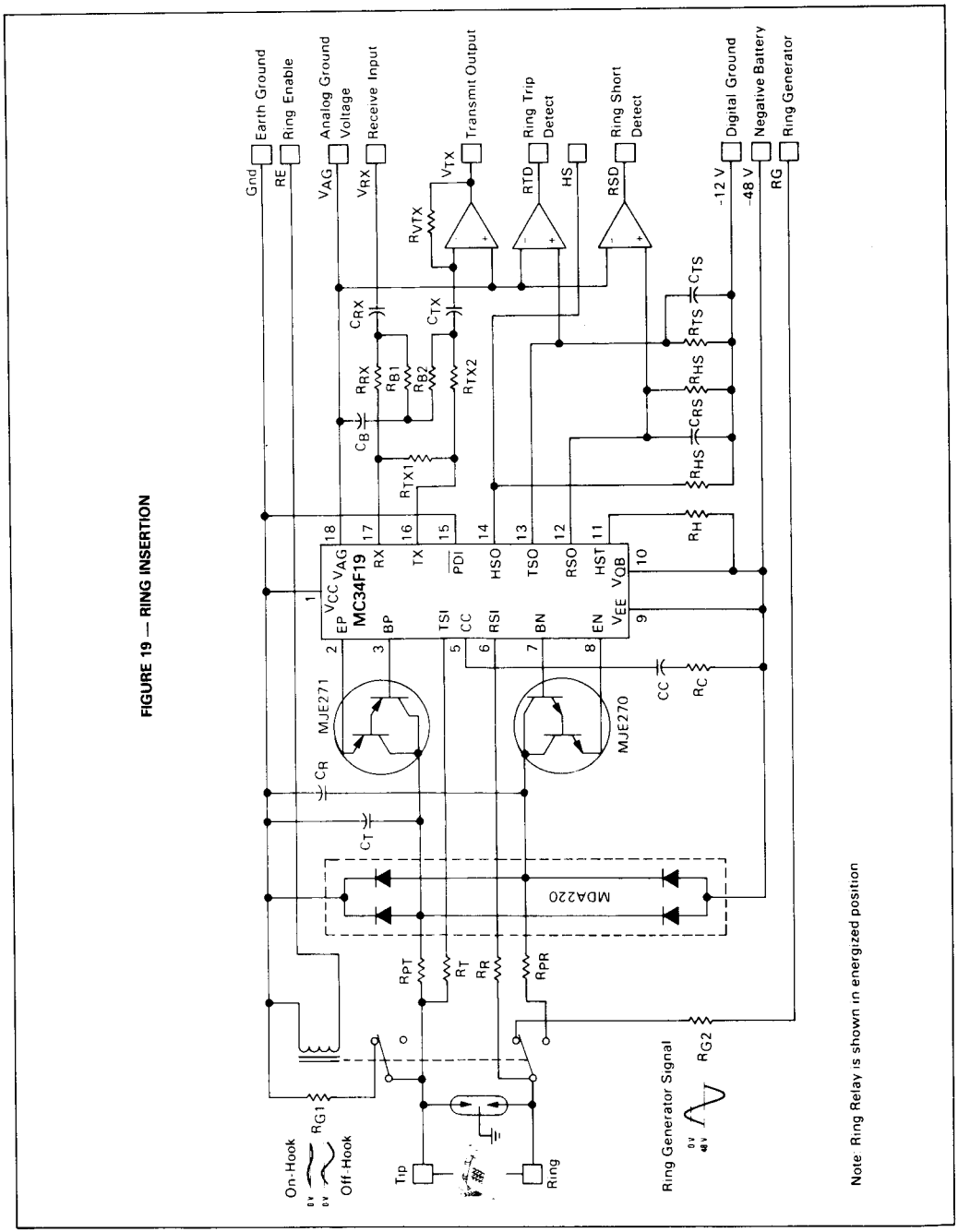

FIGURE 19 — RING INSERTION