

FEATURES

- Functionally compliant with ANSI X3T11 Fibre Channel physical and transmission protocol standards and Gigabaud Link Module Specification
- Fast RX PLL acquisition
- S2051 receiver PLL configured for clock and data recovery
- 1062, 531 and 266 Mb/s operation
- 10- or 20-bit parallel TTL compatible interface
- 0.8W Typical power dissipation for chipset
- +3.3V/+5V power supply
- Low-jitter serial PECL compatible interface
- Lock detect
- Local loopback
- 10mm x 10mm 52 PQFP package
- Fibre Channel framing performed by receiver
- Continuous downstream clocking from receiver
- TTL compatible outputs possible with +5V I/O power supply

APPLICATIONS

High-speed data communications

- Supercomputer/Mainframe
- Workstation
- Switched networks
- Proprietary extended backplanes
- Mass storage devices/RAID drives

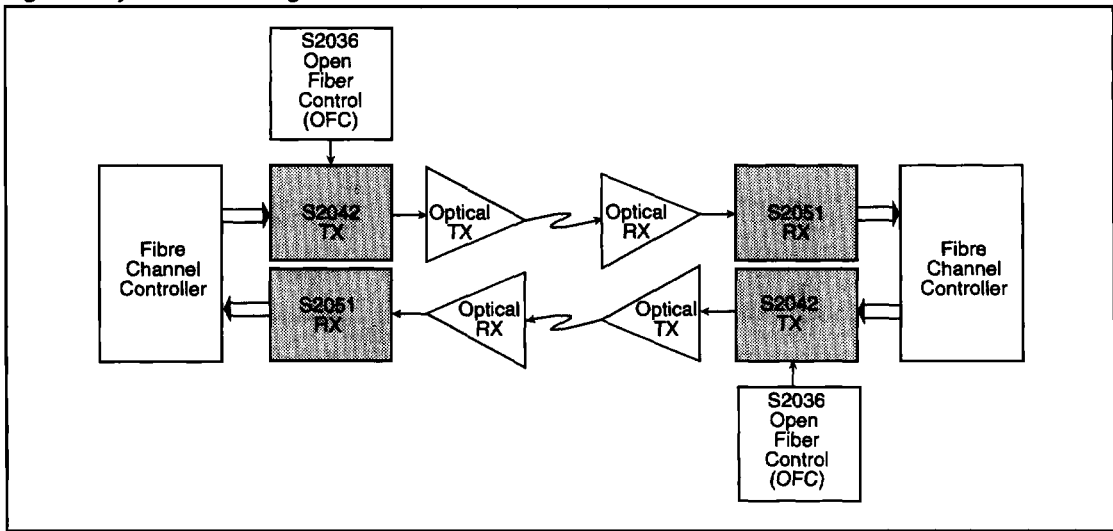
GENERAL DESCRIPTION

The S2051 receiver is designed to perform high-speed serial data reception over fiber optic or coaxial cable interfaces conforming to the requirements of the ANSI X3T11 Fibre Channel specification. The RX is selectable to 1062, 531 or 266 Mbit/s data rates with associated 10- or 20-bit data word. The chipset is GLM compliant.

The RX performs serial-to-parallel conversion and framing for block-encoded data. The S2051 on-chip PLL synchronizes directly to incoming digital signals to receive the data stream. The receiver supports differential PECL-compatible I/O for fiber optic component interfaces, to minimize crosstalk and maximize data integrity. Local loopback allows for system diagnostics. The TTL I/O section can operate from a +3.3V power supply. With a 3.3V power supply the RX dissipates only 0.8W typically.

Figure 1 shows a typical network configuration incorporating the S2042 and S2051.

Figure 1. System Block Diagram



OVERVIEW

The S2051 receiver provides deserialization for block-encoded data to implement a Fibre Channel interface. Operation of the S2042/S2051 chips is straightforward, as depicted in Figure 2. The sequence of operations is as follows:

Transmitter

1. 10/20-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver

1. Clock and data recovery from serial input
2. Serial-to-parallel conversion
3. Frame detection
4. 10/20-bit parallel output

The 10/20-bit parallel data handled by the S2051 should be from a DC-balanced encoding scheme, such as the 8B/10B transmission code, in which information to be transmitted is encoded 8 bits at a time into 10-bit transmission characters.

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figure 4.

A lock detect feature is provided on the S2051, which indicates whether the PLL is locked (synchronized) to the reference clock or the data stream.

Loopback

Local loopback is supported by the chipset, and provides a capability for performing offline testing of the interface to ensure the integrity of the serial channel before enabling the transmission medium. It also allows for system diagnostics.

Figure 2. Fibre Channel Interface Diagram

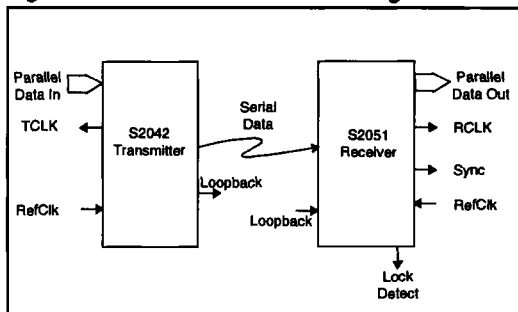


Figure 3. S2051 Functional Block Diagram

