

Dual 2-Wide 2-3-Input OR-AND/OR-AND Gate

The MC10H117 dual 2-wide 2-3-input OR-AND/OR-AND-Invert gate is a general purpose logic element designed for use in data control, such as digital multiplexing or data distribution. Pin 9 is common to both gates. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 100 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply ($V_{CC} = 0$)	V_{EE}	-8.0 to 0	Vdc
Input Voltage ($V_{CC} = 0$)	V_I	0 to V_{EE}	Vdc
Output Current— Continuous	I_{out}	50	mA
— Surge		100	
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range— Plastic	T_{stg}	-55 to +150	°C
— Ceramic		-55 to +165	°C

ELECTRICAL CHARACTERISTICS ($V_{EE} = -5.2 \text{ V} \pm 5\%$) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	29	—	26	—	29	mA
Input Current High Pins 4, 5, 12, 13 Pins 6, 7, 10, 11 Pin 9	I_{inH}	—	465	—	275	—	275	μA
		—	545	—	320	—	320	
		—	710	—	415	—	415	
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Parameter	Symbol	0.45	1.35	0.45	1.35	0.5	1.5	ns
Propagation Delay	t_{pd}							
Rise Time	t_r	0.5	1.5	0.5	1.6	0.5	1.7	
Fall Time	t_f	0.5	1.5	0.5	1.6	0.5	1.7	

NOTE:

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

MC10H117



L SUFFIX
CERAMIC PACKAGE
CASE 620-10

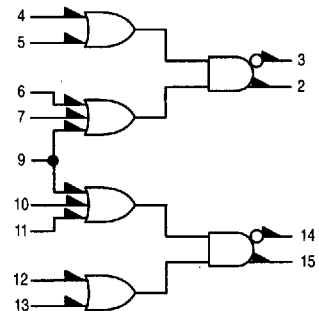


P SUFFIX
PLASTIC PACKAGE
CASE 648-08



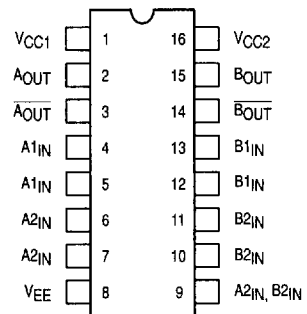
FN SUFFIX
PLCC
CASE 775-02

LOGIC DIAGRAM



$V_{CC1} = \text{PIN 1}$
 $V_{CC2} = \text{PIN 16}$
 $V_{EE} = \text{PIN 8}$

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 6-11.

