FUJITSU SEMICONDUCTOR
DATA SHEET

DS704-00008-0v01-E

16-bit Proprietary Microcontroller

CMOS

F²MC-16FX MB96620 Series

MB96F622/F623/F625*

■ DESCRIPTION

MB96620 series is based on Fujitsu's advanced 16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established 16LX series - thus allowing for easy migration of 16LX Software to the new 16FX products.
16FX improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For high processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 32MHz operation frequency from an external 4MHz resonator. The result is a minimum instruction cycle time of 31.2ns going together with excellent EMI behavior. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows selecting suitable operation frequencies for peripheral resources independent of the CPU speed.

*: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

Note: F²MC is the abbreviation of Fujitsu Flexible Microcontroller

For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

2011.3

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■ FEATURES

● Technology

- 0.18µm CMOS

● CPU

- F^2MC-16FX CPU
- Optimized instruction set for controller applications
  (bit, byte, word and long-word data types, 23 different addressing modes, barrel shift, variety of pointers)
- 8-byte instruction execution queue
- Signed multiply (16-bit ×16-bit) and divide (32-bit/16-bit) instructions available

● System clock

- On-chip PLL clock multiplier (×1 to ×8, ×1 when PLL stop)
- 4 MHz to 8 MHz external crystal oscillator clock
  (maximum frequency when using ceramic resonator depends on Q-factor)
- Up to 16 MHz external clock for devices with fast clock input feature
- 32.768 kHz subsystem quartz clock
- 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog
- Clock source selectable from main- and subclock oscillator and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals
- The subclock oscillator is enabled by the Boot ROM program controlled by a configuration marker after a Power or External reset
- Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode)

● On-chip voltage regulator

- Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures

● Low voltage reset

- Reset is generated when supply voltage is below minimum

● Code Security

- Protects Flash Memory content from unintended read-out

● DMA

- Automatic transfer function independent of CPU, can be assigned freely to resources

● Interrupts

- Fast Interrupt processing
- 8 programmable priority levels
- Non-Maskable Interrupt (NMI)

● CAN

- Supports CAN protocol version 2.0 part A and B
- ISO16845 certified
- Bit rates up to 1 Mbit/s
- 32 message objects
- Each message object has its own identifier mask
- Programmable FIFO mode (concatenation of message objects)
- Maskable interrupt
- Disabled Automatic Retransmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation

● USART

- Full duplex USARTs (SCI/LIN)
- Wide range of baud rate settings using a dedicated reload timer
- Special synchronous options for adapting to different synchronous serial protocols
- LIN functionality working either as master or slave LIN device
- Extended support for LIN-Protocol to reduce interrupt load

● I^2C

- Up to 400 Kbps
- Master and Slave functionality, 7-bit and 10-bit addressing

● A/D converter

- SAR-type
- 8/10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
- Range Comparator Function

● Source Clock Timers

- Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)

● Hardware Watchdog Timer

- Hardware watchdog timer is active after reset
- Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval

● Reload Timers

- 16-bit wide
- Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
- Event count function

● Free Running Timers

- Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency

● Input Capture Units

- 16-bit wide
- Signals an interrupt upon external event
- Rising edge, falling edge or rising and falling edge sensitive

Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with 16-bit I/O Timer occurs
- A pair of compare registers can be used to generate an output signal

Programmable Pulse Generator

- 16-bit down counter, cycle and duty setting registers
- Can be used as 2 × 8-bit PPG
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock and Reload timer underflow as clock input
- Can be triggered by software or reload timer
- Can trigger ADC conversion
- Timing point capture

Quadrature Position/Revolution Counter (QPRC)

- Edge count mode, Phase count mode, Level count mode
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers with interrupt
- Detection edge of the three external event input pins AIN, BIN and ZIN is configurable

Real Time Clock

- Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
- Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
- Read/write accessible second/minute/hour registers
- Can signal interrupts every half second/second/minute/hour/day
- Internal clock divider and prescaler provide exact 1s clock

External Interrupts

- Edge or Level sensitive
- Interrupt mask and pending bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

Non Maskable Interrupt

- Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
- Once enabled, can not be disabled other than by reset
- High or Low level sensitive
- Pin shared with external interrupt 0

I/O Ports

- Most of the external pins can be used as general purpose I/O
- All push-pull outputs (except when used as I^2C SDA/SCL line)
- Bit-wise programmable as input/output or peripheral signal
- Bit-wise programmable input enable
- One input level per GP-IO-pin (either Automotive or CMOS-Schmitt trigger)
- Bit-wise programmable pull-up resistor

● Built-in OCD (On Chip Debugger)

- One-wire debug tool interface
- Break function:
  - Hardware break: 6 points (shared with code event)
  - Software break: 4096 points
- Event function:
  - Code event: 6 points (shared with hardware break)
  - Data event: 6 points
  - Event sequencer: 2 levels
- Execution time measurement function
- Trace function: 42 branches
- Security function

● Flash Memory

- Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
- Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
- Supports automatic programming, Embedded Algorithm
- Write/Erase/Erase-Suspend/Resume commands
- A flag indicating completion of the algorithm
- Erase can be performed on each sector individually
- Sector protection
- Flash Security feature to protect the content of the Flash
- Low voltage detection during Flash erase

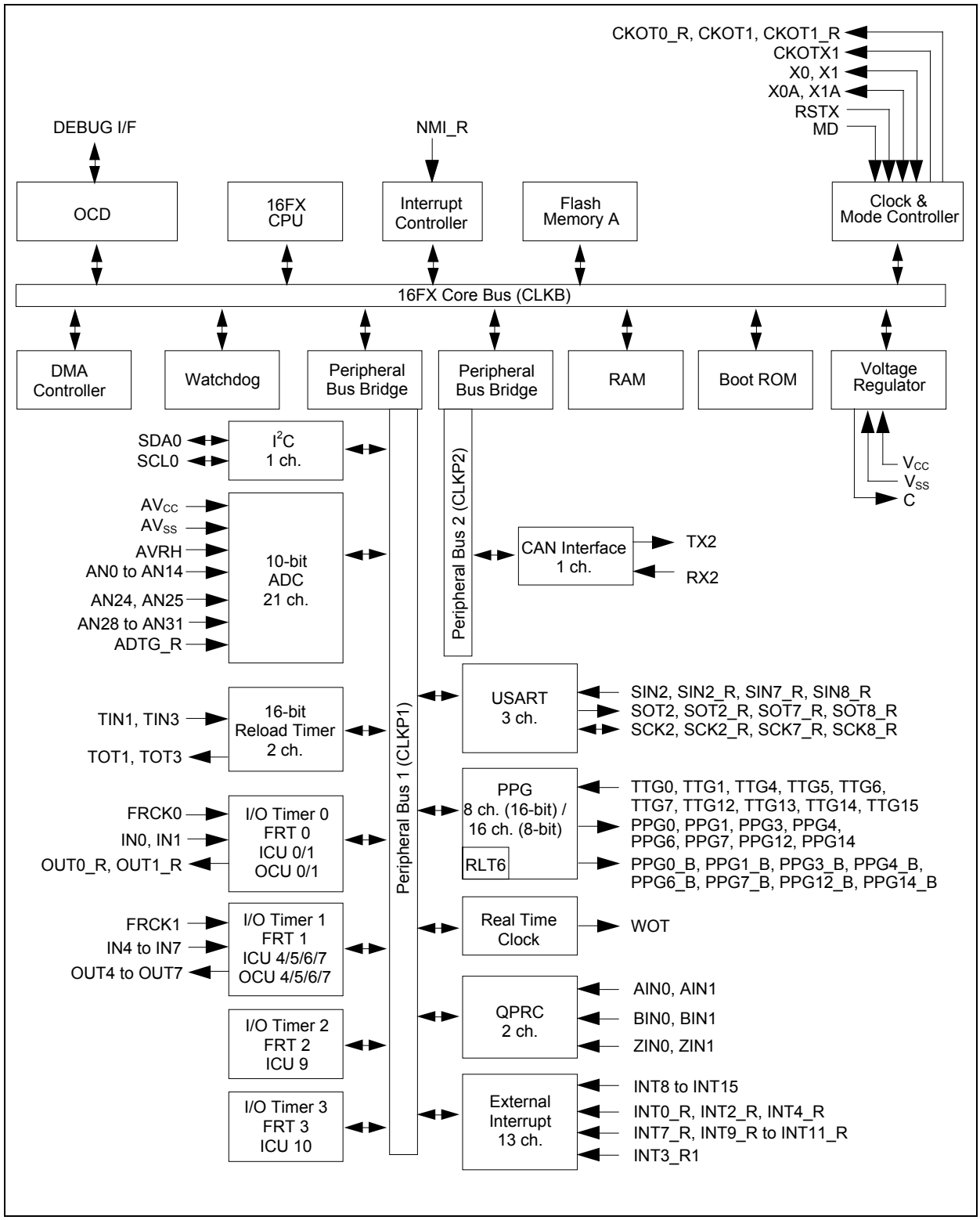
■ PRODUCT LINEUP

Features		MB96F620	Remark
Product type		Flash product: MB96F62x	
Subclock		Subclock can be set by software	
Dual Operation Flash	RAM		
32.5KB + 32KB	4KB	MB96F622	
64.5KB + 32KB	10KB	MB96F623	
128.5KB + 32KB	10KB	MB96F625	
Package		LQFP-64 FPT-64P-M23/M24	
DMA		2ch	
USART		3ch	LIN-USART 2/7/8
	with automatic LIN_Header transmission/reception	Yes (only 1ch)	LIN-USART 2
	with 16 byte RX- and TX-FIFO	No	
I^2C		1ch	I^2C0
10-bit A/D Converter		21ch	AN 0 to 14/24/25/28 to 31
	with Data Buffer	No	
	with Range Comparator	Yes	
	with Scan Disable	No	
	with ADC Pulse Detection	No	
16-bit Reload Timer (RLT)		3ch	RLT 1/3/6 Only RLT6 can be used as PPG clock source
16-bit Free-Running Timer (FRT)		4ch	FRT 0 to 3 FRT 0/1 with external clock input pin
16-bit Input Capture (ICU)		8ch (2 channels for LIN-USART)	ICU 0/1/4/5/6/7/9/10 (ICU 9/10 for LIN-USART)
16-bit Output Compare (OCU)		6ch	OCU 0/1/4/5/6/7
8/16-bit Programmable Pulse Generator (PPG)		8ch (16-bit) / 16ch (8-bit)	PPG 0/1/3/4/6/7/12/14
	with Timing point capture	Yes	
	with Start delay	No	
	with Ramp	No	
Quadrature position/revolution counter (QPRC)		2ch	QPRC 0/1
CAN Interface		1ch	CAN 2 32 Message Buffers
External Interrupts (INTerrupt)		13ch	INT 0/2/3/4/7 to 15
Non-Maskable Interrupt (NMI)		1ch	
Real Time Clock (RTC)		1ch	
I/O Ports		50(Dual clock mode) 52(Single clock mode)	
Clock Caribration Unit (CAL)		1ch	
Clock Output Function		2ch	
Low Voltage Reset		Yes	Low voltage reset can be disabled by software
Hardware Watchdog Timer		Yes	
On-chip RC-oscillator		Yes	
On-chip Debugger		Yes	

Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the General I/O port according to your function use.

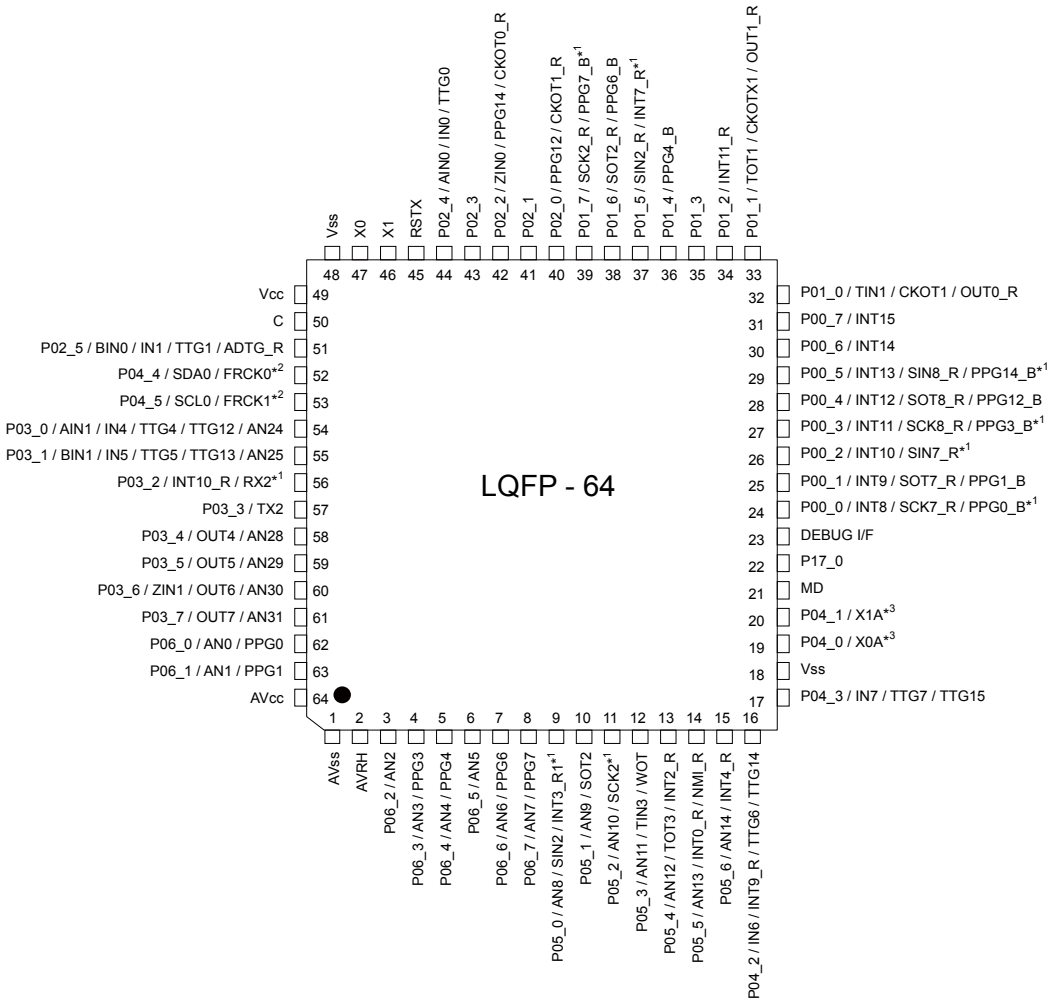
These devices are under development and specification is preliminary.
These products under development may change its specification without notice.

■ BLOCK DIAGRAM



■ PIN ASSIGNMENTS

(TOP VIEW)



(FPT-64P-M23, FPT-64P-M24)

*1: CMOS input level only
*2: CMOS input level only for I^2C
*3: Please set Rom Configuration Block (RCB) to use the subclock.
All other general-purpose pins have only Automotive input level.

■ PIN FUNCTION DESCRIPTION

Pin name	Feature	Description
ADTG_R	ADC	Relocated A/D converter trigger input
AINn	QPRC	Quadrature Position/Revolution Counter Unit n input
ANn	ADC	A/D converter channel n input
AVcc	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AVss	Supply	Analog circuits power supply
BINn	QPRC	Quadrature Position/Revolution Counter Unit n input
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTn_R	Clock output function	Relocated Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
FRCKn	Free Running Timer	Free Running Timer n input
INn	ICU	Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
INTn_R1	External Interrupt	Relocated External Interrupt n input
MD	Core	Input pins for specifying the operating mode
NMI_R	External Interrupt	Relocated Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n output
OUTn_R	OCU	Relocated Output Compare Unit n output
Pnn_m	GPIO	General purpose I/O
PPGn	PPG	Programmable Pulse Generator n output (16bit/8bit)
PPGn_B	PPG	Programmable Pulse Generator n output (8bit)
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SCLn	I^2C	I^2C interface n clock I/O input/output
SDAn	I^2C	I^2C interface n serial data I/O input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
Vcc	Supply	Power supply
Vss	Supply	Power supply
WOT	RTC	Real Time clock output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output
ZINn	QPRC	Quadrature Position/Revolution Counter Unit n input
DEBUG I/F	OCD	On Chip Debugger input/output

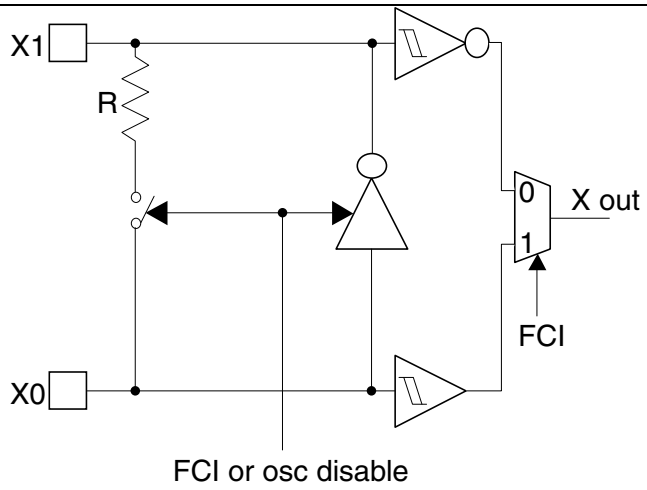
■ PIN CIRCUIT TYPE

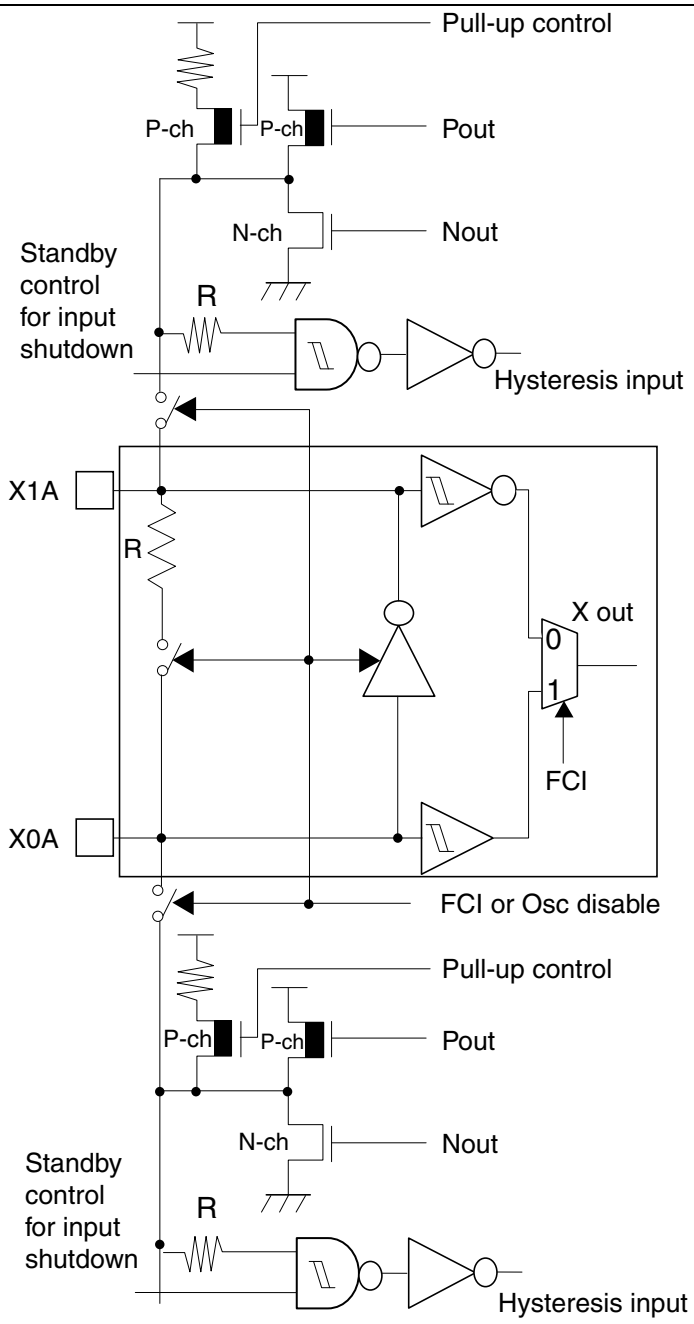
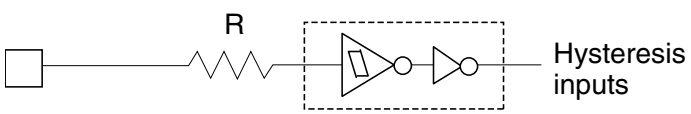
Pin no.	Circuit type*	Pin name
1	Supply	AV_{ss}
2	G	AVRH
3	K	P06_2 / AN2
4	K	P06_3 / AN3 / PPG3
5	K	P06_4 / AN4 / PPG4
6	K	P06_5 / AN5
7	K	P06_6 / AN6 / PPG6
8	K	P06_7 / AN7 / PPG7
9	I	P05_0 / AN8 / SIN2 / INT3_R1
10	K	P05_1 / AN9 / SOT2
11	I	P05_2 / AN10 / SCK2
12	K	P05_3 / AN11 / TIN3 / WOT
13	K	P05_4 / AN12 / TOT3 / INT2_R
14	K	P05_5 / AN13 / INT0_R / NMI_R
15	K	P05_6 / AN14 / INT4_R
16	H	P04_2 / IN6 / INT9_R / TTG6 / TTG14
17	H	P04_3 / IN7 / TTG7 / TTG15
18	Supply	V_{ss}
19	B	P04_0 / X0A
20	B	P04_1 / X1A
21	C	MD
22	H	P17_0
23	O	DEBUG I/F
24	M	P00_0 / INT8 / SCK7_R / PPG0_B
25	H	P00_1 / INT9 / SOT7_R / PPG1_B
26	M	P00_2 / INT10 / SIN7_R
27	M	P00_3 / INT11 / SCK8_R / PPG3_B
28	H	P00_4 / INT12 / SOT8_R / PPG12_B
29	M	P00_5 / INT13 / SIN8_R / PPG14_B
30	H	P00_6 / INT14
31	H	P00_7 / INT15
32	H	P01_0 / TIN1 / CKOT1 / OUT0_R

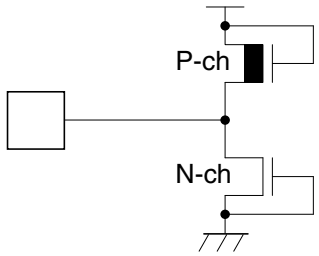
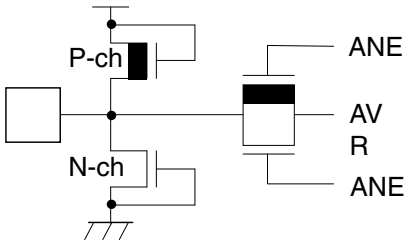
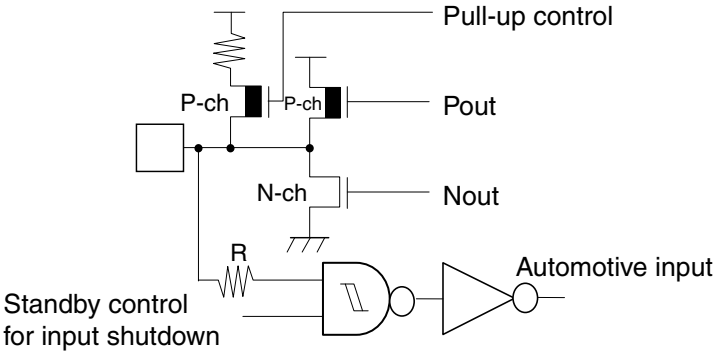
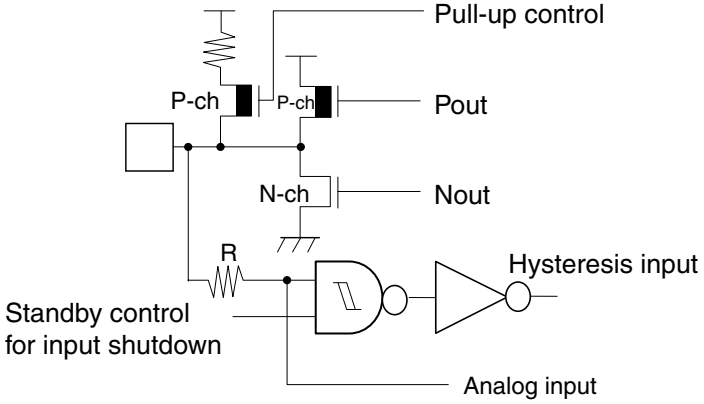
Pin no.	Circuit type*	Function
33	H	P01_1 / TOT1 / CKOTX1 / OUT1_R
34	H	P01_2 / INT11_R
35	H	P01_3
36	H	P01_4 / PPG4_B
37	M	P01_5 / SIN2_R / INT7_R
38	H	P01_6 / SOT2_R / PPG6_B
39	M	P01_7 / SCK2_R / PPG7_B
40	H	P02_0 / PPG12 / CKOT1_R
41	H	P02_1
42	H	P02_2 / ZIN0 / PPG14 / CKOT0_R
43	H	P02_3
44	H	P02_4 / AIN0 / IN0 / TTG0
45	C	RSTX
46	A	X1
47	A	X0
48	Supply	Vss
49	Supply	Vcc
50	F	C
51	H	P02_5 / BIN0 / IN1 / TTG1 / ADTG_R
52	N	P04_4 / SDA0 / FRCK0
53	N	P04_5 / SCL0 / FRCK1
54	K	P03_0 / AIN1 / IN4 / TTG4 / TTG12 / AN24
55	K	P03_1 / BIN1 / IN5 / TTG5 / TTG13 / AN25
56	M	P03_2 / INT10_R / RX2
57	H	P03_3 / TX2
58	K	P03_4 / OUT4 / AN28
59	K	P03_5 / OUT5 / AN29
60	K	P03_6 / ZIN1 / OUT6 / AN30
61	K	P03_7 / OUT7 / AN31
62	K	P06_0 / AN0 / PPG0
63	K	P06_1 / AN1 / PPG1
64	Supply	AVcc

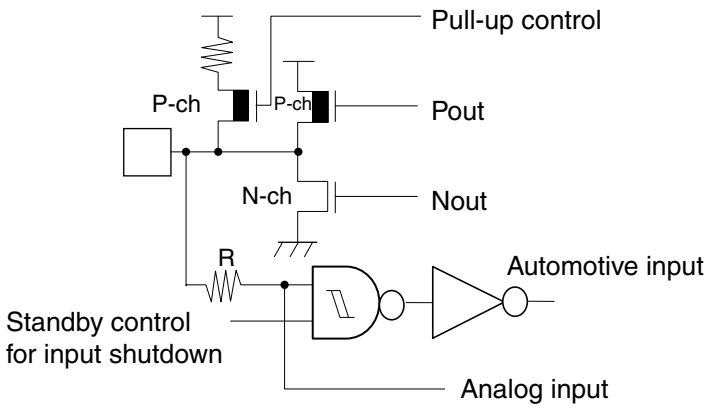
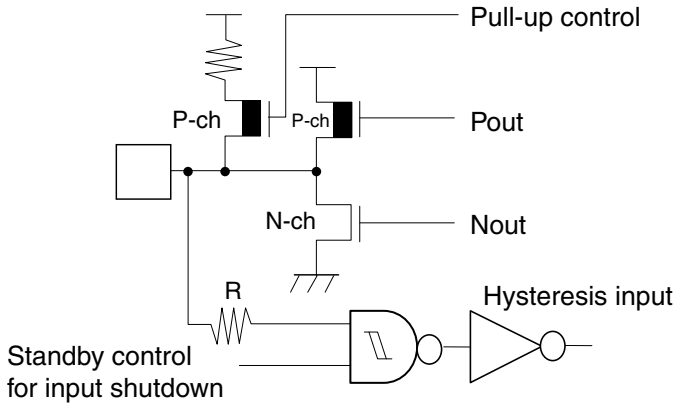
*: Please refer to "■ I/O CIRCUIT TYPE" for details on the I/O circuit types.

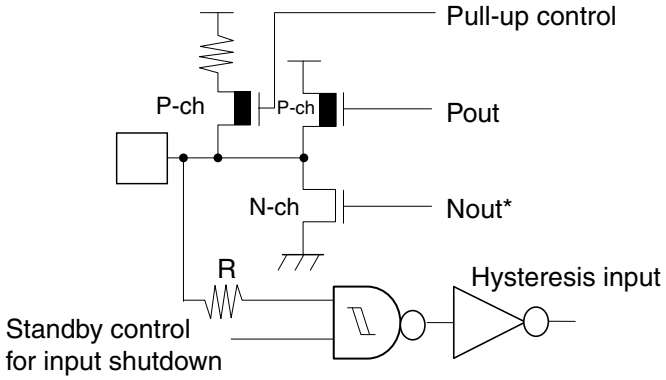
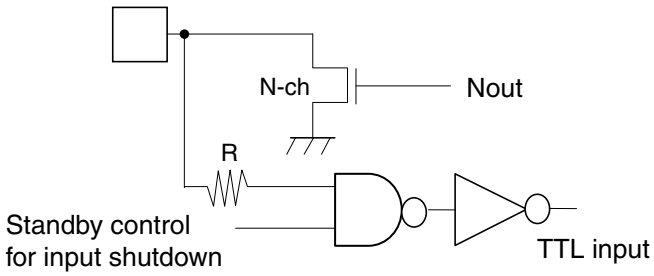
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		High-speed oscillation circuit: · Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) · Feedback resistor = approx. 1.0 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode · The amplitude: 1.8V±0.15V to operate by the internal supply voltage

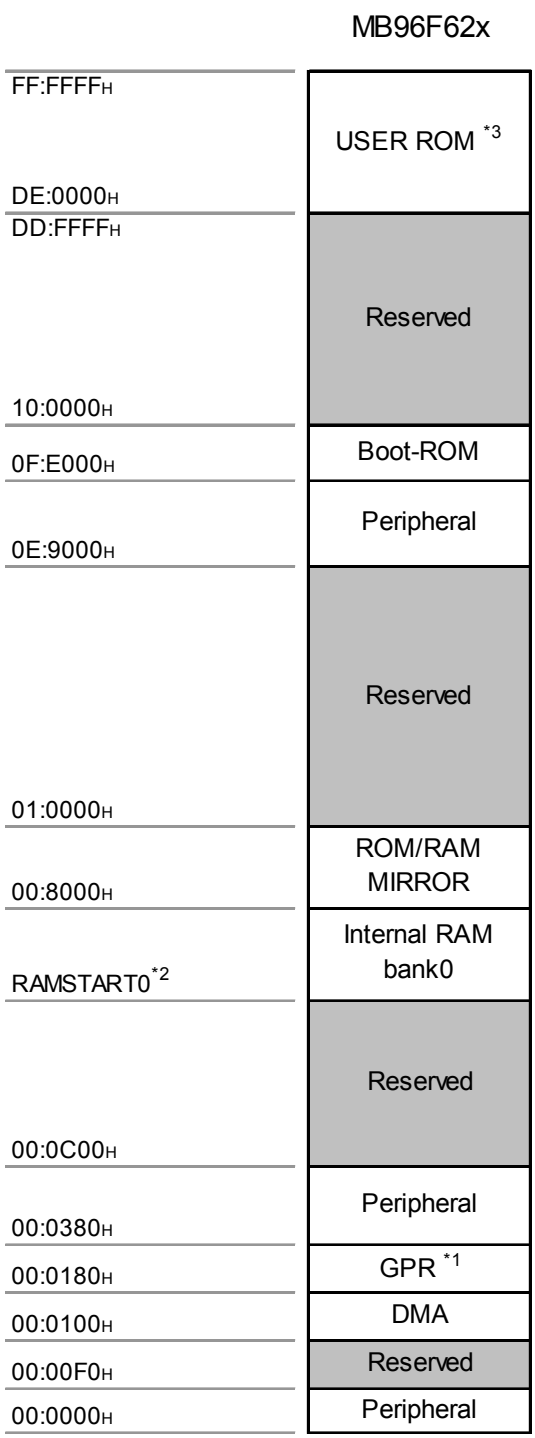
Type	Circuit	Remarks
B		Low-speed oscillation circuit shared with GPIO functionality: · Feedback resistor = approx. 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled · GPIO functionality selectable (CMOS hysteresis input with input shutdown function, I_{OL} = 4mA, I_{OH} = -4mA, Programmable pull-up resistor)
C		· CMOS hysteresis input pin

Type	Circuit	Remarks
F		· Power supply input protection circuit
G		· A/D converter ref+ (AVRH) power supply input pin with protection circuit · Without protection circuit against VCC for pins AVRH
H		· CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) · Automotive input with input shutdown function · Programmable pull-up resistor
I		· CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) · CMOS hysteresis input with input shutdown function · Programmable pull-up resistor · Analog input

Type	Circuit	Remarks
K		· CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) · Automotive input with input shutdown function · Programmable pull-up resistor · Analog input
M		· CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) · CMOS hysteresis input with input shutdown function · Programmable pull-up resistor

Type	Circuit	Remarks
N		· CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) · CMOS hysteresis input with input shutdown function · Programmable pull-up resistor * : N-channel transistor has slew rate control according to I^2C spec, irrespective of usage.
O		· I_{OL}: 25mA @ 2.7V · TTL input

■ MEMORY MAP



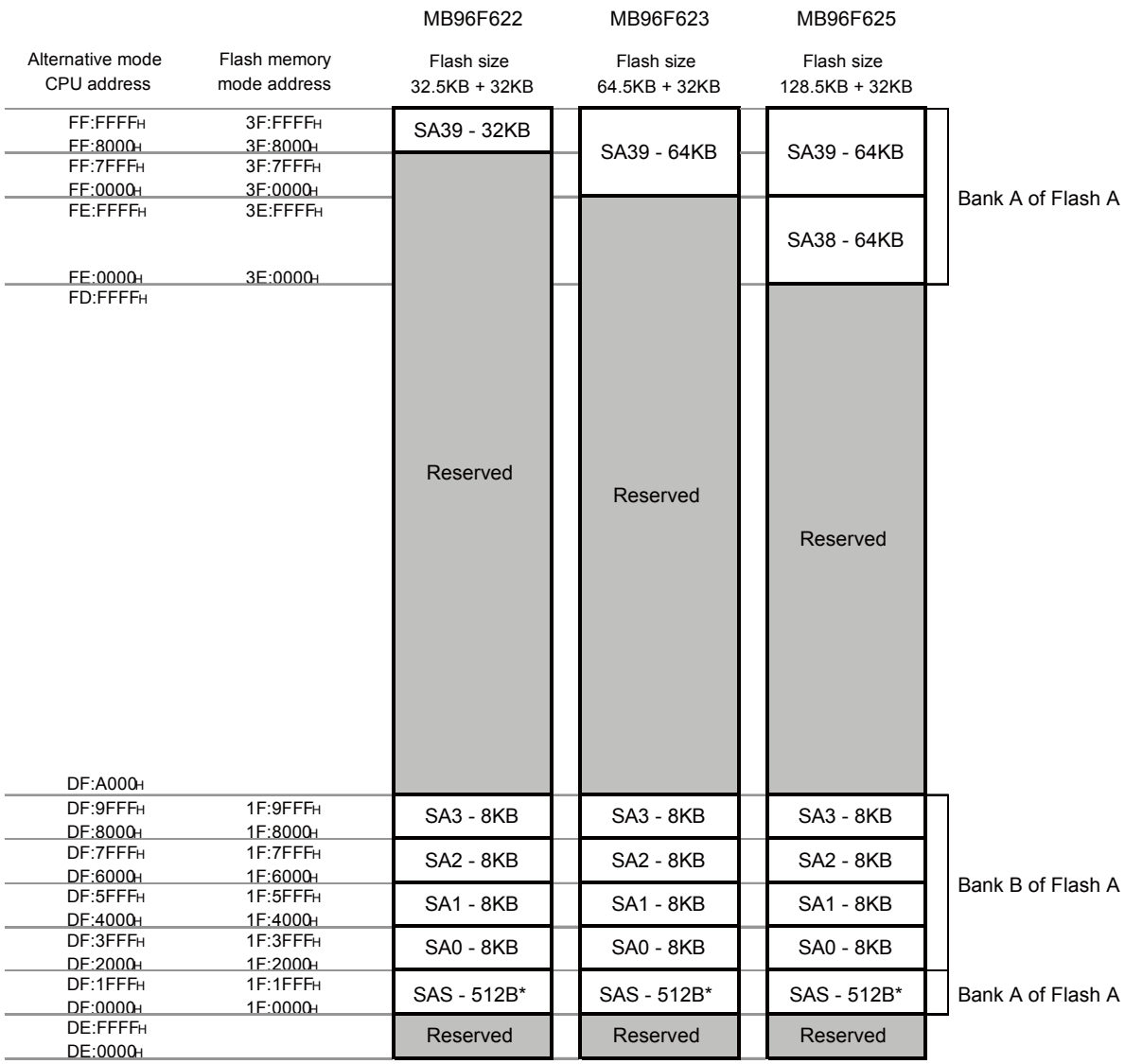
*1: Unused GPR banks can be used as RAM area
*2: For RAMSTART/END addresses, please refer to the table on the next page.
*3: For details about USER ROM area, see the "■USER ROM MEMORY MAP FOR FLASH DEVICES" on the following pages.

The DMA area is only available if the device contains the corresponding resource.
The available RAM and ROM area depends on the device.

■ RAMSTART ADDRESSES

Devices	Bank 0 RAM size	RAMSTART0
MB96F622	4KByte	$00:7200_H$
MB96F623 MB96F625	10KByte	$00:5A00_H$

■ USER ROM MEMORY MAP FOR FLASH DEVICES



*: Phiysical address area of SAS-512B is from DF:0000_H to DF:$01FF_H$.
Others (from DF:0200_H to DF:$1FFF_H$) are all ROM Mirror area for SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000_H - DF:$01FF_H$.
SAS can not be used for E^2PROM emulation.

■ SERIAL PROGRAMMING COMMUNICATION INTERFACE

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

MB96F62x		
Pin Number	USART Number	Normal Function
9	USART2	SIN2
37		SIN2_R
10		SOT2
38		SOT2_R
11		SCK2
39		SCK2_R
26	USART7	SIN7_R
25		SOT7_R
24		SCK7_R
29	USART8	SIN8_R
28		SOT8_R
27		SCK8_R

■ INTERRUPT VECTOR TABLE

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	3FC	CALLV0	No	-	Reserved
1	3F8	CALLV1	No	-	Reserved
2	3F4	CALLV2	No	-	Reserved
3	3F0	CALLV3	No	-	Reserved
4	3EC	CALLV4	No	-	Reserved
5	3E8	CALLV5	No	-	Reserved
6	3E4	CALLV6	No	-	Reserved
7	3E0	CALLV7	No	-	Reserved
8	3DC	RESET	No	-	Reserved
9	3D8	INT9	No	-	Reserved
10	3D4	EXCEPTION	No	-	Reserved
11	3D0	NMI	No	-	Non-Maskable Interrupt
12	3CC	DLY	No	12	Delayed Interrupt
13	3C8	RC_TIMER	No	13	RC Timer
14	3C4	MC_TIMER	No	14	Main Clock Timer
15	3C0	SC_TIMER	No	15	Sub Clock Timer
16	3BC	LVDI	No	16	Low Voltage Detector
17	3B8	EXTINT0	Yes	17	External Interrupt 0
18	3B4	-	-	18	Reserved
19	3B0	EXTINT2	Yes	19	External Interrupt 2
20	3AC	EXTINT3	Yes	20	External Interrupt 3
21	3A8	EXTINT4	Yes	21	External Interrupt 4
22	3A4	-	-	22	Reserved
23	3A0	-	-	23	Reserved
24	39C	EXTINT7	Yes	24	External Interrupt 7
25	398	EXTINT8	Yes	25	External Interrupt 8
26	394	EXTINT9	Yes	26	External Interrupt 9
27	390	EXTINT10	Yes	27	External Interrupt 10
28	38C	EXTINT11	Yes	28	External Interrupt 11
29	388	EXTINT12	Yes	29	External Interrupt 12
30	384	EXTINT13	Yes	30	External Interrupt 13
31	380	EXTINT14	Yes	31	External Interrupt 14
32	37C	EXTINT15	Yes	32	External Interrupt 15
33	378	-	-	33	Reserved
34	374	-	-	34	Reserved
35	370	CAN2	No	35	CAN Controller 2
36	36C	-	-	36	Reserved
37	368	-	-	37	Reserved
38	364	PPG0	Yes	38	Programmable Pulse Generator 0
39	360	PPG1	Yes	39	Programmable Pulse Generator 1
40	35C	-	-	40	Reserved
41	358	PPG3	Yes	41	Programmable Pulse Generator 3
42	354	PPG4	Yes	42	Programmable Pulse Generator 4
43	350	-	-	43	Reserved
44	34C	PPG6	Yes	44	Programmable Pulse Generator 6
45	348	PPG7	Yes	45	Programmable Pulse Generator 7
46	344	-	-	46	Reserved
47	340	-	-	47	Reserved
48	33C	-	-	48	Reserved
49	338	-	-	49	Reserved

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
50	334	PPG12	Yes	50	Programmable Pulse Generator 12
51	330	-	-	51	Reserved
52	32C	PPG14	Yes	52	Programmable Pulse Generator 14
53	328	-	-	53	Reserved
54	324	-	-	54	Reserved
55	320	-	-	55	Reserved
56	31C	-	-	56	Reserved
57	318	-	-	57	Reserved
58	314	-	-	58	Reserved
59	310	RLT1	Yes	59	Reload Timer 1
60	30C	-	-	60	Reserved
61	308	RLT3	Yes	61	Reload Timer 3
62	304	-	-	62	Reserved
63	300	-	-	63	Reserved
64	2FC	PPGRLT	Yes	64	Reload Timer 6 can be used as PPG clock source
65	2F8	ICU0	Yes	65	Input Capture Unit 0
66	2F4	ICU1	Yes	66	Input Capture Unit 1
67	2F0	-	-	67	Reserved
68	2EC	-	-	68	Reserved
69	2E8	ICU4	Yes	69	Input Capture Unit 4
70	2E4	ICU5	Yes	70	Input Capture Unit 5
71	2E0	ICU6	Yes	71	Input Capture Unit 6
72	2DC	ICU7	Yes	72	Input Capture Unit 7
73	2D8	-	-	73	Reserved
74	2D4	ICU9	Yes	74	Input Capture Unit 9
75	2D0	ICU10	Yes	75	Input Capture Unit 10
76	2CC	-	-	76	Reserved
77	2C8	OCU0	Yes	77	Output Compare Unit 0
78	2C4	OCU1	Yes	78	Output Compare Unit 1
79	2C0	-	-	79	Reserved
80	2BC	-	-	80	Reserved
81	2B8	OCU4	Yes	81	Output Compare Unit 4
82	2B4	OCU5	Yes	82	Output Compare Unit 5
83	2B0	OCU6	Yes	83	Output Compare Unit 6
84	2AC	OCU7	Yes	84	Output Compare Unit 7
85	2A8	-	-	85	Reserved
86	2A4	-	-	86	Reserved
87	2A0	-	-	87	Reserved
88	29C	-	-	88	Reserved
89	298	FRT0	Yes	89	Free Running Timer 0
90	294	FRT1	Yes	90	Free Running Timer 1
91	290	FRT2	Yes	91	Free Running Timer 2
92	28C	FRT3	Yes	92	Free Running Timer 3
93	288	RTC0	No	93	Real Time Clock
94	284	CAL0	No	94	Clock Calibration Unit
95	280	-	-	95	Reserved
96	27C	IIC0	Yes	96	I^2C interface0
97	278	-	-	97	Reserved
98	274	ADC0	Yes	98	A/D Converter
99	270	-	-	99	Reserved
100	26C	-	-	100	Reserved
101	268	-	-	101	Reserved

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
102	264	-	-	102	Reserved
103	260	-	-	103	Reserved
104	25C	-	-	104	Reserved
105	258	LINR2	Yes	105	LIN USART 2 RX
106	254	LINT2	Yes	106	LIN USART 2 TX
107	250	-	-	107	Reserved
108	24C	-	-	108	Reserved
109	248	-	-	109	Reserved
110	244	-	-	110	Reserved
111	240	-	-	111	Reserved
112	23C	-	-	112	Reserved
113	238	-	-	113	Reserved
114	234	-	-	114	Reserved
115	230	LINR7	Yes	115	LIN USART 7 RX
116	22C	LINT7	Yes	116	LIN USART 7 TX
117	228	LINR8	Yes	117	LIN USART 8 RX
118	224	LINT8	Yes	118	LIN USART 8 TX
119	220	-	-	119	Reserved
120	21C	-	-	120	Reserved
121	218	-	-	121	Reserved
122	214	-	-	122	Reserved
123	210	-	-	123	Reserved
124	20C	-	-	124	Reserved
125	208	-	-	125	Reserved
126	204	-	-	126	Reserved
127	200	-	-	127	Reserved
128	1FC	-	-	128	Reserved
129	1F8	-	-	129	Reserved
130	1F4	-	-	130	Reserved
131	1F0	-	-	131	Reserved
132	1EC	-	-	132	Reserved
133	1E8	FLASHA	Yes	133	Flash memory A interrupt
134	1E4	-	-	134	Reserved
135	1E0	-	-	135	Reserved
136	1DC	-	-	136	Reserved
137	1D8	QPRC0	Yes	137	Quad Possition/Revolution counter 0
138	1D4	QPRC1	Yes	138	Quad Possition/Revolution counter 1
139	1D0	ADCRC0	No	139	A/D Converter 0 - Range Comparator
140	1CC	-	-	140	Reserved
141	1C8	-	-	141	Reserved
142	1C4	-	-	142	Reserved
143	1C0	-	-	143	Reserved

■ HANDLING DEVICES

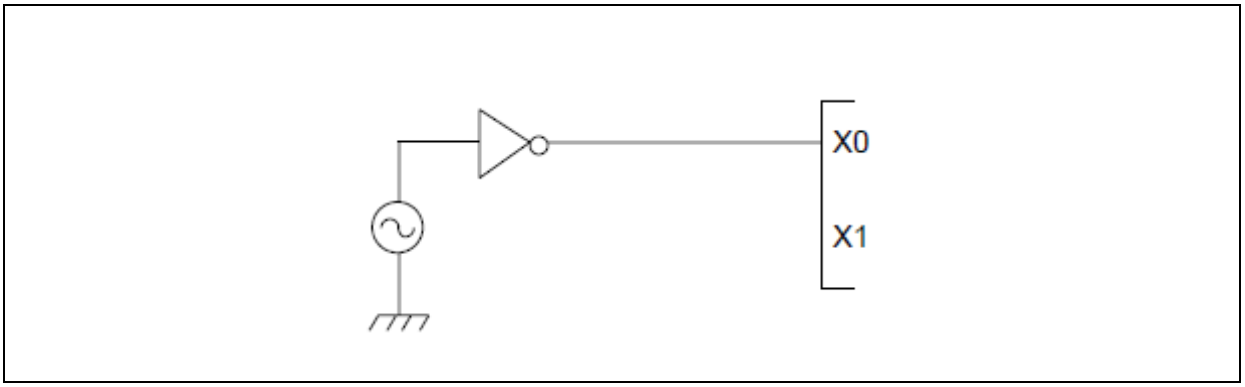
Special care is required for the following when handling the device:
• Latch-up prevention
• Unused pins handling
• External clock usage
• Notes on PLL clock mode operation
• Power supply pins (V_{CC}/V_{SS})
• Crystal oscillator circuit
• Turn on sequence of power supply to A/D converter and analog inputs
• Pin handling when not using the A/D converter
• Notes on Power-on
• Stabilization of power supply voltage
• Serial communication

1. Latch-up prevention
CMOS IC chips may suffer latch-up under the following conditions:
• A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
• A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.
• The AV_{CC} power supply is applied before the V_{CC} voltage.
Latch-up may increase the power supply current dramatically, causing thermal damages to the device.
For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

2. Unused pins handling
Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).
Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.
Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

3. External clock usage
The permitted frequency range of an external clock depends on the oscillator type and configuration.
See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

1. Single phase external clock for Main oscillator
• When using a single phase external clock for the Main oscillator, X0 pin must be driven and X1 pin left open. And supply 1.8V power to the external clock.



2. Single phase external clock for Sub oscillator

- When using a single phase external clock for the Sub oscillator, 'External clock mode' must be selected and X0A/GP04_0 must be driven. X1A/GP04_1 must be configured as GPIO.

4. Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

5. Power supply pins (V_{CC}/V_{SS})

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.
V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.
As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 µF between Vcc and Vss as close as possible to Vcc and Vss pins.

6. Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.
It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.
It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

7. Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.
It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

8. Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

9. Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2V to 2.7V.

10. Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50Hz to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

11. Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

■ ELECTRICAL CHARACTERISTICS

This section describes the electrical characteristics of MB96620 series.

1. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage*1	Vcc	-	Vss - 0.3	Vss + 6.0	V	
Analog power supply voltage*1	AVcc	-	Vss - 0.3	Vss + 6.0	V	Vcc = AVcc*2
Analog reference voltage*1	AVRH	-	Vss - 0.3	Vss + 6.0	V	AVCC ≥ AVRH AVRH ≥ AVSS
Input voltage*1	V_I	-	Vss - 0.3	Vcc + 0.3	V	VI ≤ VCC + 0.3V*3
Output voltage*1	V_O	-	Vss - 0.3	Vcc + 0.3	V	VO ≤ VCC + 0.3V*3
Maximum clamp current	I_{CLAMP}	-	-4.0	+4.0	mA	Applicable to general purpose I/O pins*4
Total maximum clamp current	$\sum\|I_{CLAMP}\|$	-	-	17	mA	Applicable to general purpose I/O pins*4
"L" level maximum output current	I_{OL}	-	-	15	mA	
"L" level average output current	I_{OLAV}	-	-	4	mA	
"L" level maximum overall output current	$\sum I_{OL}$	-	-	TBD	mA	
"L" level average overall output current	$\sum I_{OLAV}$	-	-	21	mA	
"H" level maximum output current	I_{OH}	-	-	-15	mA	
"H" level average output current	I_{OHAV}	-	-	- 4	mA	
"H" level maximum overall output current	$\sum I_{OH}$	-	-	TBD	mA	
"H" level average overall output current	$\sum I_{OHAV}$	-	-	-21	mA	
Power consumption*5	P_D	T_A=+85°C	-	TBD*6	mW	
		T_A=+105°C	-	TBD*6	mW	
		T_A=+85°C	-	TBD*6	mW	No Flash program erase*7
Operating ambient temperature	T_A	-	-40	+105	°C	
Storage temperature	T_{STG}	-	- 55	+ 150	°C	

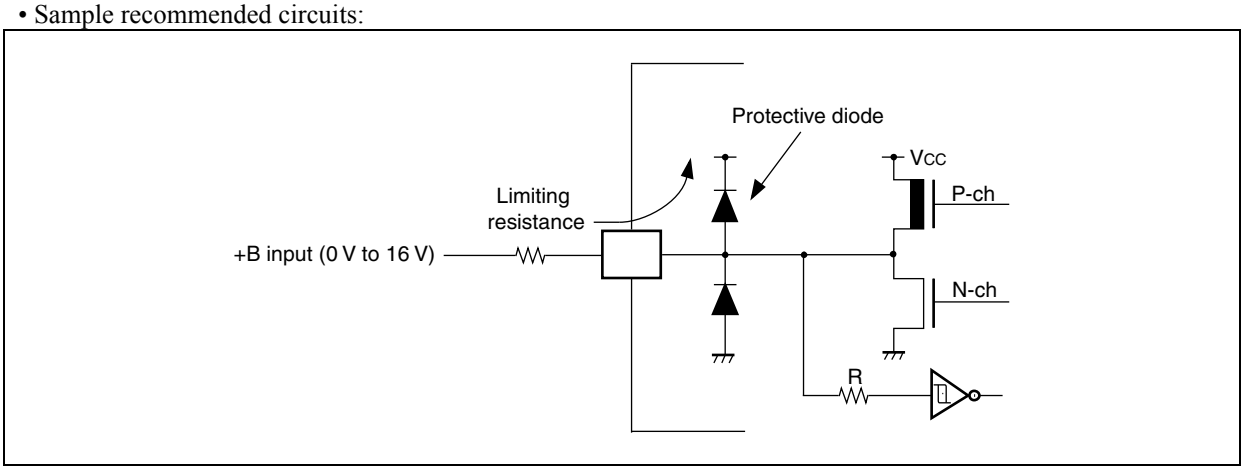
*1: Base on Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 105°C.

*2: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC}.

*4: • Applicable to all general purpose I/O pins (Pnn_m)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

• Sample recommended circuits:



*5: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} \times I_{OL} + V_{OH} \times I_{OH})$ (I/O load power dissipation, sum is performed on all I/O ports)
$P_{INT} = V_{CC} \times (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.
I_A is the analog current consumption into AV_{CC}.
*6: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.
*7: Please contact FUJITSU SEMICONDUCTOR for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(Vss = AVss = 0.0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	Vcc	2.7	-	5.5	V	
Smoothing capacitor at C pin	Cs	0.5	1.0	1.5	µF	1.0µF (Allowance within ± 50%) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at Vcc must use the one of a capacity value that is larger than Cs.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges.
Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

The following tables show the DC characteristics.

1. Current rating of MB96F622/F623/F625 (Provisional value)

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes*1	I_{CCPLL}	Vcc	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz (CLKRC and CLKSC stopped)	-	30	-	mA	T_A =+ 25°C
				-	-	40	mA	T_A = +105°C
	I_{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	-	5	-	mA	T_A = +25°C
				-	-	10	mA	T_A = +105°C
	I_{CCSUB}		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	-	0.5	-	mA	T_A = +25°C
				-	-	5	mA	T_A = +105°C
Power supply current in Sleep modes*1	I_{CCSPLL}	Vcc	PLL Sleep mode with CLKS1/2 = CLKP1/2 = 32MHz (CLKRC and CLKSC stopped)	-	10	-	mA	T_A =+ 25°C
				-	-	15	mA	T_A = +105°C
	$I_{CCSMAIN}$		Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz (CLKPLL, CLKRC and CLKSC stopped)	-	3	-	mA	T_A =+ 25°C
				-	-	8	mA	T_A = +105°C
	I_{CCSSUB}		Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz, (CLKMC, CLKPLL and CLKRC stopped)	-	0.3	-	mA	T_A =+ 25°C
				-	-	4.5	mA	T_A = +105°C
Power supply current in Timer modes*2	$I_{CCTMAIN}$	Vcc	Main Timer mode with CLKMC = 4MHz CL=10pF (CLKPLL, CLKRC and CLKSC stopped)	-	360	430	µA	T_A =+ 25°C
				-	-	1250	µA	T_A = +105°C
	I_{CCTRCH}		RC Timer mode with (CLKRC = 2MHz)	-	150	190	µA	T_A = +25°C
				-	-	1025	µA	T_A = +105°C
	I_{CCTRCL}		RC Timer mode with (CLKRC = 100kHz)	-	45	75	µA	T_A =+ 25°C
				-	-	855	µA	T_A = +105°C
	I_{CCTSUB}		Sub Timer mode with CLKSC = 32kHz CL=10pF (CLKMC, CLKPLL and CLKRC stopped)	-	40	75	µA	T_A = +25°C
				-	-	840	µA	T_A = +105°C

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Stop mode *3	I_{CCH}	Vcc	-	-	30	55	µA	T_A = +25°C
				-	-	830	µA	T_A = +105°C
Power supply current for active Low Voltage detector	I_{CCLVD}		Low voltage detector enabled	-	5	10	µA	This current must be added to all Power supply currents above
Flash Write/ Erase current	$I_{CCFLASH}$		Current for Flash module	-	15	25	mA	Must be added to all current above

*1: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control.

*2: The power supply current in Timer mode is the value when Flash is in Flash Deep sleep mode.
Main Timer mode is the value in crystal oscillator of 4MHz (C_L=10pF).
Sub Timer mode is the value in crystal oscillator of 32kHz (C_L=10pF).

*3: The power supply current in Stop mode is the value when Flash is in Flash Deep Sleep mode.

2. Pin Characteristics

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	Port inputs Pnn_m	-	Vcc × 0.7	-	Vcc + 0.3	V	CMOS Hysteresis Input
			-	Vcc × 0.8	-	Vcc + 0.3	V	AUTOMOTIVE Hysteresis Input
	V_{IHX0S}	X0	External clock in "oscillation mode"	VD × 0.8	-	VD	V	VD=1.8V±0.15V
	V_{IHX0AS}	X0A	External clock in "oscillation mode"	Vcc × 0.8	-	Vcc + 0.3	V	
	V_{IHR}	RSTX	-	Vcc × 0.8	-	Vcc + 0.3	V	CMOS Hysteresis Input
	V_{IHM}	MD	-	Vcc - 0.3	-	Vcc + 0.3	V	CMOS Hysteresis Input
	V_{IHD}	DEBUG I/F	-	2.0	-	Vcc + 0.3	V	TTL Input
"L" level input voltage	V_{IL}	Port inputs Pnn_m	-	Vss - 0.3	-	Vcc × 0.3	V	CMOS Hysteresis Input
			-	Vss - 0.3	-	Vcc × 0.5	V	AUTOMOTIVE Hysteresis Input
	V_{ILX0S}	X0	External clock in "oscillation mode"	Vss	-	VD × 0.2	V	VD=1.8V±0.15V
	V_{ILX0AS}	X0A	External clock in "oscillation mode"	Vss - 0.3	-	Vcc × 0.2	V	
	V_{ILR}	RSTX	-	Vss - 0.3	-	Vcc × 0.2	V	CMOS Hysteresis Input
	V_{ILM}	MD	-	Vss - 0.3	-	Vss + 0.3	V	CMOS Hysteresis Input
	V_{ILD}	DEBUG I/F	-	Vss - 0.3	-	0.8	V	TTL Input
"H" level output voltage	V_{OH4}	4mA type	4.5V ≤ Vcc ≤ 5.5V I_{OH} = -4mA	Vcc - 0.5	-	Vcc	V	
			2.7V ≤ Vcc < 4.5V I_{OH} = TBD					
	V_{OH3}	3mA type	4.5V ≤ Vcc ≤ 5.5V I_{OH} = -3mA	Vcc - 0.5	-	Vcc	V	
			2.7V ≤ Vcc < 4.5V I_{OH} = TBD					
"L" level output voltage	V_{OL4}	4mA type	4.5V ≤ Vcc ≤ 5.5V I_{OH} = +4mA	-	-	0.4	V	
			2.7V ≤ Vcc < 4.5V I_{OH} = TBD					
	V_{OL3}	3mA type	4.5V ≤ Vcc < 5.5V I_{OH} = -3mA	-	-	0.4	V	
Input leak current	I_{IL}	Pnn_m	Vss < V_I < Vcc AVss < V_I < AVcc, AVRH	- 1	-	1	µA	
Pull-up resistance value	R_{PU}	Pnn_m	Vcc=5.0V ±10%	25	50	100	kΩ	

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input capacitance	C_{IN}	Other than Vcc, Vss, AVcc, AVss, AVRH	-	-	5	15	pF	

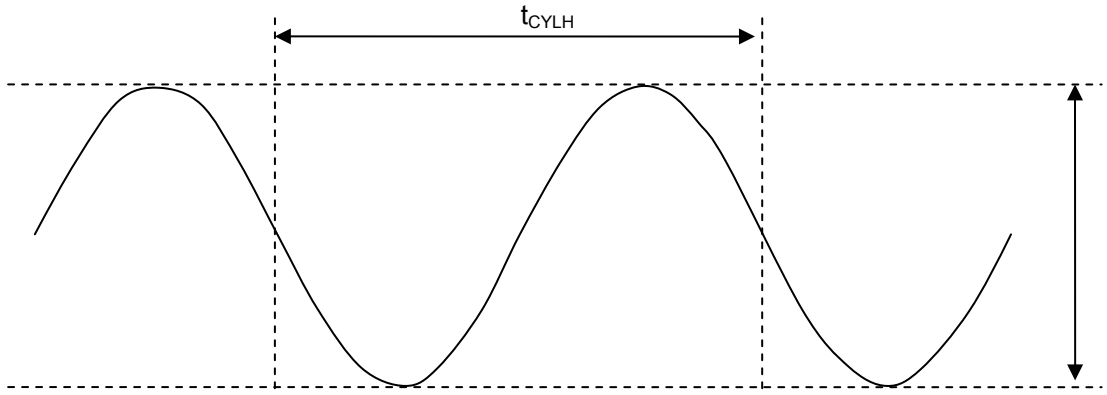
4. AC Characteristics

The following tables show the AC characteristics.

(1) Main Clock Input Characteristics

(AVcc = 2.7V to 5.5V, Vcc= 1.8V ± 0.15V, Vss = AVss = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_C	X0, X1	-	4	-	8	MHz	When using a crystal oscillator, PLL off
				-	-	8	MHz	When using an opposite phase external clock, PLL off
				4	-	8	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Input frequency	f_{FCI}	X0	-	-	-	16	MHz	When using a single phase external clock in “Fast Clock Input mode” , PLL off
				4	-	16	MHz	When using a single phase external clock in “Fast Clock Input mode” , PLL on
Input clock cycle	t_{CYLH}	-	-	62.5	-	-	ns	
Input clock pulse width	P_{WH}, P_{WL}	-	-	30	-	70	%	

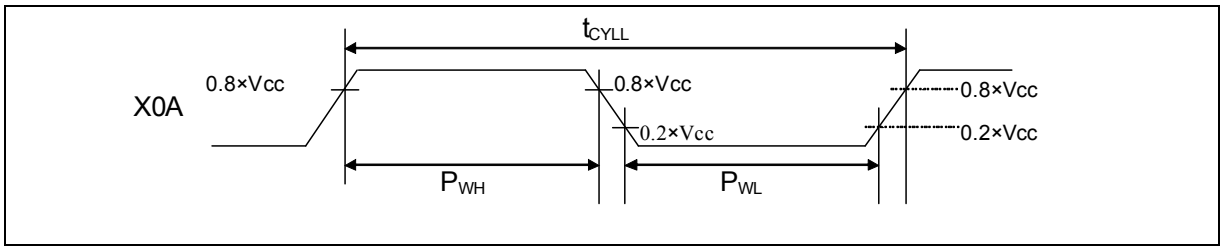


The amplitude changes by resistance, capacity which added outside or the difference of the device.

(2) Sub Clock Input Characteristics

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	F_{CL}	X0A, X1A	-	-	32.768	-	kHz	When using an oscillation circuit
			-	-	-	100	kHz	When using an opposite phase external clock
		X0A	-	-	-	50	kHz	When using a single phase external clock
Input clock cycle	t_{CYLL}	-	-	10	-	-	µs	
Input clock pulse width	-	-	P_{WH}/t_{CYLL} P_{WL}/t_{CYLL}	30	-	70	%	



(3) Built-in CR Oscillation Characteristics

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CR}	-	50	100	200	kHz	When using slow frequency of RC oscillator
		-	1	2	4	MHz	When using fast frequency of RC oscillator

(4) Internal Clock timing

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value		Unit
		Min	Max	
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	-	54	MHz
Internal CPU clock frequency (CLKB), Internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	-	32	MHz
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	-	32	MHz

(5) Operating Conditions of PLL

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)	t_{LOCK}	1	-	4	ms	Time from when the PLL starts operating until the oscillation stabilizes
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL macro oscillation clock frequency	f_{PLLO}	56	-	108	MHz	

(6) Reset Input Characteristics

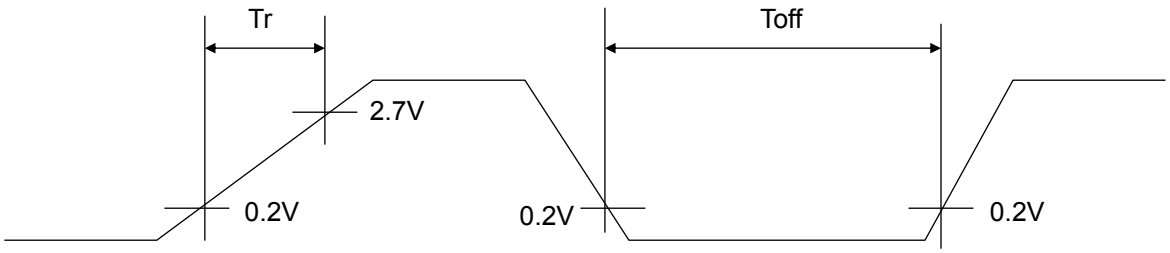
(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Reset input time	T_{RSTL}	RSTX	-	10	-	µs
Rejection of reset input time			-	1	-	µs

(7) Power-on Reset Timing

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power on rise time	Tr	0.05	-	30	ms
Power off time	Toff	1	-	-	ms



If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

(8) USART Timing (Provisional value)

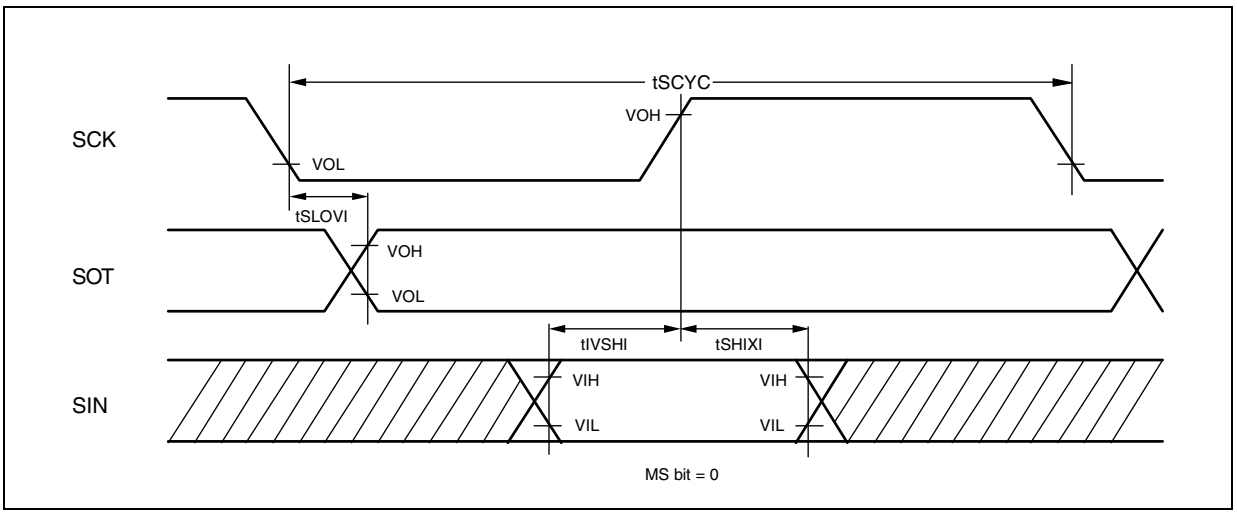
(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 105°C, C_L=50pF)

Parameter	Symbol	Pin name	Conditions	4.5V ≤ Vcc < 5.5V		2.7V ≤ Vcc < 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	tSCYC	SCKn	Internal shift clock operation	4 t_{CLKP1}	-	4 t_{CLKP1}	-	ns
SCK ↓ → SOT delay time	tSLOVI	SCKn SOTn		- 20	+ 20	- 30	+ 30	ns
SOT → SCK ↑ delay time	tOVSHI	SCKn SOTn		N× t_{CLKP1} – 20*	-	N× t_{CLKP1} – 30*	-	ns
SIN → SCK ↑ setup time	tIVSHI	SCKn SINn		t_{CLKP1} + 45	-	t_{CLKP1} + 55	-	ns
SCK ↑ → SIN hold time	tSHIXI	SCKn SINn		0	-	0	-	ns
Serial clock "L" pulse width	tSLSH	SCKn	External shift clock operation	t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
Serial clock "H" pulse width	tSHSL	SCKn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK ↓ → SOT delay time	tSLOVE	SCKn SOTn		-	2 t_{CLKP1} +45	-	2 t_{CLKP1} + 55	ns
SIN → SCK ↑ setup time	tIVSHE	SCKn SINn		t_{CLKP1}/2 + 10	-	t_{CLKP1}/2 + 10	-	ns
SCK ↑ → SIN hold time	tSHIXE	SCKn SINn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK fall time	tF	SCKn		-	20	-	20	ns
SCK rise time	tR	SCKn		-	20	-	20	ns

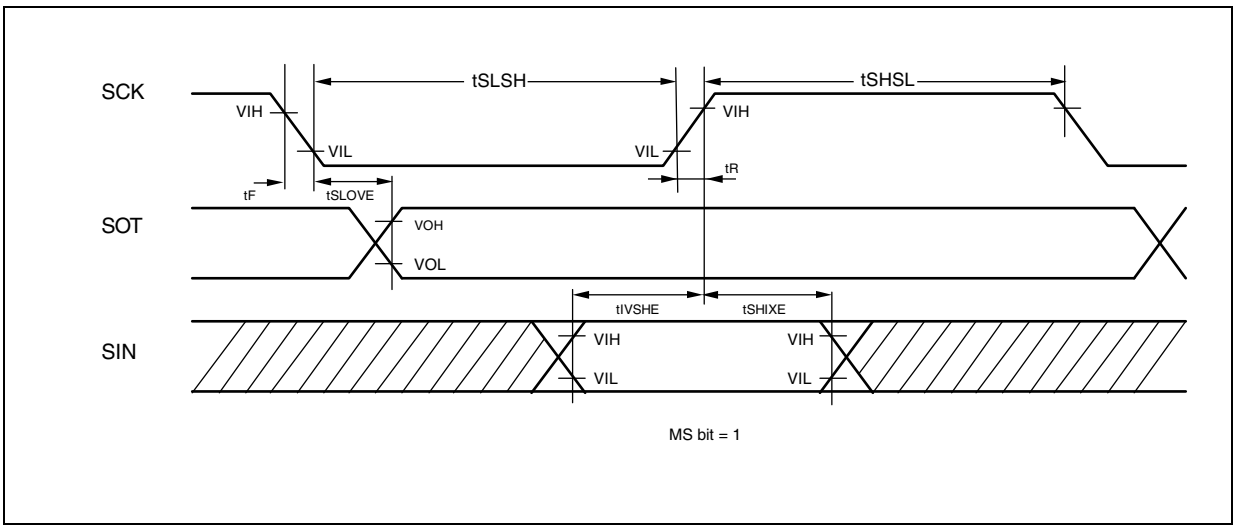
Notes:
- The above characteristics apply to CLK synchronous mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96620 series HARDWARE MANUAL”
- t_{CLKP1} indicates the peripheral clock 1 (CLKP1), Unit : ns
- These characteristics only guarantee the same relocate port number. For example, The combination of SCLKn_0 and SOTn_1 is not guaranteed.

*: Parameter N depends on t_{SCYCI} and can be calculated as follows:
• If t_{SCYCI} = 2× k× t_{CLKP1}, then N = k, where k is an integer > 2
• If t_{SCYCI} = (2× k+1) × t_{CLKP1}, then N = k+1, where k is an integer > 1
Examples:

tSCYC	N
4× t_{CLKP1}	2
5× t_{CLKP1}, 6× t_{CLKP1}	3
7× t_{CLKP1}, 8× t_{CLKP1}	4
...	...



MS bit = 0



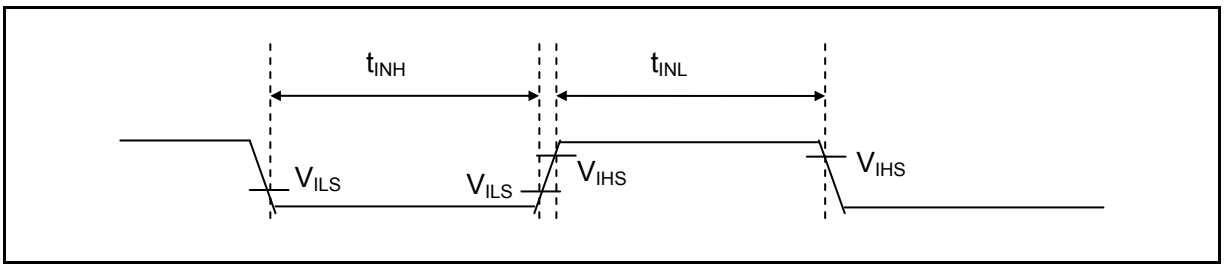
MS bit = 1

(9) External input timing

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 105°C, C_L=50pF)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH} t_{INL}	Pnn_m	-	$2t_{CLKP1}$ +200 (t_{CLKP1}= $1/f_{CLKP1}$)*	-	ns	General Purpose I/O
		ADTG_R					A/D converter trigger input
		TINn					Reload Timer
		TTGn					PPG Trigger input
		FRCKn					Free-Running Timer input clock
		INn					Input capture
		AINn BINn ZINn					Quadrature position/revolution counter
		INTn(_R, _R1), NMI_R		200	-	ns	External interrupt NMI

* : t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time except stop time at stop mode.



(10) I^2C timing

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to +105°C)

Parameter	Symbol	Conditions	Typical mode		High-speed mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	fSCL	CL = 50pF, R = (Vp/I_{OL}) *1	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	tHDSTA		4.0	-	0.6	-	µs
SCLclock "L" width	tLOW		4.7	-	1.3	-	µs
SCLclock "H" width	tHIGH		4.0	-	0.6	-	µs
(Repeated) START setup time SCL ↑ → SDA ↓	tSUSTA		4.7	-	0.6	-	µs
Data hold time SCL ↓ → SDA ↓ ↑	tHDDAT		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑ → SCL ↑	tSUDAT		250	-	100	-	ns
STOP condition setup time SCL ↑ → SDA ↑	tSUSTO		4.0	-	0.6	-	µs
Bus free time between "STOP condition" and "START condition"	tBUS		4.7	-	1.3	-	µs
Capacitive load for each bus line	Cb	-	-	400	-	400	pF

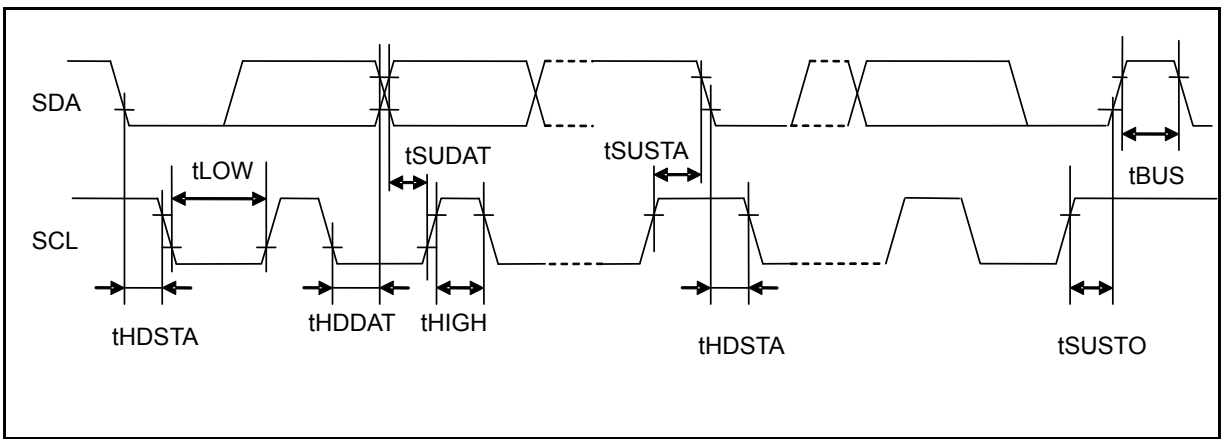
*1: R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum tHDDAT must satisfy that it doesn't extend at least "L" period (tLOW) of device's SCL signal.

*3: A high-speed mode I^2C bus device can be used on a standard mode I^2C bus system as long as the device satisfies the requirement of "tSUDAT ≥ 250 ns".

*4: t_{CLKP1} is the peripheral clock1 (CLKP1) cycle time. To use I^2C, set the peripheral bus clock at 8 MHz or more.

*5: Cb = Capacitance of each bus line in pF.



● 10bit A/D Converter

This chapter shows the electrical characteristics for the A/D converter.

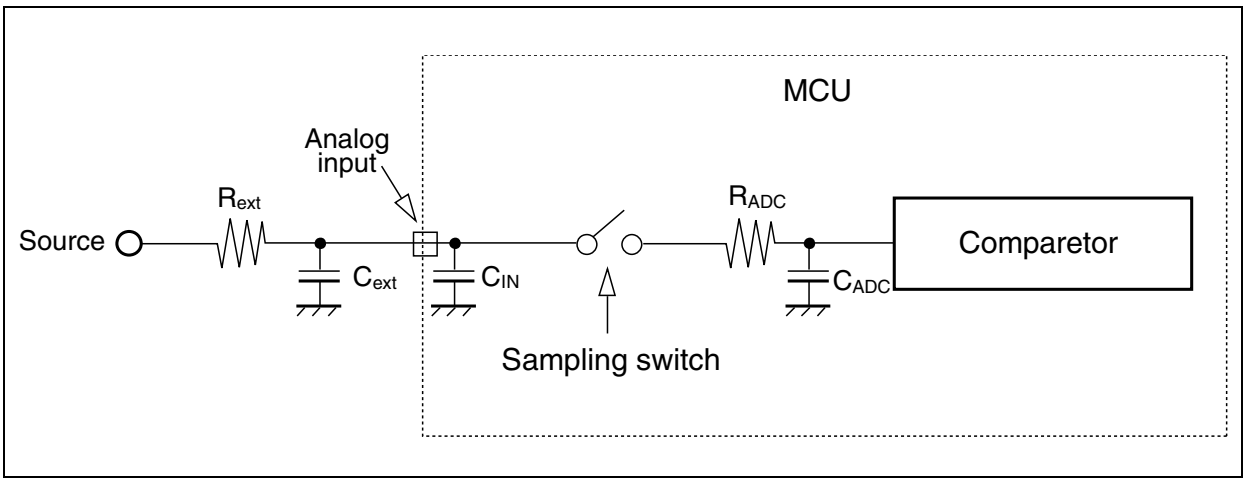
- Electrical characteristics for the A/D converter (Provisional value)

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	- 3.0	-	+ 3.0	LSB	
Nonlinearity error	-	-	- 2.5	-	+ 2.5	LSB	
Differential Nonlinearity error	-	-	- 1.9	-	+ 1.9	LSB	
Zero transition voltage	V_{OT}	ANx	Typ - 20	AVss + 0.5LSB	Typ + 20	mV	
Full transition voltage	V_{FST}	ANx	Typ - 20	AVRH - 1.5LSB	Typ + 20	mV	
Compare time	-	-	1.0	-	5.0	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.0	-	TBD	µs	2.7V ≤ AV_{CC} < 4.5V
Sampling time	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	2.7V ≤ AV_{CC} < 4.5V
Power supply current	I_A	AV_{CC}	-	2.0	3.1	mA	A/D Converter active
	I_{AH}		-	-	3.3	µA	A/D Converter not operated
Reference power supply current (between AVRH to AVSS)	I_R	AVRH	-	TBD	TBD	mA	A/D Converter active
	I_{RH}		-	-	TBD	µA	A/D Converter not operated
Analog input capacity	C_{VIN}	ANx	-	-	15.5	pF	
Analog port input current	I_{AIN}	ANx	- 0.3	-	+ 0.3	µA	AV_{SS} < V < AV_{CC}, AVRH
Analog input voltage	V_{AIN}	ANx	AV_{SS}	-	AVRH	V	
Reference voltage range	-	AVRH	AV_{CC} - 0.1	-	AV_{CC}	V	

Accuracy and setting of the A/D Converter sampling time

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.
To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time depends on the external driving impedance R_{ext}, the board capacitance of the A/D converter input pin C_{ext} and the AV_{cc} voltage level. The following replacement model can be used for the calculation:



R_{ext}: External driving impedance

C_{ext}: Capacitance of PCB at A/D converter input

C_{VIN}: Capacitance of MCU input pin (I/O, analog switch and ADC are contained)

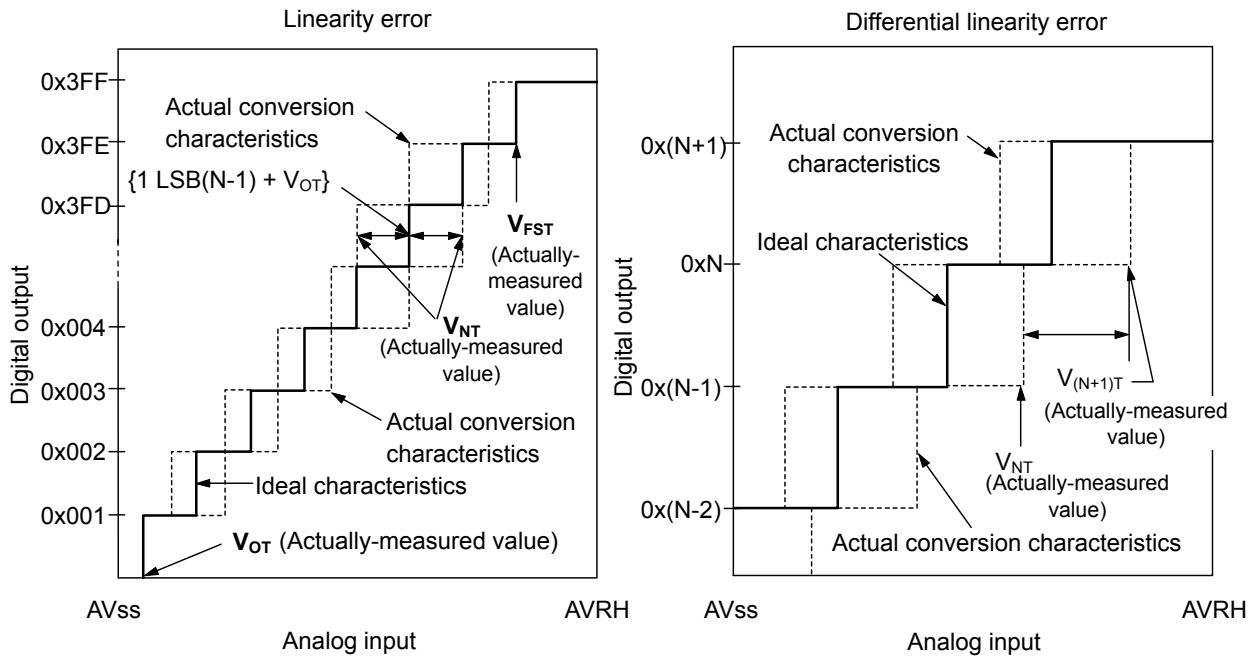
R_{VIN}: Analog input impedance (I/O, analog switch and ADC are contained)

The following approximation formula for the replacement model above can be used:
T_{samp} [min] = TBD

- Do not select a sampling time below the absolute minimum permitted value.
  (0.5µs for 4.5V ≤ AVcc ≤ 5.5V,1.2 µs for 2.7V ≤ AVcc < 4.5V).
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current IIL (static current before the sampling switch) or the analog input leakage current IAIN (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current IIL cannot be compensated by an external capacitor.
- The accuracy gets worse as |AVRH - AV_{SS}| becomes smaller.

• Definition of 10-bit A/D Converter Terms

· Resolution : Analog variation that is recognized by an A/D converter.
· Linearity error : Deviation of the line between the zero-transition point (0b0000000000⟷ 0b0000000001) and the full-scale transition point (0b1111111110⟷ 0b1111111111) from the actual conversion characteristics.
· Differential linearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.
· Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and linearity error.



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB'} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022}$$

N : A/D converter digital output value.
V_{OT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0x3FE to 0x3FF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

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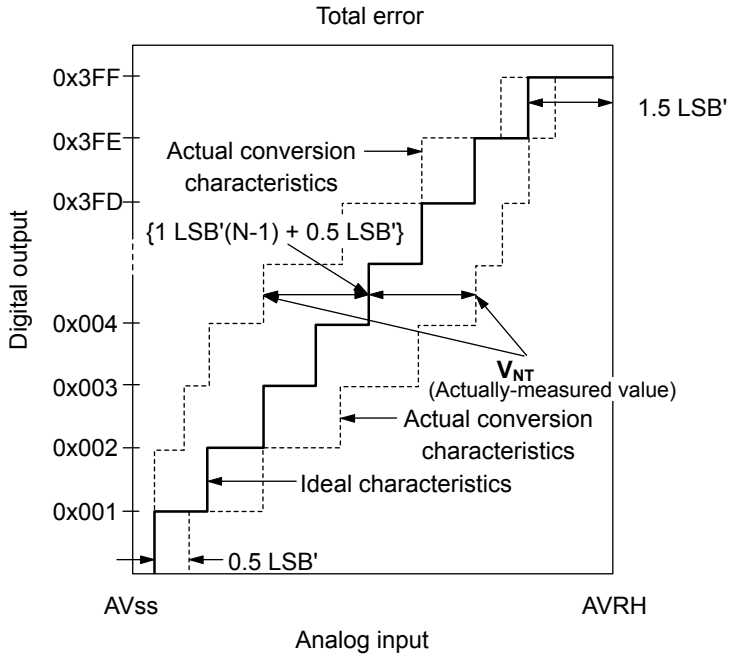


$$1LSB' \text{ (Ideal value)} = \frac{AVRH - AV_{SS}}{1024} \text{ [V]}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1LSB' \times (N - 1) + 0.5LSB'\}}{1LSB'}$$

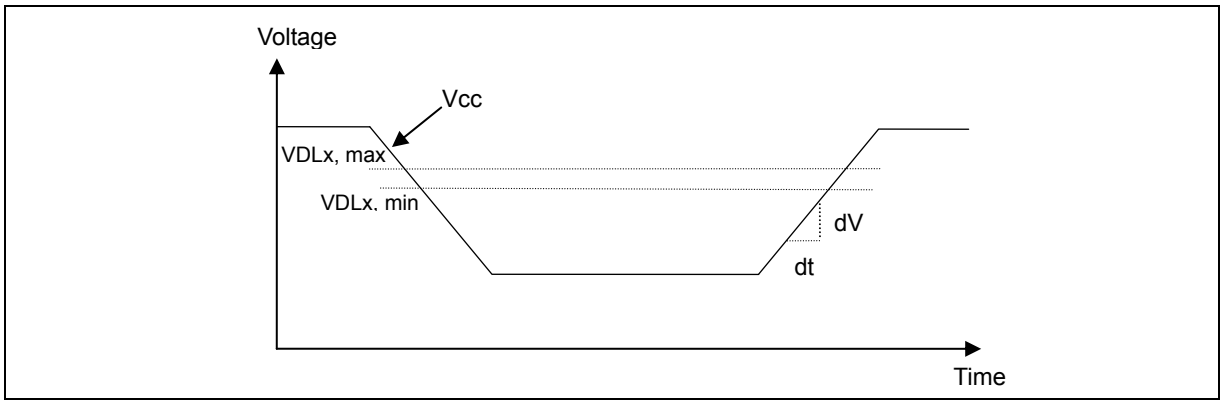
N : A/D converter digital output value.
V_{NT} : Voltage at which the digital output changes from 0x(N + 1) to 0xN.
V_{OT}' (Ideal value) = AV_{SS} + 0.5LSB[V]
V_{FST}' (Ideal value) = AVRH - 1.5LSB[V]

● Low voltage detection characteristics

・Low voltage detection reset

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL0	-	2.70	2.90	3.10	V	CILCR:LVL = 0000_B
Detected voltage	VDL1	-	2.79	3.00	3.21	V	CILCR:LVL = 0001_B
Detected voltage	VDL2	-	2.98	3.20	3.42	V	CILCR:LVL = 0010_B
Detected voltage	VDL3	-	3.26	3.50	3.74	V	CILCR:LVL = 0011_B
Detected voltage	VDL4	-	3.45	3.70	3.95	V	CILCR:LVL = 0100_B
Detected voltage	VDL5	-	3.73	4.00	4.27	V	CILCR:LVL = 0111_B
Detected voltage	VDL6	-	3.91	4.20	4.49	V	CILCR:LVL = 1001_B
Change ration of power supply voltage	dV/dt	-	-0.004	-	-	V/µs	Detected voltage (VDL) must be within standards.



● Flash Memory Write/Erase Characteristics

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 105°C)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	0.6	3.1	s	Excludes write time prior to internal erase.
	Small Sector	-	0.3	1.6	s	
Half word (16 bit) write time		-	25	400	µs	Not including system-level overhead time.
Chip erase time		-	2.7	14.2	s	Excludes write time prior to internal erase.

Erase/write cycles and data hold time (target value)

Erase/write cycles (cycle)	Data hold time (year)
1,000	20 *
10,000	10 *
100,000	5 *

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

■ ORDERING INFORMATION

MCU with CAN controller

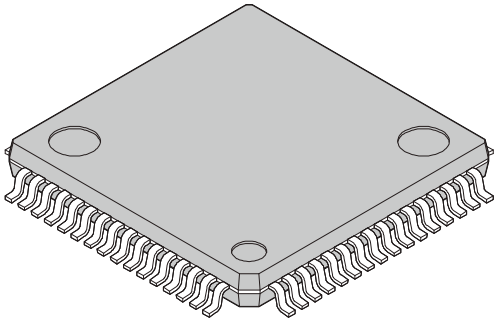
Part number	Flash/ROM	Package
MB96F622RAPMC-GSE1 *	Flash A (64.5KBytes)	64-pin plastic LQFP (FPT-64P-M23)
MB96F622RAPMC-GSE2 *		
MB96F622RAPMC1-GSE1 *		64-pin plastic LQFP (FPT-64P-M24)
MB96F622RAPMC1-GSE2 *		
MB96F623RAPMC-GSE1 *	Flash A (96.5KBytes)	64-pin plastic LQFP (FPT-64P-M23)
MB96F623RAPMC-GSE2 *		
MB96F623RAPMC1-GSE1 *		64-pin plastic LQFP (FPT-64P-M24)
MB96F623RAPMC1-GSE2 *		
MB96F625RAPMC-GSE1 *	Flash A (160.5KBytes)	64-pin plastic LQFP (FPT-64P-M23)
MB96F625RAPMC-GSE2 *		
MB96F625RAPMC1-GSE1 *		64-pin plastic LQFP (FPT-64P-M24)
MB96F625RAPMC1-GSE2 *		

MCU without CAN controller

Part number	Flash/ROM	Package
MB96F622AAPMC-GSE1 *	Flash A (64.5KBytes)	64-pin plastic LQFP (FPT-64P-M23)
MB96F622AAPMC-GSE2 *		
MB96F622AAPMC1-GSE1 *		64-pin plastic LQFP (FPT-64P-M24)
MB96F622AAPMC1-GSE2 *		
MB96F623AAPMC-GSE1 *	Flash A (96.5KBytes)	64-pin plastic LQFP (FPT-64P-M23)
MB96F623AAPMC-GSE2 *		
MB96F623AAPMC1-GSE1 *		64-pin plastic LQFP (FPT-64P-M24)
MB96F623AAPMC1-GSE2 *		
MB96F625AAPMC-GSE1 *	Flash A (160.5KBytes)	64-pin plastic LQFP (FPT-64P-M23)
MB96F625AAPMC-GSE2 *		
MB96F625AAPMC1-GSE1 *		64-pin plastic LQFP (FPT-64P-M24)
MB96F625AAPMC1-GSE2 *		

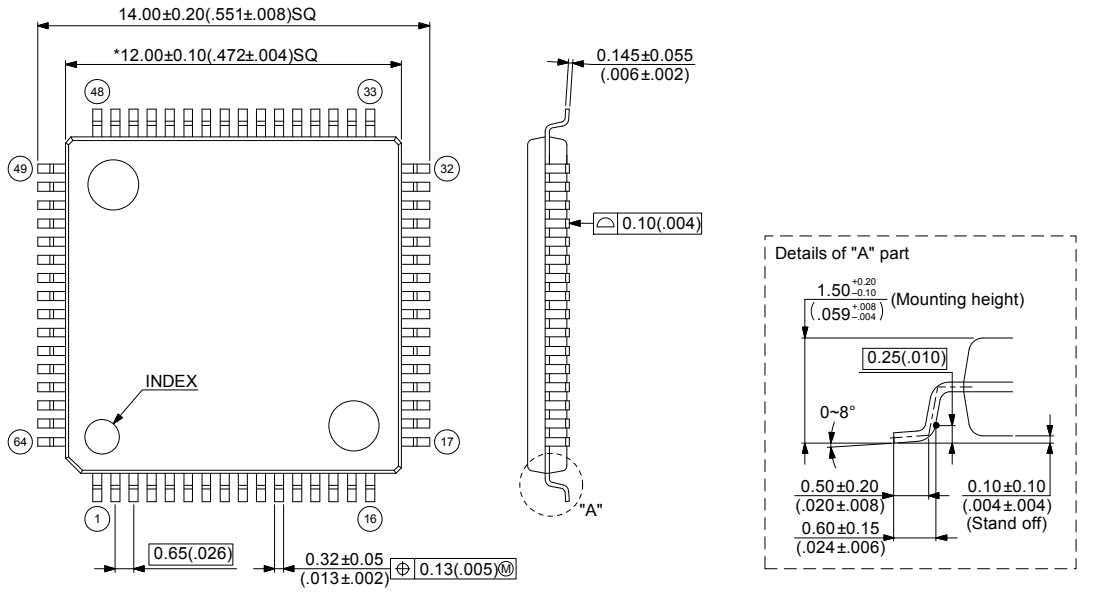
*: These devices are under development and specification is preliminary.
These products under development may change its specification without notice.

■ PACKAGE DIMENSION

64-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.47 g
(FPT-64P-M23)	Code (Reference)	P-LQFP64-12×12-0.65

64-pin plastic LQFP
(FPT-64P-M23)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

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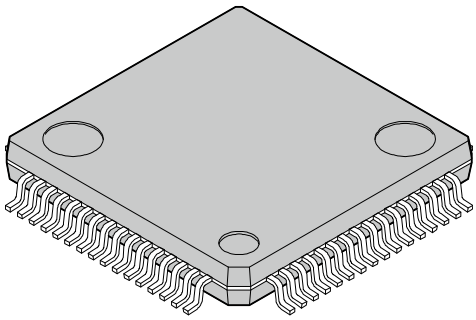
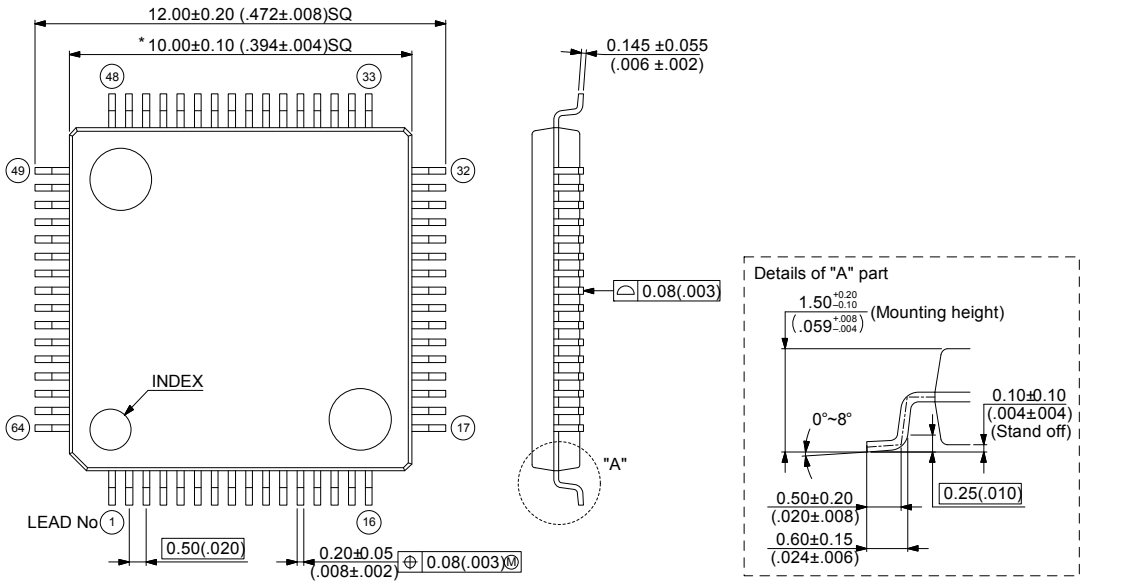
64-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	10.0 × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
(FPT-64P-M24)	Code (Reference)	P-LFQFP64-10×10-0.50

64-pin plastic LQFP
(FPT-64P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ REVISION HISTORY

Revision	Date	Modification
Prelim 1	2011-03-07	Creation

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