GD4531B
13-INPUT PARITY CHECKER GENERATOR

DESCRIPTION — The 4531B is a 13-Input Parity Checker/Generator with 13 Parity Inputs (I_0–I_{12}) and a Parity Output (Z). When the number of Parity Inputs that are HIGH is even, the Output (Z) is LOW. When the number of Parity Inputs that are HIGH is odd, the Output (Z) is HIGH. For words of 12 bits or less, the Output (Z) can be used to generate either odd or even parity by appropriate termination of the unused Parity Input (s). For words of 14 or more bits, the devices can be cascaded by connecting the output (Z) of one device to any Parity Input (I_0–I_{12}) of another device. When cascading devices, it is recommended that the Output (Z) of one device be connected to the I_{12} input of the other device since there is less delay to the Output (Z) from the I_{12} input than from any other Input (I_0-I_{11}).

- **VARIABLE WORD LENGTH**
- **FULLY BUFFERED OUTPUT (ACTIVE HIGH)**
- **PARITY INPUTS (ACTIVE HIGH)**

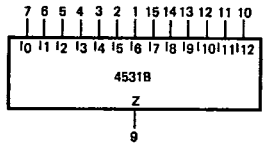
PIN NAMES	FUNCTION
I_0–I_{12}	Parity Inputs
Z	Buffered Output

TRUTH TABLE

INPUTS													OUTPUT
I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	Z
All Thirteen Inputs LOW													L
Any One Input HIGH													H
Any Two Inputs HIGH													L
Any Three Inputs HIGH													H
Any Four Inputs HIGH													L
Any Five Inputs HIGH													H
Any Six Inputs HIGH													L
Any Seven Inputs HIGH													H
Any Eight Inputs HIGH													L
Any Nine Inputs HIGH													H
Any Ten Inputs HIGH													L
Any Eleven Inputs HIGH													H
Any Twelve Inputs HIGH													L
All Thirteen Inputs HIGH													H

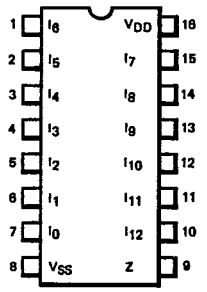
L = LOW Level
H = HIGH Level

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The SO Package has the same pinouts (Connection Diagram) as the Dual In-line Package.

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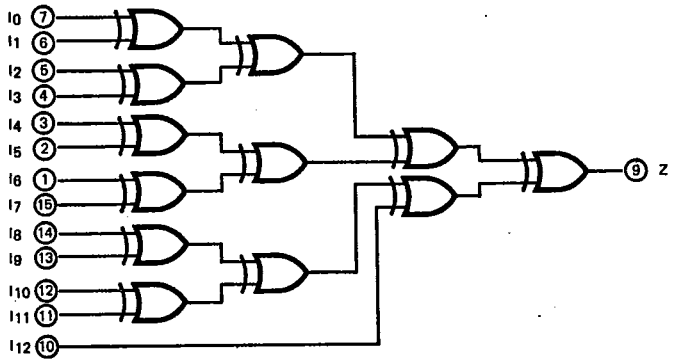
LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, I_0-I_{11} to Z		195	500		80	225		55	180	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}			195	500		80	225		55	180	ns	
t_{PLH}	Propagation Delay, I_{12} to Z		115	300		50	135		35	109	ns	
t_{PHL}			115	300		50	135		35	109	ns	
t_{TLH}	Output Transition Time		65	135		35	75		15	45	ns	
t_{THL}			65	135		35	75		15	45	ns	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.